Integrated Atomistic Process and Device Simulation of Decananometre MOSFETs

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***Abstract* – In this paper we present a methodology for the integrated atomistic process and device simulation of decananometre MOSFETs. The atomistic process simulations were carried out using the kinetic Monte Carlo process simulator DADOS, which is now integrated into the Synopsys 3D process and device simulation suite Taurus. The device simulations were performed using the Glasgow 3D statistical atomistic simulator, which incorporates density gradient quantum corrections. The overall methodology is illustrated in the atomistic process and device simulation of a well behaved 35 nm physical gate length MOSFET reported by Toshiba.**

I. INTRODUCTION

According to the 2001 edition of the International Technology Roadmap for Semiconductors, MOSFETs with physical channel length less than 10 nm will be in mass production by 2016 [1]. Such devices (Fig. 1) will have approximately 10 silicon atoms along the effective channel length and the position of each silicon, dopant or insulator atom is likely to have a macroscopic impact on the device characteristics.

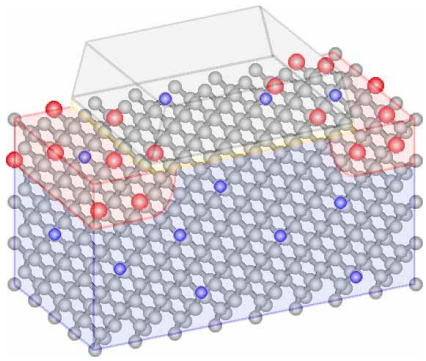

Fig. 1: Impression of a 5 nm MOSFET with the silicon crystal lattice superimposed.

It is well known that the discrete random distribution of dopants [2], atomic scale silicon/insulator interface roughness [3] and gate line edge roughness (LER) [4] create increasingly large parameter fluctuations in decananometre MOSFETs. However, until now the discrete dopant distribution in device simulation studies of intrinsic fluctuation effects were generated, to a great extent, superficially from the corresponding continuous doping distribution using a range of stochastic techniques [2, 5].

Previous approaches exclude possible correlations in the discrete dopant distribution introduced at the implantation/annealing stage by electrostatic interactions [6] and large defect conglomerates [7]. The next advance in improving the degree of realism in the atomistic device simulations is to use discrete dopant distributions generated from atomistic process simulators. Recent progress in atomistic process simulation has now made this possible [8].

II. ATOMISTIC PROCESS SIMULATION

In a 'standard' statistical atomistic process simulation, a continuous doping profile – obtained analytically or by using PDE based process simulators – is used to generate the random discrete dopant distributions in large samples of macroscopically identical but microscopically different devices, using a variety of stochastic techniques [2,5]. Here we explore the possibility of using DADOS as a direct source of stochastic discrete dopant distribution for statistical atomistic device simulation.

The Kinetic Monte Carlo (KMC) simulator DADOS [7, 8] has been developed over a number of years to study fundamental physical diffusion phenomena in silicon. Its integration in the commercial TCAD tool Taurus [9] now allows the simulation of complete process flow including implant, etch, deposition, anneal, oxidation, epitaxy and silicidation and enables the complete atomistic process simulation of realistic devices. The integration has required enhancements of present atomistic diffusion simulations at the level of physical models (e.g. for modelling of the interaction at material interfaces or self-consistent inclusion of the electric field) and to data structure and algorithms. As devices scale below 100 nm, reducing the device dopant count, KMC simulations become increasingly viable for practical TCAD, and, even for larger scale devices, KMC may play a fundamental role in extracting parameters for the models to be used in continuum based simulators. For our present purposes KMC process simulations are also an excellent source of the random discrete dopant distributions needed to improve the realism and the accuracy of atomistic device simulations. The integrated atomistic process and

device simulations will help to provide a better understanding of the characteristics of intrinsic parameter fluctuations in next generation devices and the restrictions that such fluctuations may impose on device scaling in the silicon end game.

In this paper, the integrated atomistic process and device simulation methodology is exemplified through the extraction of the intrinsic parameter fluctuations introduced by random discrete dopants in a 35 nm, n-channel MOSFET. This device, developed by Toshiba [10] and depicted schematically in Fig. 2, is at present the best performer at the 80 nm technology node expected to be in mass production by 2005. Well documented structure and doping profiles, critical for reliable simulator calibration, were the primary reasons for our choice of this device.

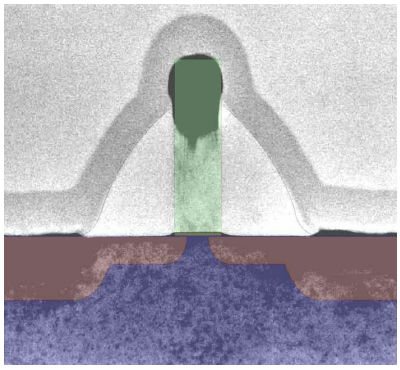

Fig. 2: Schematic view of the 35 nm Toshiba MOSFET

We start with careful calibration of the current voltage characteristics using continuous doping distribution in order to confirm and refine the structure and the doping profiles in the measured device. As illustrated in Fig. 3 the standard drift diffusion simulation results obtained from Taurus and our 3D simulator using similar continuous doping distributions are both in very good agreement with the measured device characteristics.

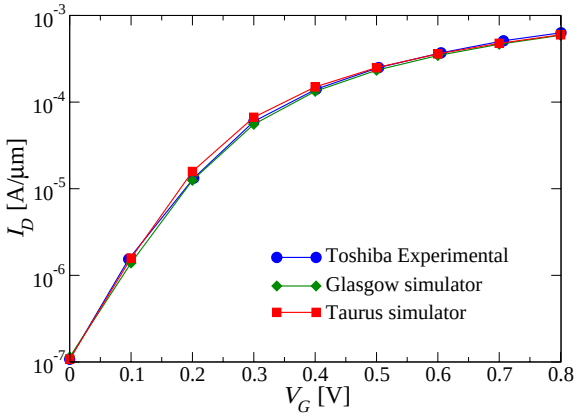

Fig. 3: Experimental and simulated current-voltage characteristics of the device from Fig. 2.

The continuous and the atomistic doping distributions in the source/drain regions of the test MOSFETs are compared in Fig. 4. The continuous profile is obtained using PDE based diffusion simulation and the discrete dopant distribution is obtained from a DADOS diffusion simulation.

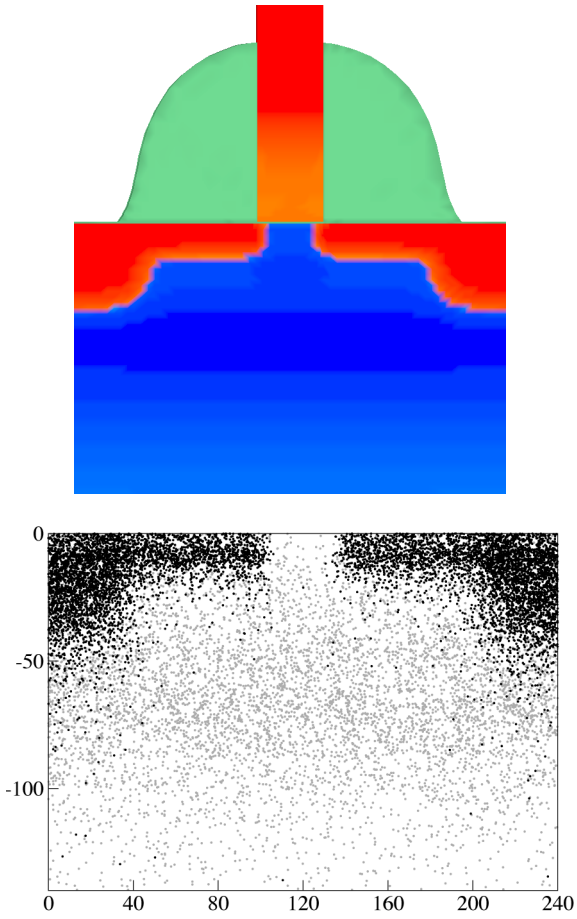

Fig. 4: Dopant distribution in the test MOSFET. a) continuous net doping distribution from PDE based process simulation; b) discrete dopant distribution from DADOS.

III. ATOMISTIC DEVICE SIMULATION

The Glasgow atomistic statistical 3D device simulator is described in detail elsewhere [2]. It solves the semiconductor equations in the drift-diffusion approximation utilising efficient parallel solution techniques on a rectilinear mesh. This means that dopants imported from the DADOS simulations that are located within the continuum of the silicon must be assigned to the nodes of the rectilinear mesh of the device simulator. To perform this task the dopant coordinates in the DADOS output file are imported into the atomistic device simulator. For each dopant we perform a check to establish the mesh 'brick' in which it resides and then assign a weighted fraction of the unit electronic charge to the eight mesh nodes at the corner of the brick using the cloud in cell charge assignment method widely used in particle based Monte Carlo device simulators [11]. A band of continuous doping at the source/drain edges and the device substrate is introduced to simplify boundary conditions.

Although simple to implement, this dopant assignment strategy can introduce problems when a fine mesh spacing is used – particularly in source/drain regions in an attempt to resolve the contribution of individual discrete dopants. These are approximately 2 nm apart at a doping concentration of 10^{20} cm^{-3}. The origin of these problems is apparent from Fig. 5*a* which illustrates the potential distribution at the Si/SiO_2 interface of the test device when continuous acceptor doping is used in the channel region but discrete random donors are introduced in the source and drain junctions.

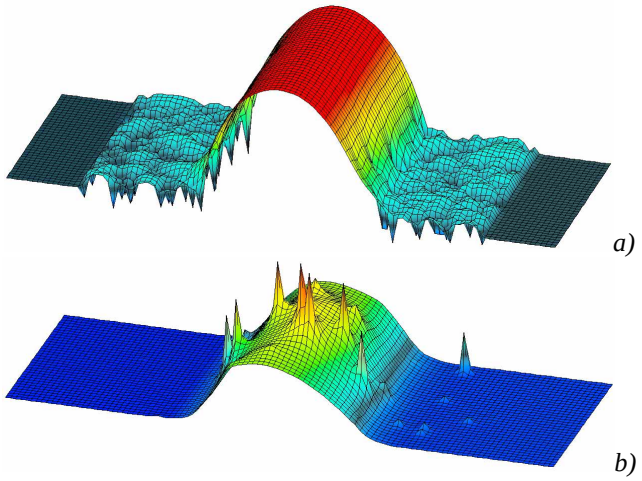

Fig. 5: 2D potential distribution at the Si/SiO_2 interface of the 35 nm MOSFET: a) continuous channel and atomistic source/drain doping; b) atomistic channel and continuous source/drain doping.

A uniform grid with mesh spacing 1 nm is used in this case. In classical drift diffusion simulations a significant number of electrons in the source/drain region become trapped in the valleys of the Coulomb potential of ionised donors which are sharply resolved by the fine mesh, and which in reality are prohibited due to electron energy quantisation. This reduces the effective concentration of mobile electrons and artificially increases the resistance of the source/drain regions. Attempts to split the Coulomb potential into short and long-range components for the purpose of the atomistic simulation have been made in the past [12], but they suffer shortfalls and at present there is no commonly agreed strategy for dealing with the problem. In our simulations presented below, atomicity is included in the channel, source and drain regions, and the artificial trapping is compensated by increasing the electron mobility in source and drain regions.

Fortunately such problems are absent in the channel region where the resolution of the Coulomb barriers associated with ionised acceptors do not influence significantly the current flow through the potential valleys. Therefore the previously reported results in the literature, where the main source of intrinsic parameter fluctuations are the random dopants in the channel region, remain valid.

Further insight into the atomistic device simulation is provided in Fig. 6, which illustrates the potential and the electron concentration distributions for the dopant distribution of Fig. 4*b*. In the equiconcentration contour plot the position of the individual acceptors (blue) and donors (red) are also marked.

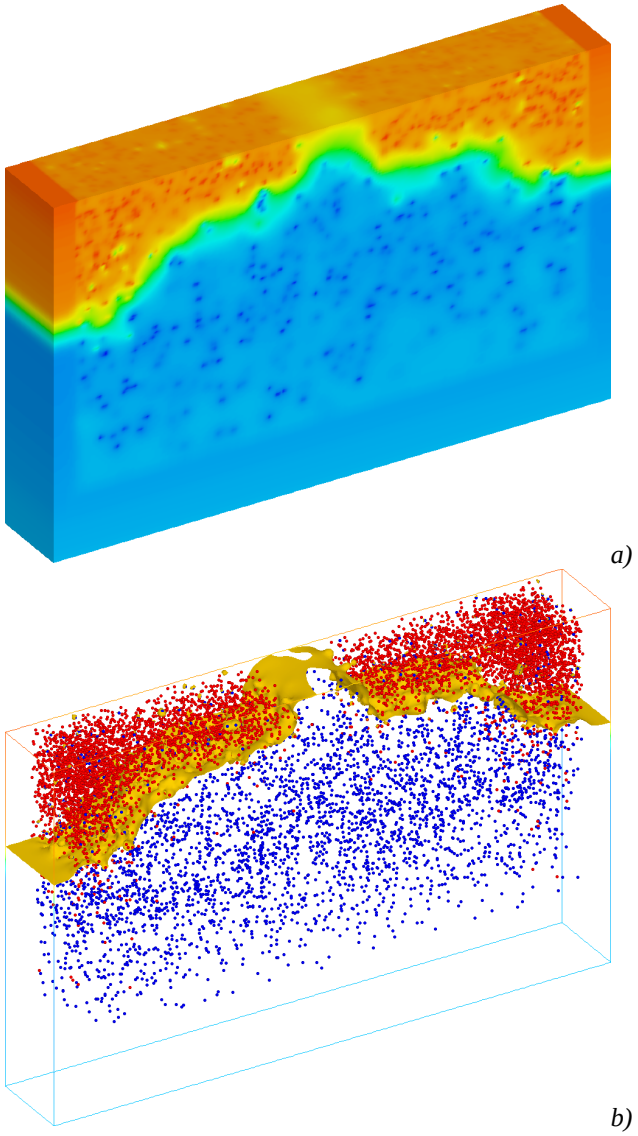

Fig. 6: a) Potential and b) electron concentration distribution in the 35 nm test MOSFET at V_G = 0 V and V_D = 0.01 V.

Atomistically simulated current-voltage characteristics for 50 microscopically different test MOSFETs are compared in Fig. 7 with the results of continuous doping simulations. As previously reported [13,14], in addition to the macroscopic variation of device parameters, the averaged current from an ensemble of atomistic simulations is different from that obtained using continuous doping. Aside from the obvious device implications, this introduces new challenges for the proper calibration of atomistic device simulations, which have to be made with respect to the average and standard deviation of a statistical ensemble of measured devices. This is further complicated as the

standard deviation in the current varies with applied gate voltage as illustrated in Fig. 8.

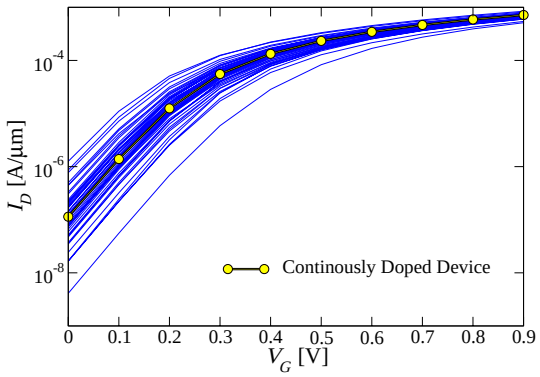

Fig. 7: Comparison between the atomistically simulated current voltage characteristics of a sample of 50 microscopically different test MOSFETs with results obtained from continuous doping.

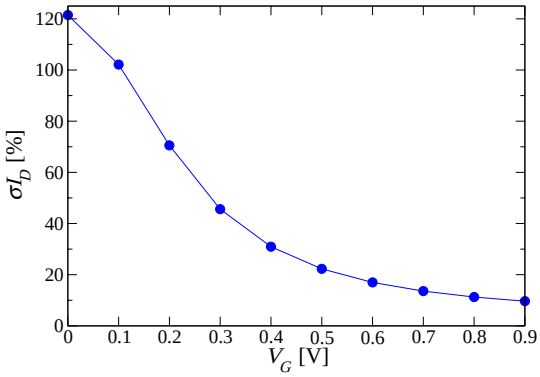

Fig. 8: Dependence of the standard deviation of the MOSFET current on gate voltage.

IV. FUTURE CHALLENGES

In addition to studying intrinsic parameter fluctuations introduced by discrete random dopants, the integrated simulation approach will be indispensable for investigating the combination of various sources of intrinsic parameter fluctuations.

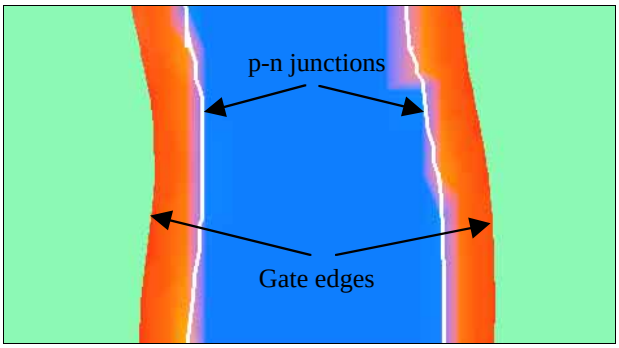

Fig. 9: Process simulation with Taurus Process including LER associated with gate patterning of the test MOSFET.

Fig. 9 illustrates the gate shape and the continuous doping profile for the 35 nm MOSFET when gate LER is introduced in the process simulation using the statistical approach outlined in [4]. The future goal is to combine the contribution from line edge roughness and random discrete dopants in the simulation of intrinsic parameter fluctuations.

V. CONCLUSIONS

In this paper we have presented the methodology and provisional results illustrating the integration of atomistic process and device simulation. This is the only consistent approach for studying intrinsic parameter fluctuations introduced by discrete random dopants in the next generation decananometre MOSFETs.

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