

**Problem Solutions to Problems Marked With a \* in  
Logic Computer Design Fundamentals, Ed. 2**

**CHAPTER 9**

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**9-2.**

a) LD R1, A	b) MOV T1, A	c) LD A
LD R2, B	ADD T1, C	ADD C
LD R3, C	MOV T2, B	ST T1
LD R4, D	MUL T2, D	LD B
ADD R3, R1, R3	MOV T3, A	MUL D
ADD R1, R1, R2	ADD T3, B	ST T2
MUL R2, R2, R4	MUL T3, T1	LD A
MUL R1, R3, R1	SUB T3, T2	ADD B
SUB R1, R1, R2	MOV Y, T3	MUL T1
ST Y, R1		SUB T2
		ST Y

**9-3.**

A)  $(A + B) \times (A + C) - (B \times D) = AB + CA + \times BD \times -$

B,C)

<b>PUSH A</b>	<b>PUSH B</b>	<b>ADD</b>	<b>PUSH A</b>	<b>PUSH C</b>	<b>ADD</b>
A	B	A+B	A	C	A+C
	A		A+B	A	A+B
				A+B	

  

<b>MUL</b>	<b>PUSH B</b>	<b>PUSH D</b>	<b>MUL</b>	<b>SUB</b>
(A+B)x(A+C)	B	D	BxD	(A+B)x(A+C) - BxD
	(A+B)x(A+C)	B	(A+B)x(A+C)	
		(A+B)x(A+C)		

**9-6.**

a)  $X = 200 - 208 - 1 = -9$     b)  $X = 1111\ 1111\ 1111\ 0111$

**9-9.**

address field = 0

**9-11.**

- a) 3 Register Fields x 5 bits/Field = 15 bits. 32 bits - 15 bits = 17 bit.  $2^{17} = 131,072$   
 b) 256 = 8 bits. 2 Register Fields x 5 bits/Field = 10 bits. 32 bits - 8 bits - 10 bits = 14 Memory Bits

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**Problem Solutions – Chapter 9**

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**9-13.**

Read and Write of the FIFO work in the following manner:

Write:  $M[WC] \leftarrow DATA$                       Read:  $DST \leftarrow M[RC]$   
 $ASC \leftarrow ASC + 1$                                        $ASC \leftarrow ASC - 1$   
 $WC \leftarrow WC + 1$      $RC \leftarrow RC + 1$

	WC	RC	ASC
WR	1	0	1
WR	2	0	2
RD	2	1	1
RD	2	2	0

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**9-17.**

- |  |  |
|--|--|
| <p>a) ADD R0, R4<br/>         ADC R1, R5<br/>         ADC R2, R6<br/>         ADC R3, R7</p> | <p>b) <math>R0 \leftarrow 8C + 5C</math>,      <math>R0 = E8</math>,   <math>C = 0</math><br/> <math>R1 \leftarrow 35 + FE + 0</math>,      <math>R1 = 33</math>,   <math>C = 1</math><br/> <math>R2 \leftarrow D7 + 68 + 1</math>,      <math>R2 = 40</math>,   <math>C = 1</math><br/> <math>R3 \leftarrow 2B + 11 + 1</math>,      <math>R3 = 3D</math>,   <math>C = 0</math></p> |
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**9-20.**

OPP	Result Register	C
SHR	0101 1101	1
SHL	1011 1010	1
SHRA	1101 1101	1
SHLA	1011 1010	1
ROR	0101 1101	1
ROL	1011 1010	1
RORC	1101 1101	0
ROLC	1011 1010	1

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**9-22.**

$$\begin{aligned} \text{Smallest Number} &= 0.5 \times 2^{-255} \\ \text{Largest Number} &= (1 - 2^{-26}) \times 2^{+255} \end{aligned}$$

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**9-24.**

E	e	(e) <sub>2</sub>
+8	15	1111
+7	14	1110
+6	13	1101
+5	12	1100
+4	11	1011
+3	10	1010
+2	9	1001
+1	8	1000
0	7	0111
-1	6	0110
-2	5	0101
-3	4	0100
-4	3	0011
-5	2	0010
-6	1	0001
-7	0	0000

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**Problem Solutions – Chapter 9**

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**9-27.**

TEST R, (0001)<sub>16</sub>      (AND Immediate 1 with Register R)  
BNZ ADRS              (Branch to ADRS if Z = 0)

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**9-29.**

a)    A =    0011 0101            53  
      B =    0011 0100            - 52  
      A - B = 0000 0001            1

b) C (borrow) = 0,    Z = 0

c) BH, BHE, BNE

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**9-31.**

	PC	SP	TOS
a) Initially	2000	2735	3250
b) After Call	2147	2734	2002
c) After Return	2002	2735	3250

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**9-34.**

External Interrupts:

- 1) Hard Disk
- 2) Mouse
- 3) Keyboard
- 4) Modem
- 5) Printer

Internal Interrupts:

- 1) Overflow
- 2) Divide by zero
- 3) Invalid opcode
- 4) Memory stack overflow
- 5) Protection violation

A software interrupt provides a way to call the interrupt routines normally associated with external or internal interrupts by inserting an instruction into the code. Privileged system calls for example must be executed through interrupts in order to switch from user to system mode. Procedure calls do not allow this change.