Nonlinearity Correction for Multibit $\Delta\Sigma$ DACs

Jesus Arias, Peter Kiss, Vito Boccuzzi, Luis Quintanilla, Lourdes Enriquez, José Vicente, David Bisbal, Jacinto San Pablo, and Juan Barbolla

***Abstract*—This paper presents a digital correction technique for wide-band multibit error-feedback (EF) digital-to-analog converters (DACs). The integral nonlinearity (INL) error of the multibit DAC is estimated (on line or off line) by a calibration analog-to-digital converter (CADC) and stored in a random-access memory table. The INL values are then used to compensate for the multibit DAC's distortion by a simple digital addition. The accuracy requirements for the error estimates are derived. These requirements can be significantly relaxed when the correction is combined with data-weighted averaging (DWA). Simulation and discrete-component measurement results are presented for a fourth-order 5-bit EF DAC. The results show a 14-bit DAC operating at an oversampling ratio of 8, which is suitable for digital subscriber line applications. The correction uses simple digital circuitry and a 3-bit CADC enhanced by DWA.**

***Index Terms*—Data-weighted averaging (DWA), digital–analog conversion, digital correction, digital subscriber lines (DSLs), high speed, multibit, nonlinearities, nonlinearity correction, sigma–delta modulation.**

I. Introduction

THE USE OF multibit quantizers in delta–sigma modulators has great advantages over single-bit ones, such as increased signal-to-noise ratio (SNR) and improved stability [1]. However, the performance bottleneck is usually the linearity of the internal multibit "analog" digital-to-analog converter (ADAC[1]), which needs to be at least as good as that of the overall converter. This limitation applies for both multibit delta–sigma analog-to-digital converters (ADCs), see Fig. 1(a) and DACs, see Fig. 1(b) [1].

There are many known techniques to deal with the nonlinearity of the multibit ADAC in delta–sigma modulators. Dynamic element matching, also called mismatch shaping [1]–[7], transform harmonic distortion into shaped pseudo-random noise, which is usually acceptable in the output. There are several methods that can achieve first-order shaping such as individual-level averaging [3], data-weighted averaging (DWA) [4], vector feedback [5], butterfly structures [6], selection trees [7], etc. However, first-order methods require relatively high values (say, 16 or higher) of the oversampling ratio (OSR) to be effective. Therefore, second-order mismatch shaping techniques were developed [5], [7]. However, second-order methods need increased circuit complexity, which boost up the power consumption and require large integrated chip area.

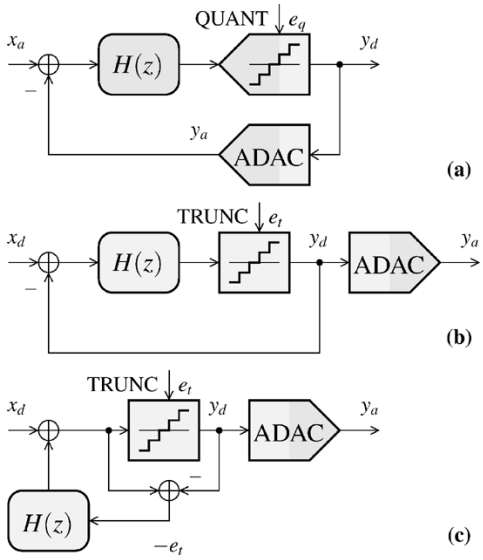

Fig. 1. Single-loop delta–sigma modulator topologies. (a) Delta–sigma ADC. (b) Delta–sigma DAC. (c) EF DAC.

In addition to dynamic element matching, off-line [8] and on-line [9], [10] digital calibration, as well as on-line analog [11] correction have been used. An on-line digital linearizing technique, based on correlation operations, was also suggested by Galton [12] for ADACs embedded into pipelined ADCs.

It was shown recently [13] that multibit error-feedback (EF) modulators Fig. 1(c) can use aggressive noise-transfer functions (NTFs) without compromising stability and, therefore, achieve high resolution even for low (say, 4 or 8) OSR values. The EF topology is not suitable for delta–sigma ADCs since the imperfections of the analog loop filter $H(z)$ would enter the critical input node and adversely affect the output. However, this drawback does not exist in digital modulator loops. Therefore, EF modulators are widely used in delta–sigma DACs [14], [15] and fractional-N phase-locked loops (PLLs) [16].

A fourth-order 5-bit EF DAC was proposed in [13], which used an aggressive NTF. Since only 10-bit signal-to-noise-and-distortion ratio (SNDR) was targeted at an OSR of 4, using DWA was sufficient to handle the 5-bit ADAC's nonlinearity. The same fourth-order 5-bit EF DAC can potentially achieve 14 bits of resolution (88.9-dB SNR) for an OSR of 8. This accuracy, however, cannot be achieved with DWA (alone) at such a low OSR.

This paper proposes a digital correction of multibit ADAC nonlinearities for EF DACs to extend its performance well

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[1]In this paper, the embedded DAC is called "ADAC," as opposed to the "global" delta–sigma DAC, which includes the digital delta–sigma modulator.

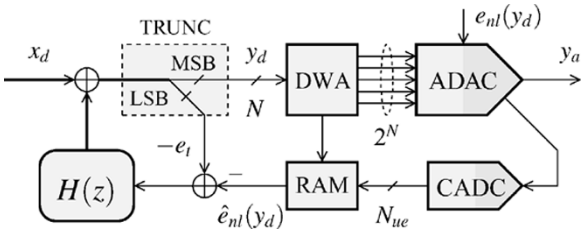

Fig. 2. EF DAC with the proposed digital correction.

beyond 10 bits of resolution. In this approach the integral nonlinearity (INL) error of the multibit ADAC is estimated (on line or off line) by a low-resolution calibration ADC (CADC) and stored in a random-access-memory (RAM) table (Fig. 2). The INL values are then used to compensate for the ADAC's distortion in the digital domain. When this compensation is combined with mismatch-shaping techniques such as DWA [4], the resolution requirement for CADC can be relaxed significantly. The concept of the proposed RAM-based correction is similar to [8], used in delta–sigma ADCs , and to [17], applied for chain-of-accumulator delta–sigma DACs . However, the implementation of the proposed correction circuit for EF modulators is inherently simpler, since the correction only consist of a digital summation without any additional digital filtering as required in [17].

After this introduction, Section II presents the proposed nonlinearity correction. Then simulation and discrete-component experimental results are presented for a fourth-order 5-bit (32-element) EF DAC in Section III. The results demonstrate the feasibility of achieving 10-bit and 14-bit performance at a low OSR of 4 and 8, respectively. The proposed DAC uses simple circuitry to implement the digital modulator, the necessary error scrambling and correction.

II. Proposed Nonlinearity Correction

A. Ideal EF DAC

The block diagram of an EF DAC is shown in Fig. 1(c). The truncator (TRUNC) provides the most-significant bits (MSB) for the following DAC, and feeds the least-significant bits (LSB) to the digital loop filter $H(z)$. Using the additive white-noise model [1, Sec. 2.3] for the truncator, which replaces a deterministic nonlinearity with a stochastic linear system, it results in

$$\begin{aligned} Y_d(z) &= X_d(z) + (1 - H(z))\, E_t(z) \\ &= STF(z)\, X_d(z) + \mathrm{NTF}(z)\, E_t(z) \end{aligned} \tag{1}$$

where e_t is the truncation error [similar to the quantization error e_q in Fig. 1(a)], $STF(z) = 1$ is the signal transfer function and $\mathrm{NTF}(z) = 1 - H(z)$ is the truncation error (or truncation noise) transfer function.

The digital EF modulator is followed by a multibit ADAC, which converts the digital output y_d into a proportional analog waveform y_a, i.e., $y_a = \kappa \cdot y_d$. For simplicity of calculations, the scaling factor κ can be assumed to be unity for ADAC, so $y_a = y_d$. Since ADAC is in the critical path, its performance should be at least as good as that of the overall converter.

B. Proposed Error Correction

In practical scenarios, ADAC is affected by nonlinearity errors. These errors can be modeled as an input-dependent additive term $e_{\mathrm{nl}}(y_d)$, as shown in Fig. 2. When no correction is applied, the distorted output becomes

$$Y_a(z) = X_d(z) + \mathrm{NTF}(z)\, E_t(z) + E_{\mathrm{nl}}(z). \tag{2}$$

The estimated values $\hat{e}_{\mathrm{nl}}$ of the errors e_{nl} are determined by CADC and stored in the RAM table. One can decompose $\hat{e}_{\mathrm{nl}}$ into $e_{\mathrm{nl}} + \delta e_{\mathrm{nl}}$, where e_{nl} is the actual nonlinearity error of ADAC and δe_{nl} is the inaccuracy of the nonlinearity error's estimate due to CADC.

During normal operation, the $\hat{e}_{\mathrm{nl}}(y_d)$ value, corresponding to the current digital output y_d, is read from the RAM table and subtracted from the negated truncation error "$-e_t$" [Fig. 2]. In other words, "$-e_t - \hat{e}_{\mathrm{nl}}$" is fed back to the digital loop filter $H(z)$. From (2), therefore, the distorted output after correction becomes

$$\begin{aligned} &Y_a(z) \\ &= X_d(z) + \mathrm{NTF}(z)\left(E_t(z) + \hat{E}_{\mathrm{nl}}(z)\right) + E_{\mathrm{nl}}(z) \\ &= X_d(z) + \mathrm{NTF}(z)E_t(z) + \mathrm{NTF}(z)E_{\mathrm{nl}}(z) - H(z)\delta E_{\mathrm{nl}}(z). \end{aligned} \tag{3}$$

The loop filter $H(z)$ has a magnitude of unity within the signal band, since $H(z) + \mathrm{NTF}(z) = 1$ (from (1)) and $|\mathrm{NTF}(z)| \ll 1$ within the signal band. Therefore, the corrected output can be approximated as

$$Y_a(z) \cong X_d(z) + \mathrm{NTF}(z)E_t(z) + \mathrm{NTF}(z)E_{\mathrm{nl}}(z) - \delta E_{\mathrm{nl}}(z) \tag{4}$$

where the first two terms describe the ideal output given in (1), and the last two terms give the nonlinearity error's contribution after digital correction.

As (4) shows, the truncation error e_t and the nonlinearity error e_{nl} of the ADAC are shaped in frequency by the same NTF. When a high-order EF modulator is used, a high-order shaping of the truncation error and of the nonlinearity error is achieved. Therefore, this method is effective even at low OSRs .

Equation (4) also shows that the inaccuracies δe_{nl} of the error estimation do not exhibit frequency shaping, and they directly degrade the precision of the corrected output. When the correction is combined with first-order mismatch-shaping techniques, δe_{nl} gets also first-order shaped, and the resolution requirement for the CADC can be relaxed significantly, as derived in Section II.C.

In conclusion, the proposed correction "replaces" the nonlinearity error e_{nl} (2) with the nonlinearity error's estimate δe_{nl} (4). While strongly reducing e_{nl} at low OSRs requires the use of high-order mismatch-shaping techniques, δe_{nl} can be made much smaller than e_{nl} by employing the proposed correction enhanced by first-order mismatch-shaping methods, such as DWA [4]. This paper shows that implementing the latter needs simple circuitry.

C. Error Estimation Process

Estimating the actual nonlinearity of the ADAC can be done off-line or on-line. This process involves the measurement of

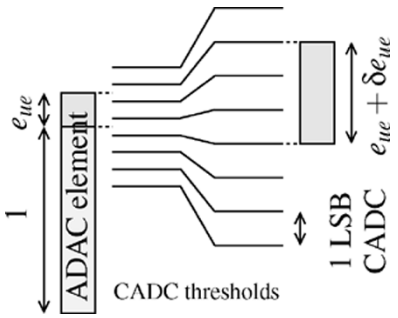

Fig. 3. Error estimation by CADC.

the relative error of each ADAC unit element via CADC, and the computation of the RAM table entries that is merely the addition of the unit-element errors of all the selected elements (Fig. 2). For on-line calibration the ADAC must include a redundant element to replace the element under measurement.

Fig. 3 shows the error estimation process. For an N-bit ADAC, there are 2^N unit elements (Fig. 2). Each unit element has a normalized value of 1 and it is affected by an error $e_{\rm ue}$ due to circuit-element mismatch. This error is measured by comparing the ADAC element with a reference element and by amplifying the resulting error before the CADC conversion. The error $e_{\rm ue}$ is affected by an inaccuracy $\delta e_{\rm ue}$ mainly due to the finite resolution of CADC.

At each clock cycle n, $y_d[n]$ determines how many unit elements of ADAC are selected to generate an analog value for $y_a[n]$. The error scrambler, e.g., DWA, chooses which elements are selected (specified by a set of elements $S[n]$) according to the mismatch shaping algorithm. The nonlinearity error $e_{\rm nl}$ of ADAC at each clock cycle n is given by the sum of the errors of the selected unit elements

$$e_{\rm nl}(y_d[n]) = \sum_{i\in S[n]} e_{\rm ue}(i). \tag{5}$$

Since the error estimates $\hat{e}_{\rm nl}$ and $\hat{e}_{\rm ue}$ can be decomposed into $e_{\rm nl}+\delta e_{\rm nl}$ and $e_{\rm ue}+\delta e_{\rm ue}$, respectively, (5) holds for inaccuracies too

$$\delta e_{\rm nl}(y_d[n]) = \sum_{i\in S[n]} \delta e_{\rm ue}(i). \tag{6}$$

Initially, one may assume a white spectral density and a normal distribution for these error terms. Therefore, $\sigma_{\rm nl}$ and $\sigma_{\rm ue}$ are used to represent the standard deviation of the random variables $\delta e_{\rm nl}$ and $\delta e_{\rm ue}$, respectively.

Since $\delta e_{\rm ue}$ is mainly due to the quantization error of CADC, it is convenient to express $\sigma_{\rm ue}$ as a function of the number of bits $N_{\rm ue}$ of CADC. For a quantizer of $N_{\rm ue}$ bits with its quantization error uniformly distributed over $-1/2 \ldots 1/2\,\text{LSB}$, the standard deviation of the quantization error is given by

$$\sigma_{\rm ue} = \frac{1\,\text{LSB}}{\sqrt{12}} = \frac{1}{\sqrt{12}}\,\frac{1}{2^{N_{\rm ue}-1}} \tag{7}$$

where the full scale of CADC is normalized to 1. Therefore

$$N_{\rm ue} \cong \frac{\log_2 0.3}{\sigma_{\rm ue}} \quad [\text{bits}]. \tag{8}$$

Similarly, $\sigma_{\rm nl}$ can also be expressed by a corresponding $N_{\rm nl}$-bit quantizer of

$$N_{\rm nl} \cong \frac{\log_2 0.3}{\sigma_{\rm nl}} \quad [\text{bits}]. \tag{9}$$

Note that the values of the selected unit elements are summed together to generate an analog value for y_a, so the estimation errors $\delta e_{\rm ue}$ of the unit elements get "averaged" in this process and the relative accuracy of the overall ADAC is better than that of a single element. Based on the derivation of [1, Sec. 8.3.1], it results in

$$\sigma_{\rm nl} = \frac{1}{2\sqrt{2^N}}\,\sigma_{\rm ue}. \tag{10}$$

Therefore, only a fraction of the error $\delta e_{\rm ue}$ of CADC affects the actual output y_a. In other words, $\sigma_{\rm ue}$ can be $2^{N/2+1}$ times larger than $\sigma_{\rm nl}$, i.e., $N_{\rm ue}$ can be $N/2+1$ bits less than $N_{\rm nl}$.

In the following section, an approximation of the required accuracy for CADC is derived.

D. Required Accuracy for Error Estimation

The overall SNDR of the corrected converter is limited by many noise and distortion elements, such as the shaped truncation error e_t, the shaped nonlinearity error $e_{\rm nl}$, and the nonshaped nonlinearity error's estimate $\delta e_{\rm nl}$, as shown in (4). Usually, the dominant contributors are the shaped truncation error e_t and the nonshaped nonlinearity error's estimate $\delta e_{\rm nl}$. It is generally acceptable that the overall SNDR of the corrected converter to drop by about 1 dB from its ideal (i.e., truncation-error limited) value due to imperfect nonlinearity error correction. Therefore, as a rule of thumb, the resolution of CADC should be chosen such that the in-band power of $\delta e_{\rm nl}$ should be 6 dB lower than the in-band power of the shaped e_t. Obviously, the noise budget resulting from (4) can be distributed differently when needed.

Next, an approximation of the required accuracy for CADC is derived. Again, this approximation assumes white power spectral density and normal distribution for the error terms. First, the achievable SNR of the corrected output y_a, when limited by $\delta e_{\rm nl}$ only, is given by [18]

$$\text{SNR}_0 = 1.76 + 6.02\,(N_{\rm nl}+N) + 10\,\log_{10}(\text{OSR}) \quad [\text{dB}] \tag{11}$$

where N is the number of bits of y_d. When first-order mismatch shaping is used, (11) becomes [18]

$$\text{SNR}_1 = 1.76 + 6.02(N_{\rm nl}+N) + 30\log_{10}(\text{OSR}) - 5.17 \quad [\text{dB}]. \tag{12}$$

Since $N_{\rm ue}$ can be $N/2+1$ bits less than $N_{\rm nl}$ according to (10)–(12), thus, become

$$\begin{aligned}\text{SNR}_0 &= 1.76 + 6.02(N_{\rm ue} + 1.5N + 1) \\ &\quad + 10\,\log_{10}(\text{OSR}) \quad [\text{dB}] \end{aligned} \tag{13}$$

$$\begin{aligned}\text{SNR}_1 &= 1.76 + 6.02\,(N_{\rm ue} + 1.5N + 1) \\ &\quad + 30\,\log_{10}(\text{OSR}) - 5.17 \quad [\text{dB}]. \end{aligned} \tag{14}$$

Equations (13) and (14) express the impact on the achievable SNR by the number of bits $N_{\rm ue}$ of CADC. This effect of the error-estimation accuracy on the corrected DAC's performance

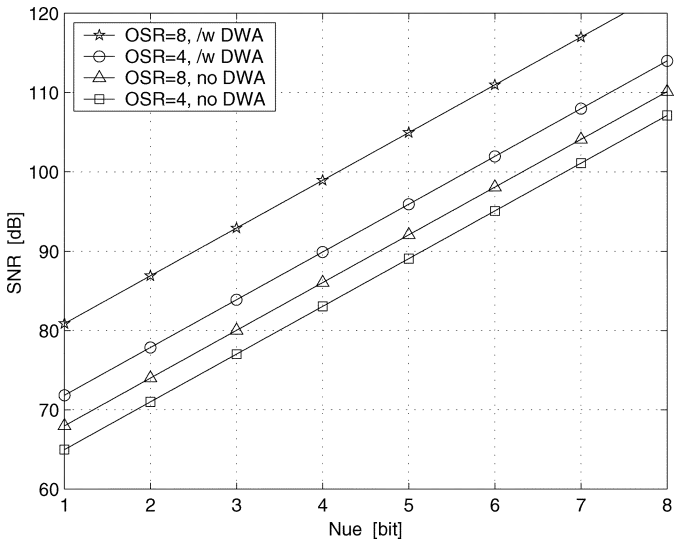

Fig. 4. Achievable SNR when limited by the estimation errors $\delta e_{\rm ue}$ (due to CADC with $N_{\rm ue}$ bits) of the unit-element errors $e_{\rm ue}$ only (ADAC with N of 5 bits).

is represented graphically on Fig. 4 for an OSR of 4 and 8, N of 5 bits, and for various resolutions of CADC.

As stated earlier, SNR_0 (or SNR_1) should exceed the truncation-error limited SNR obtainable with an ideal ADAC by at least 6 dB. When this occurs the overall corrected SNDR of a practical converter drops by about 1 dB from its ideal value and, consequently, Fig. 4 can serve as a guidance to choose the resolution for CADC.

For example, an EF DAC with N of 5 bits and OSR of 8 targets an overall 14 bits or 86.04 dB of SNR. Therefore, a SNR_0 (or SNR_1) in excess of 92.04 dB is recommended. This yields to a 5-bit CADC without DWA (from Fig. 4 and (13)) or a 3-bit CADC with DWA [from Fig. 4 and (14)]. This last result is very encouraging, since implementing a 3-bit CADC and a DWA algorithm require simple circuitry.

III. Design Examples

To support the effectiveness of the proposed nonlinearity correction, two low-OSR EF DACs were designed, simulated, built from discrete components, and measured.

The core of the EF DACs are the digital delta–sigma modulators. Its 24-bit input x_d is provided by a digital sinusoidal generator and its 5-bit output y_d is scrambled prior to being converted into an analog signal y_a by the 32-element ADAC [Fig. 5(a)]. Both modulators have a fourth-order 5-bit (32-element) architecture with optimized zeros [19] and obey the stability criterion of [13].

The first example[2] of EF DAC is capable of 62.5 dB of truncation-error limited SNR (10 bits) with an OSR of only 4. Its NTF has two complex-conjugate zero pairs optimally distributed over the signal band [19], namely, $\mathrm{NTF}(z) = 1 - 3.4888\,z^{-1} + 5.0089\,z^{-2} - 3.4888\,z^{-3} + z^{-4}$. The second example of EF DAC is designed for an OSR of 8. It can achieve 88.9 dB of truncation-error limited SNR (14.5 bits) with $\mathrm{NTF}(z) = 1 - 3.8689\,z^{-1} + 5.7399\,z^{-2} - 3.8689\,z^{-3} + z^{-4}$.

[2]The same EF DAC, but without the proposed correction, was presented in [13] to illustrate a stable high-order modulator.

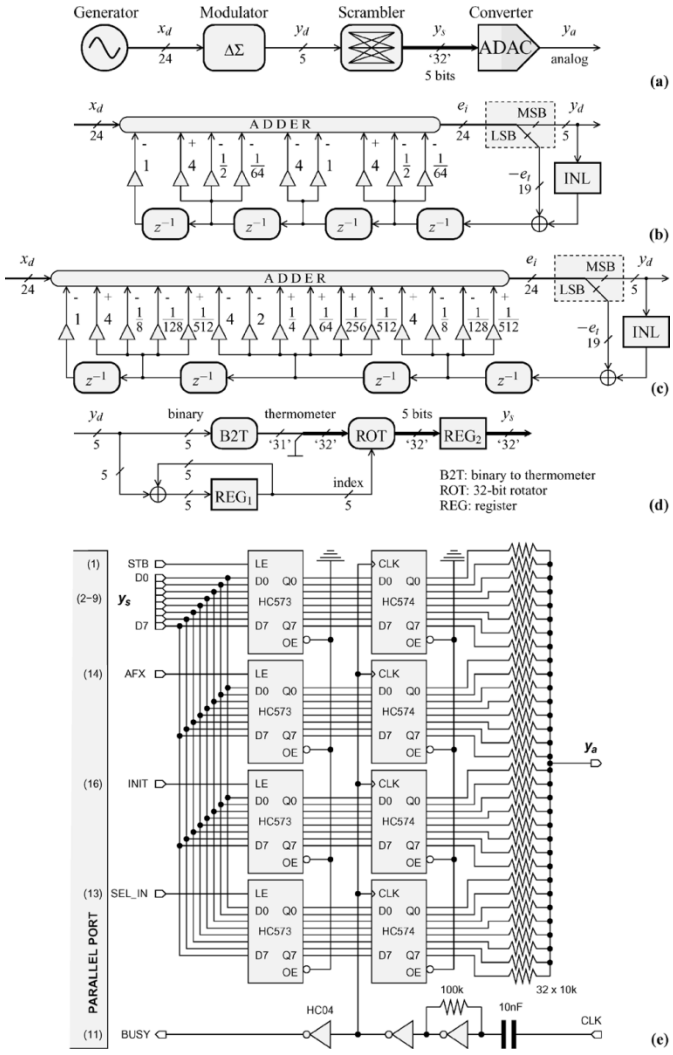

Fig. 5. Discrete-component experimental setup of two fourth-order 5-bit EF DACs . (a) Block diagram. (b) Digital EF modulator (OSR of 4). (c) Digital EF modulator (OSR of 8). (d) DWA scrambler. (e) 32-element resistive DAC interfaced to the PC's parallel port.

The digital modulator loops were coded in software using integer, 24-bit, arithmetic. Expensive multipliers can be avoided since the NTF's coefficients are easy to implement by shifting and adding/subtracting binary operations, i.e., $3.4888 \cong 4 - 1/2 - 1/64$ and $5.0089 \cong 4 + 1$ for an OSR of 4 (Fig. 5(b)), and $3.8689 \cong 4 - 1/8 - 1/128 + 1/512$ and $5.7399 \cong 4 + 2 - 1/4 - 1/64 - 1/256 + 1/512$ for an OSR of 8 [Fig. 5(c)]. These approximations give about 0.2 dB drop of SNR from its value achievable with floating-point coefficients.

The truncator is a mere splitting of bits. The five MSBs constitutes the modulator's output y_d, while the 19-LSB truncation error "$-e_t$" along with the correction term read from the RAM table are fed back into the loop filter $H(z)$ [Fig. 5(b)–(c)].

The discrete-component prototype is shown in Fig. 5(e) [13]. The digital logic (i.e., generator, modulator, and scrambler) was implemented using integer arithmetic on a x86 processor. The 32-line thermometer-coded digital output y_s was interfaced with

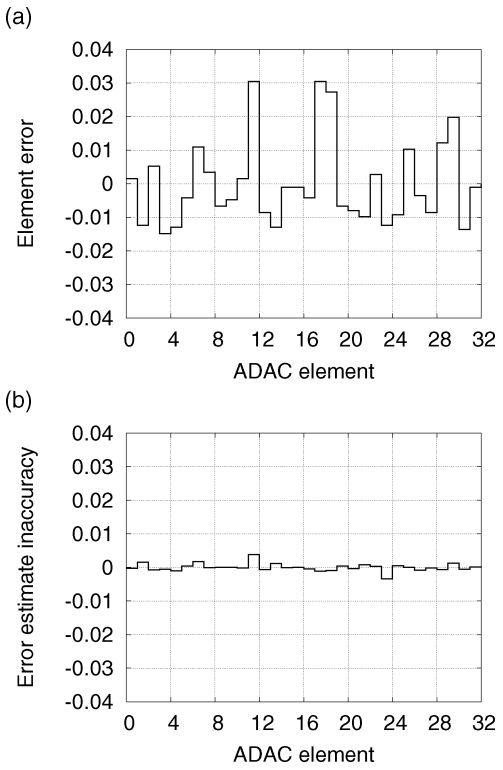

Fig. 6. 32-element ADAC. (a) Measured unit-element errors $e_{\rm ue}$. (b) Assumed error estimate inaccuracies $\delta e_{\rm ue}$. Both graphs show errors relative to the nominal element value ($\rm element\ value = 1$).

the 32-resistor ADAC using the parallel port of a personal computer (PC) and eight 8-bit buffers. The common node of the resistors provides the analog output y_a of the EF DAC. The timing of the circuit is controlled by an accurate external clock (CLK).

The discrete-component experimental setup mimics an integrated circuit (IC). Currently, the sampling rate of the DAC is limited to 64 kHz by the parallel port of the PC used in the experiment.

In all simulations and measurements, a nonlinear ADAC is used. This thermometer-code 5-bit ADAC uses CMOS registers and 32 identical resistors with 3% tolerance [Fig. 5(e)]. Each unit element was measured by a high-accuracy digital multimeter. The measured unit-element errors $e_{\rm ue}$ of the resistor-string ADAC are shown in Fig. 6(a). In order to take into account the potential inaccuracies in the nonlinearity-error estimates due to CADC, an intentional error $\delta e_{\rm ue}$ with a standard deviation $\sigma_{\rm ue}$ corresponding to a 3-bit CADC is included into simulations [Fig. 6(b)]. The same nonlinearities $e_{\rm ue}$, captured by measurements [Fig. 6(a)], are used in simulations to compare simulation results with experimental data.

The nonlinearity errors $e_{\rm nl}$ of the ADAC are corrected by the proposed digital correction (Fig. 2) enhanced by the first-order mismatch shaping offered by DWA [4]. The DWA scrambler rotates the thermometer-coded word using a barrel shifter [ROT in Fig. 5(d)]. A 5-bit register ($\rm REG_1$) holds the rotation index which is incremented by the output value of each sample y_d. Due to the circular nature of the rotator, the index adder truncates its output to 5 bits. The last register ($\rm REG_2$) of the scrambler avoids data-dependent delays in the signal path.

In the following subsections, simulation and experimental results are presented. During the measurements, the analog output signal y_a of the modulator was captured using a high-performance data acquisition card capable of handling audio-range signals with more than 105 dB of SNDR. The captured analog samples were post processed with a PC to obtain the SNDR and SNR values from the resulting spectra.

A. Simulated 10-bit DAC (OSR of 4)

Fig. 7 shows the simulation results for an OSR of 4. The spectrum shows some harmonic content and a high noise floor when no correction is used [Fig. 7(a)]. The effect of the ADAC mismatches is attenuated by 4.1 dB when the DWA algorithm is activated [Fig. 7(b)]. However, some spurious tones are present due to the tonal behavior of the first-order mismatch-shaping algorithm [20].

The results obtained using the proposed INL correction are shown in Fig. 7(c). With a 3-bit CADC, the resulting spectrum and SNDR of 62.0 dB is almost that of the ideal modulator, as expected from Fig. 4. The two notches of the NTF are clearly visible. A second harmonic is still present, but its power is well below the noise floor of the truncation error. The obtained SNDR of 62.0 dB is almost that of the ideal modulator.

Finally, the results obtained by using the INL correction combined with the DWA algorithm are shown in Fig. 7(d). The harmonic distortion is no longer visible and the two NTF notches are deeper than those of Fig. 7(c). However, the achieved SNDR improvement of 0.4 dB is not significant.

B. Simulated 14-bit DAC (OSR of 8)

The simulation results for an OSR of 8 are presented in Fig. 8. To clearly identify the dominant error components in the spectra, (4) was reproduced and visually confirmed by simulations in Fig. 8(e) and (f) for the INL correction [Fig. 8(c)] and for the INL correction with DWA [Fig. 8(d)] scenarios, respectively.

Fig. 8(a) shows the spectrum obtained when no correction is used. The high noise floor lowers the SNDR value to 61.0 dB, that is, 27.9 dB below that of an ideal modulator. Thus, 4.3 effective bits are lost due to the nonlinearity of the ADAC.

The spectrum obtained using the DWA algorithm is shown in Fig. 8(b). In this case, the noise floor shows the expected frequency dependence related to the first-order shaping of the DWA algorithm. However, the noise and distortion are still too high to achieve a performance close to that of an ideal modulator. This causes a loss of 2.4 effective bits. This result confirms that first-order mismatch shaping is not effective enough at such a low OSR.

The results obtained using the INL correction method are shown in Fig. 8(c). With a 3-bit CADC the resulting spectrum shows a flat noise floor and a second harmonic caused by the inaccuracies $\delta e_{\rm nl}$ affecting the nonlinearity error's estimate $\hat{e}_{\rm nl}$ used in the correction [Fig. 8(e)]. The distortion introduced by the second harmonic lowers the SNDR value to 74.0 dB while the SNR is 81.5 dB. This result is comparable with that achieved with the DWA [Fig. 8(b)].

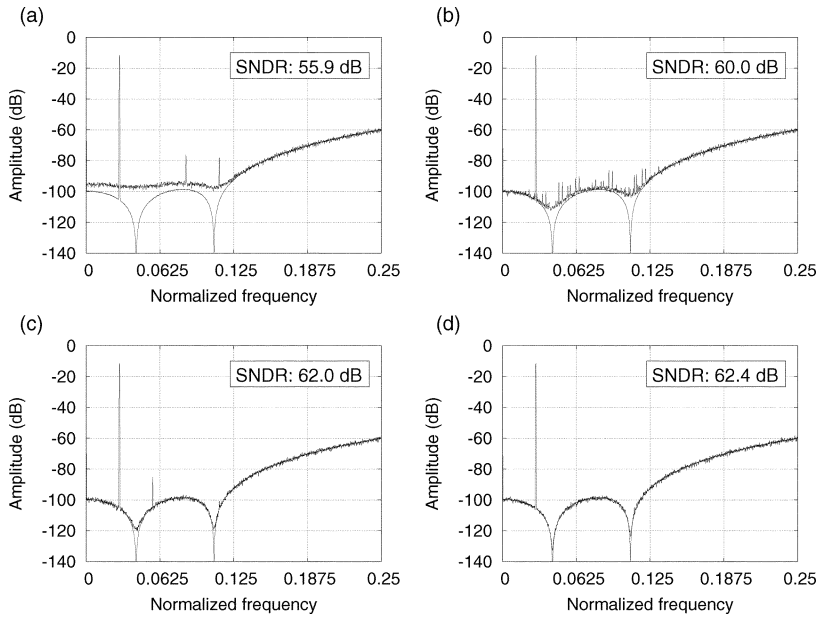

Fig. 7. Simulated spectra for an OSR of 4 and a 3-bit CADC (FFT length of 65 536 samples). (a) Without any correction. (b) With DWA algorithm. (c) With INL correction. (d) Combined INL correction with DWA. In each case, the spectrum of an ideal modulator (SNR of 62.5 dB) is included for comparison.

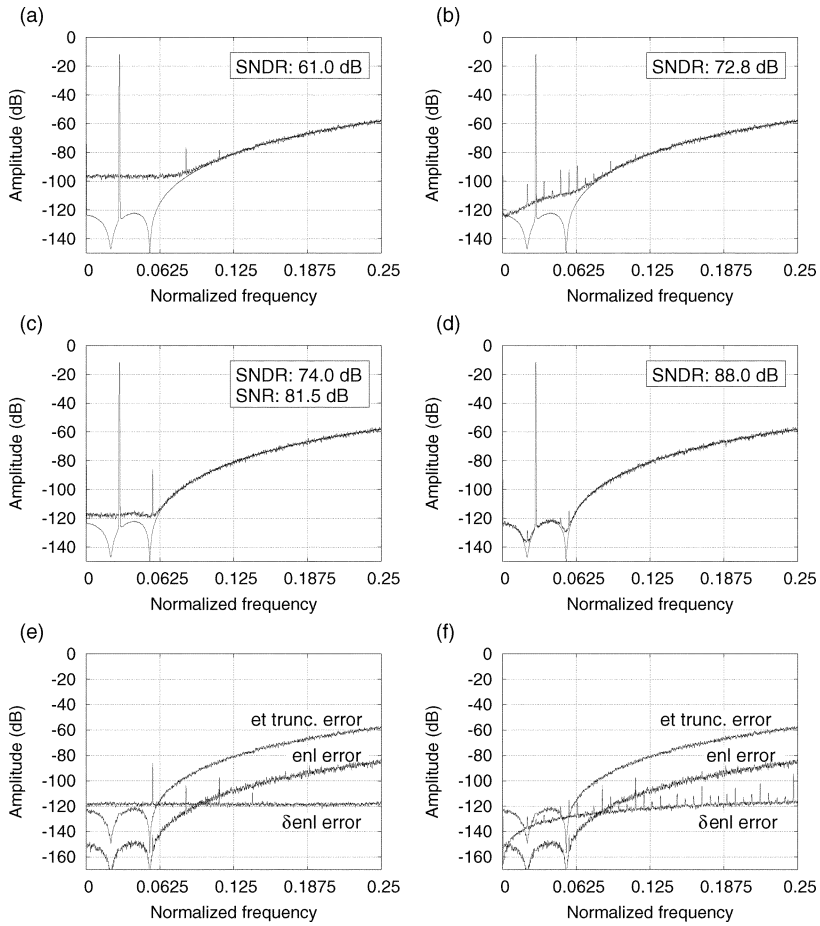

Fig. 8. Simulated spectra for an OSR of 8 and a 3-bit CADC (FFT length of 65 536 samples). (a) Without any correction. (b) With DWA algorithm. (c) With INL correction. (d) Combined INL correction with DWA. (e) With INL correction: error components. (f) Combined INL correction with DWA: error components. In each case, the spectrum of an ideal modulator (SNR of 88.9 dB) is included for comparison.

Note that (13) and Fig. 4 predicted an SNR of 80.0 dB for this scenario, which is pretty similar with the simulated 81.5-dB value. Since the calculations of Section II-C assumed white power-spectral density for the error components, the SNDR

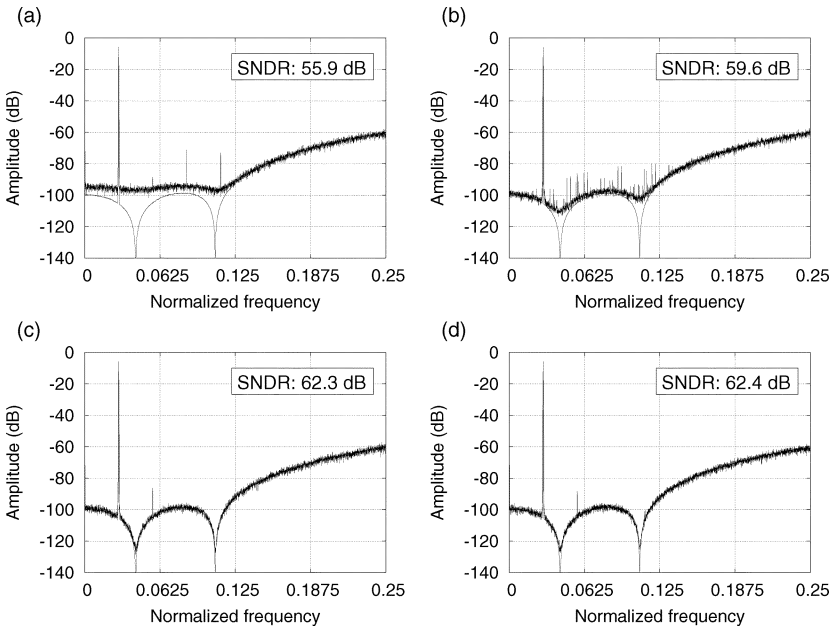

Fig. 9. Measured spectra for an OSR of 4 (FFT length of 65 536 samples). (a) Without any correction. (b) with DWA algorithm. (c) With INL correction. (d) Combined INL correction with DWA. In each case, the spectrum of an ideal modulator (SNR of 62.5 dB) is included for comparison.

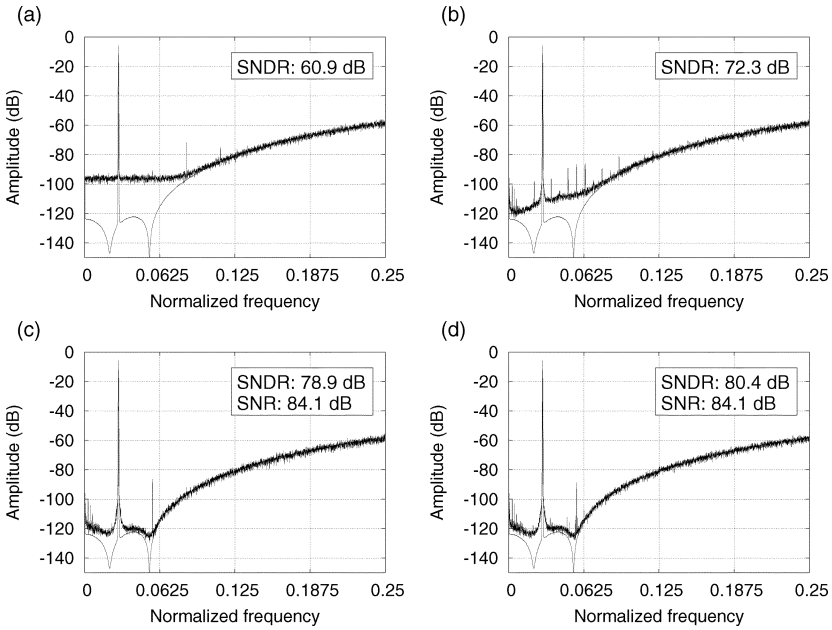

Fig. 10. Measured spectra for an OSR of 8 (FFT length of 65 536 samples). (a) Without any correction. (b) With DWA algorithm. (c) With INL correction. (d) Combined INL correction with DWA. In each case, the spectrum of an ideal modulator (SNR of 88.9 dB) is included for comparison.

of 74.0 dB could not be predicted. However, when the ADAC elements are scrambled, the spectrum gets whitened and the predictions become more reliable.

Finally, the results obtained by using the INL correction combined with the DWA algorithm are shown in Fig. 8(d) and (f). The resulting spectrum is close to that of the ideal modulator even for a 3-bit CADC. The SNDR loss from the ideal value is 0.9 dB, as predicted exactly by (14) and Fig. 4.

C. Measured 10-bit DAC (OSR of 4)

The experimental results obtained for an OSR of 4 are shown in Fig. 9. These spectra are in good agreement with the simulated results (Fig. 7). With respect to Fig. 9(c), the experimental spectrum is closer to the ideal than the simulated one [Fig. 7(c)], since the experimental estimates $\hat{e}_{\rm nl}$ are not disturbed by the random inaccuracies $\delta e_{\rm nl}$. When INL correction is combined with the DWA algorithm, the experimental spectrum [Fig. 9(d)] still shows a small second-harmonic distortion, but this does not degrade the SNDR value of 62.4 dB which is 0.1 dB less than that of an ideal modulator.

D. Measured 14-bit DAC (OSR of 8)

The results obtained for an OSR of 8 are presented in Fig. 10. Due to the expected high resolution of this converter the effects

of analog-circuit imperfections of the experimental setup become visible and dominant in some spectra.

First, the low-frequency spurious tones visible in Fig. 10(b)–(d) are due to 60-Hz power-source interference that was difficult to attenuate. Second, the signal tone exhibits some skirts due to the jitter of the clock-signal generator in Fig. 10(c)–(d). Also, clock jitter spreads the in-band noise and it could be responsible for the higher than expected noise floor of Fig. 10(c)–(d) compared to the simulated case of Fig. 8(c)–(d).

Finally, the mismatch between the on-resistance of the nMOS and pMOS devices of the CMOS HC574 output buffers [Fig. 5(e)] introduces a systematic error in the RAM table which cannot be taken into account by the digital correction. This mismatch error generates even-order harmonic distortion and an increased in-band noise floor. Both effects are present in the experimental spectra. When 38- and 25-Ω output resistance is used for pMOS and nMOS devices, respectively, simulations can reproduce this effect. However, when an integrated-IC scenario chooses the popular current-steering architecture instead of the voltage-driven architecture of the experimental setup, then this systematic error will disappear.

Despite these experimental-setup problems, the EF DAC using the INL correction combined with DWA provides 84.1 dB of SNR and 80.4 dB of SNDR using an OSR of 8. As simulations demonstrated earlier in Section III.B, this fourth-order 5-bit EF DAC potentially can achieve 14 effective bits of resolution for an OSR of 8.

IV. Conclusion

This paper presents an efficient architecture to achieve high-resolution DACs at low OSRs , i.e, for wide-band applications such as digital subscriber lines. It proposes a high-order multibit EF DAC with improved stability and with digital correction enhanced by DWA. The unit elements of the DAC are measured by a low-resolution CADC and stored in a RAM table. These values are then used to compensate for the multibit DAC's distortion by a simple digital addition. A fourth-order 5-bit EF DAC is designed, modeled and extensively simulated. Also, a prototype is built from discrete components and measured. The correction uses simple digital circuitry and a 3-bit CADC enhanced by DWA. Simulation and experimental results show a 14-bit DAC operating at an OSR of 8. At such a low OSR, using DWA alone leads to a resolution of less than 12 bits.

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