Low-Power Pipelined ADC Design for Wireless LANs

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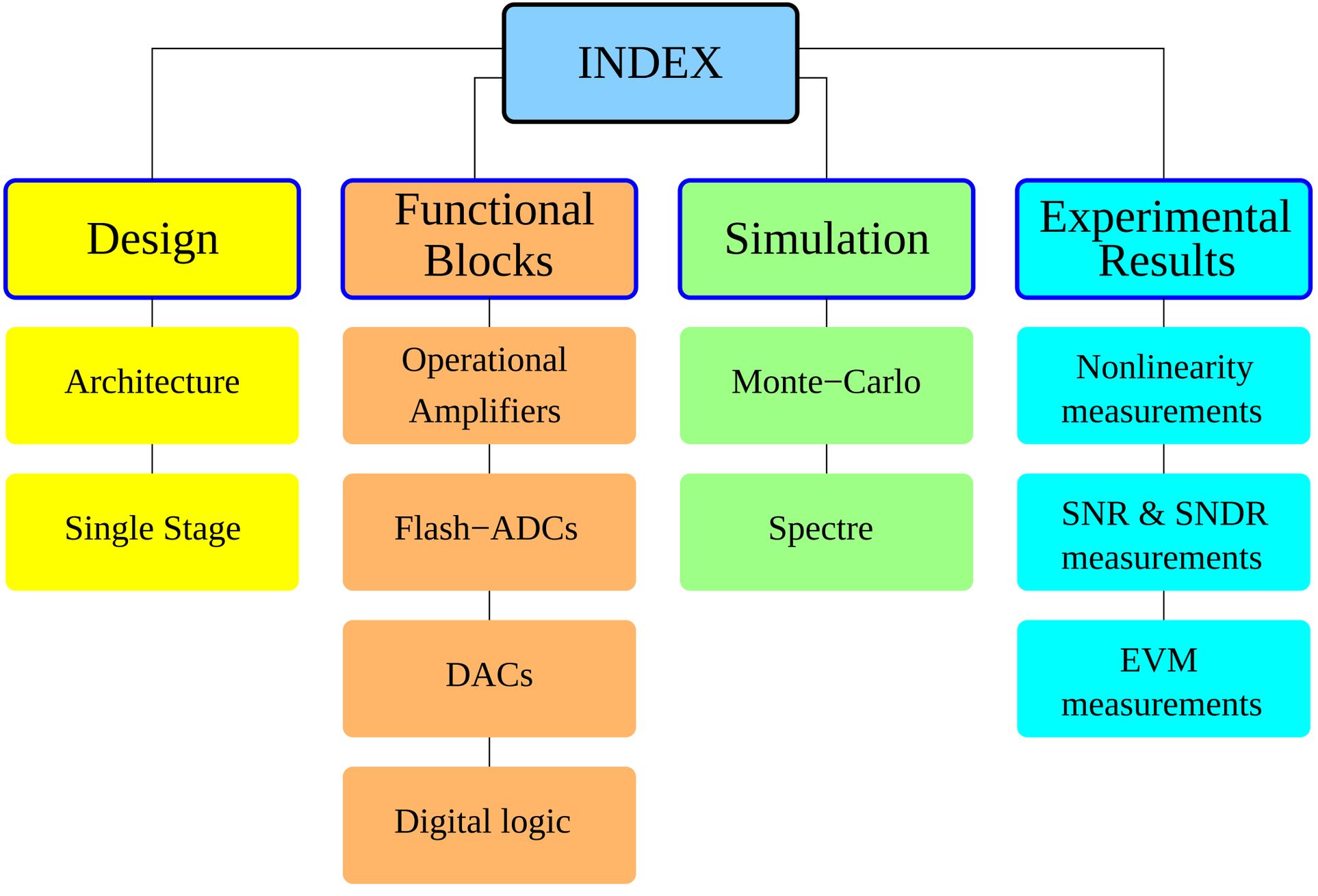
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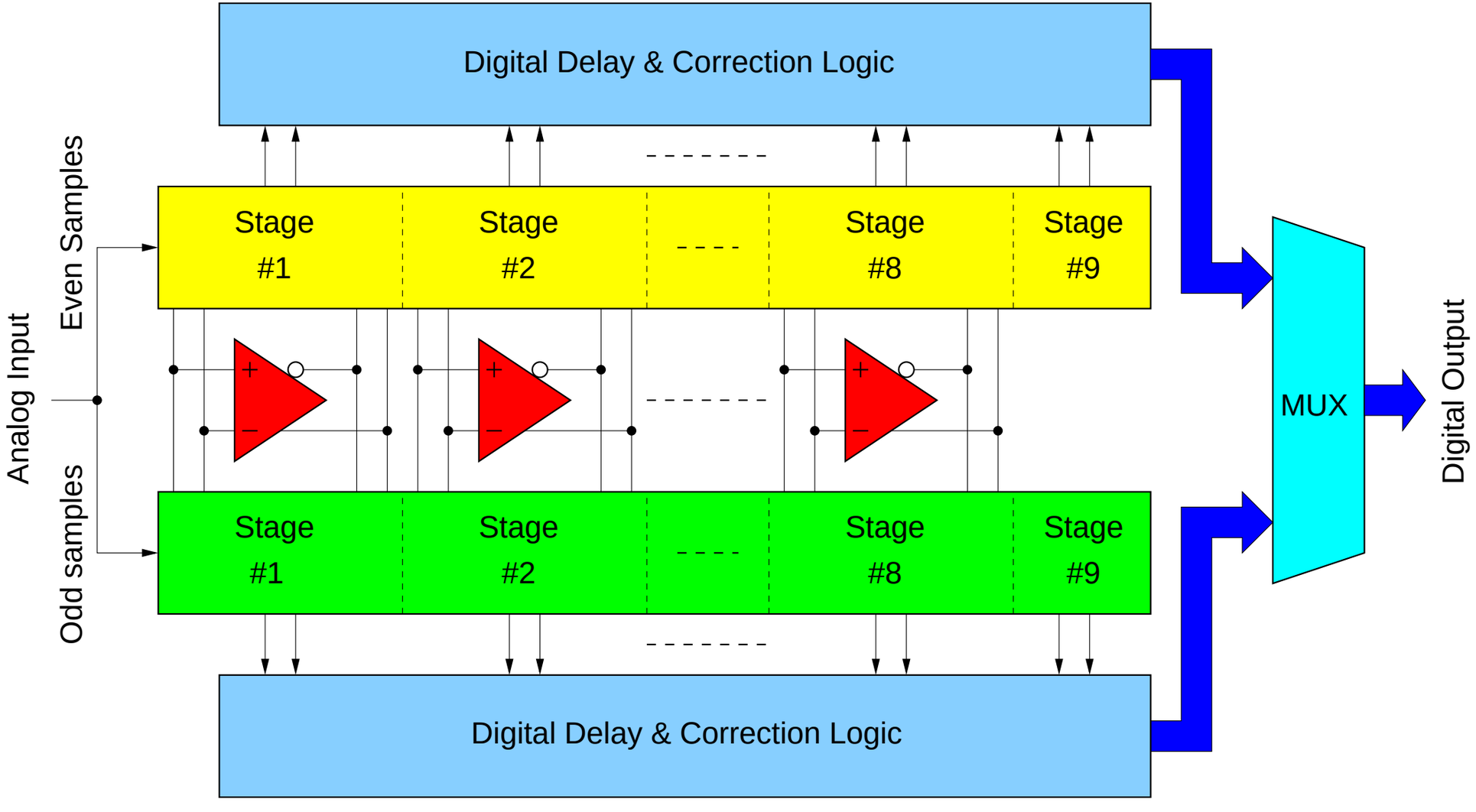
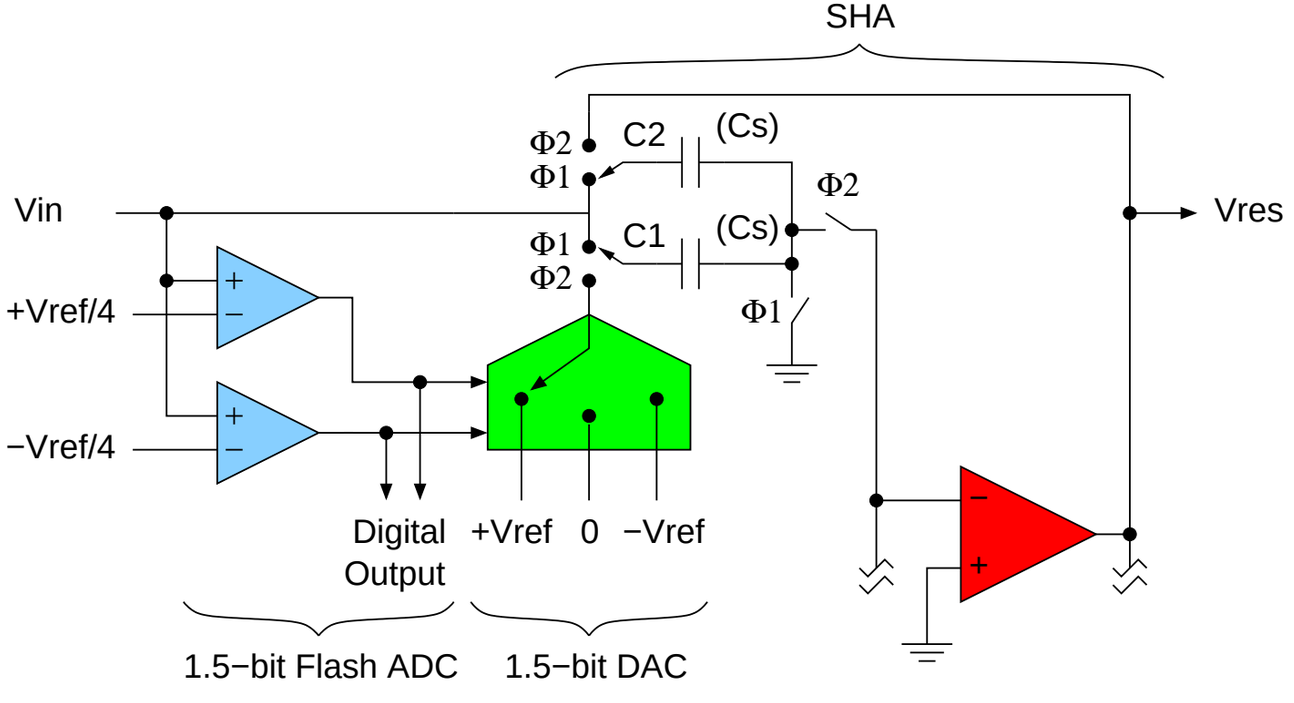
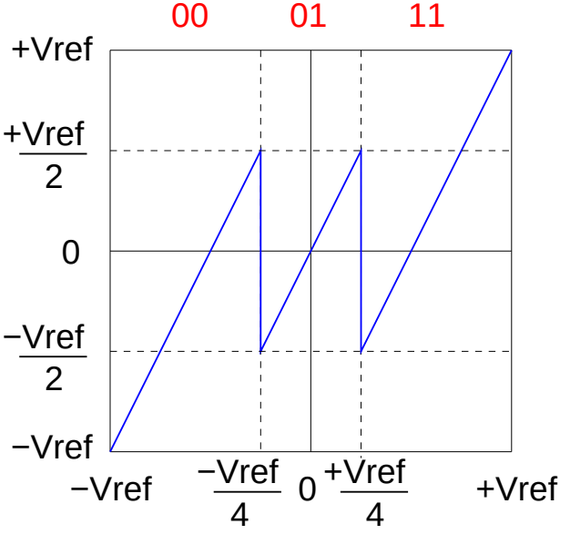
Block Diagram of the ADC



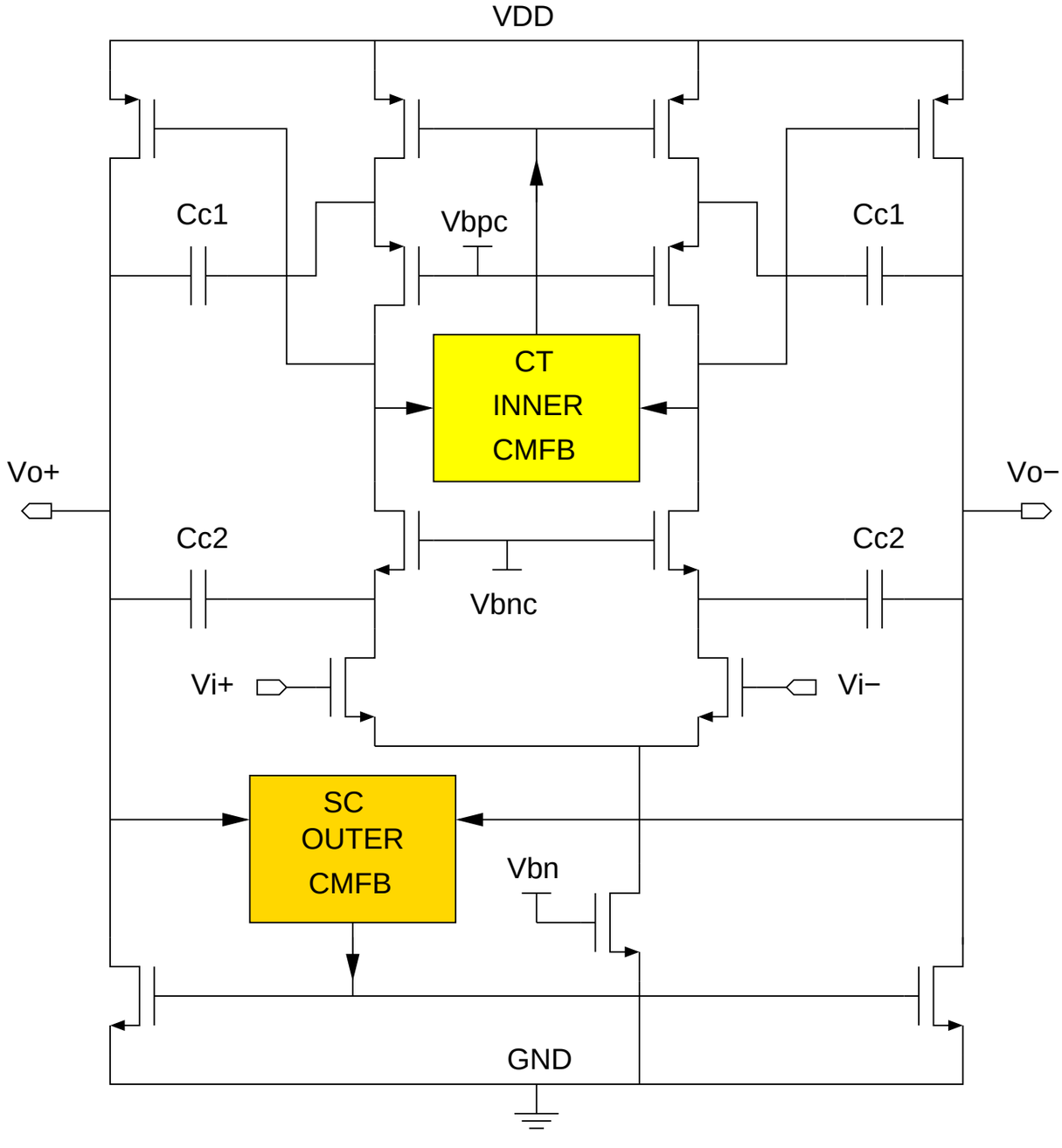
Simplified Pipeline Stage



Transfer function



Operational Amplifiers



First stage is a telescopic cascode:

− Large DC gain:
  · Short−channel devices are OK
    · Low Parasitics
− 2 cascode nodes available for compensation:
  · Split Compensation Capacitors give more Gain−Bandwidth or Phase−Margin

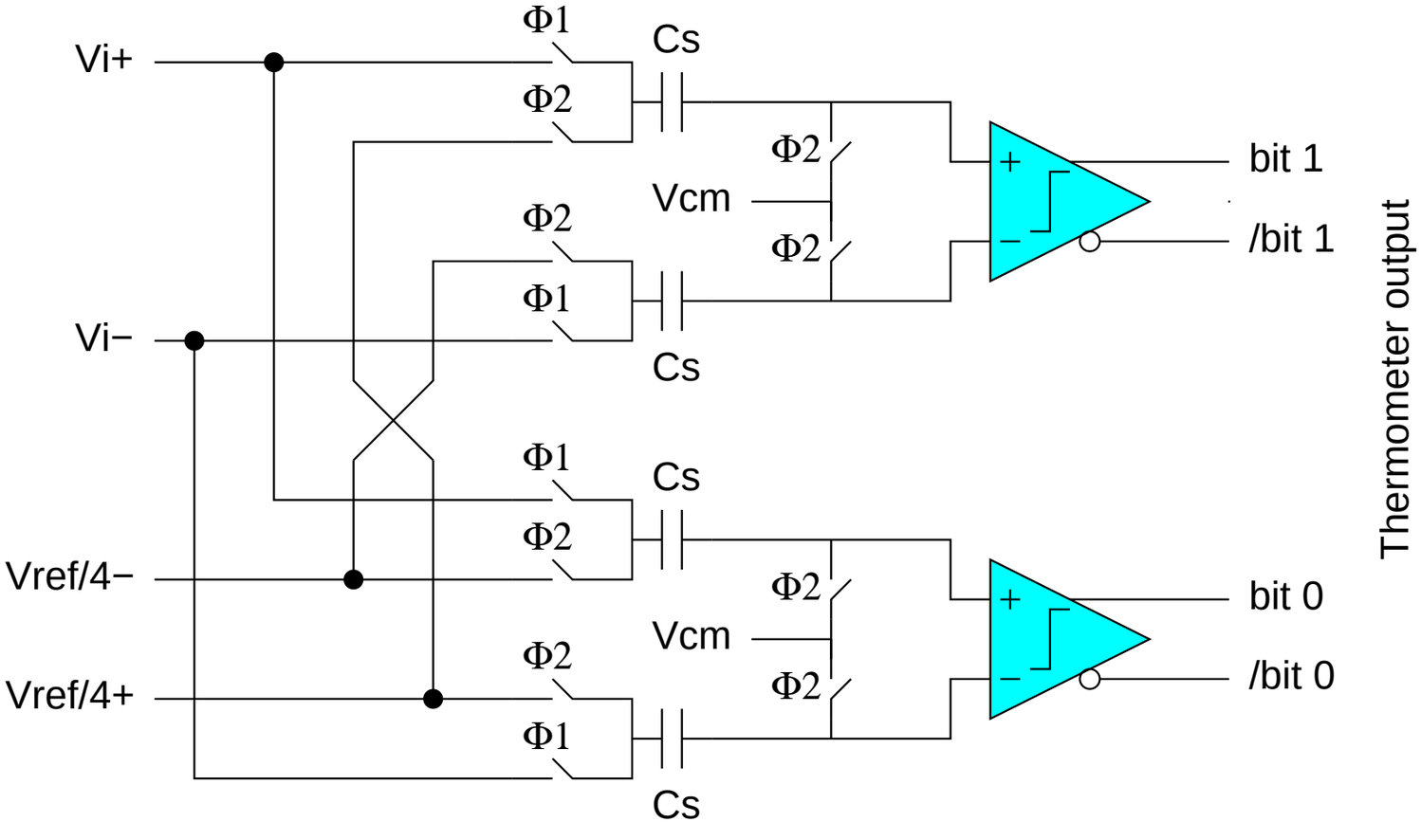
Two Common−Mode−Feedback loops:

− Good stability
− Outer loop is a SC circuit due to linearity requirements.

Main Specs:

− Slew rate: 166 V/μs
− Gain−Bandwidth: 200 MHz

1.5−Bit, Flash, sub−ADC



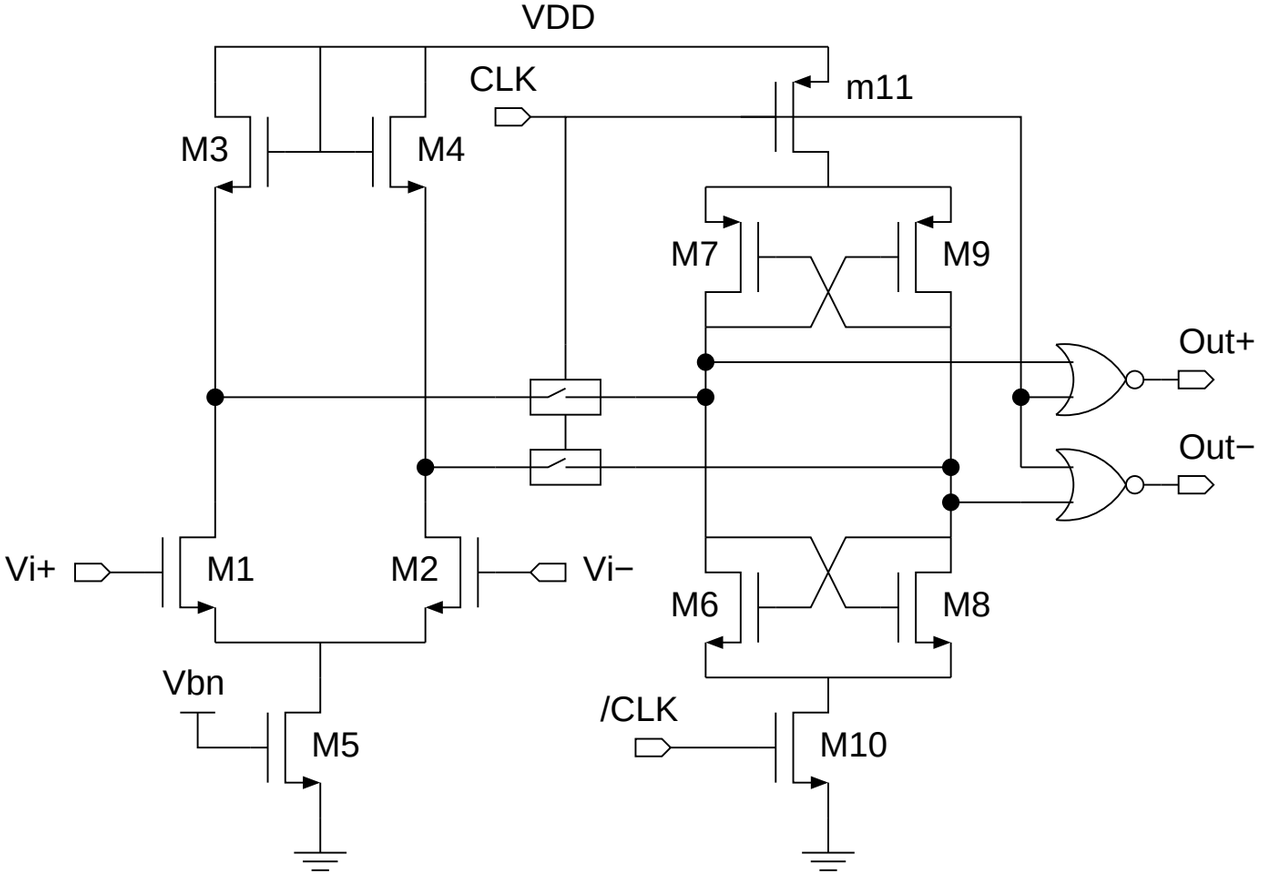
− No charge pumping. Low Power

− Sensitive to charge injection from switches, but:

  · Charge injection generate offsets

  · Offsets are removed through digital correction

Comparator



Low−gain Preamplifier

- Isolates input from kick−back noise
- fast settling

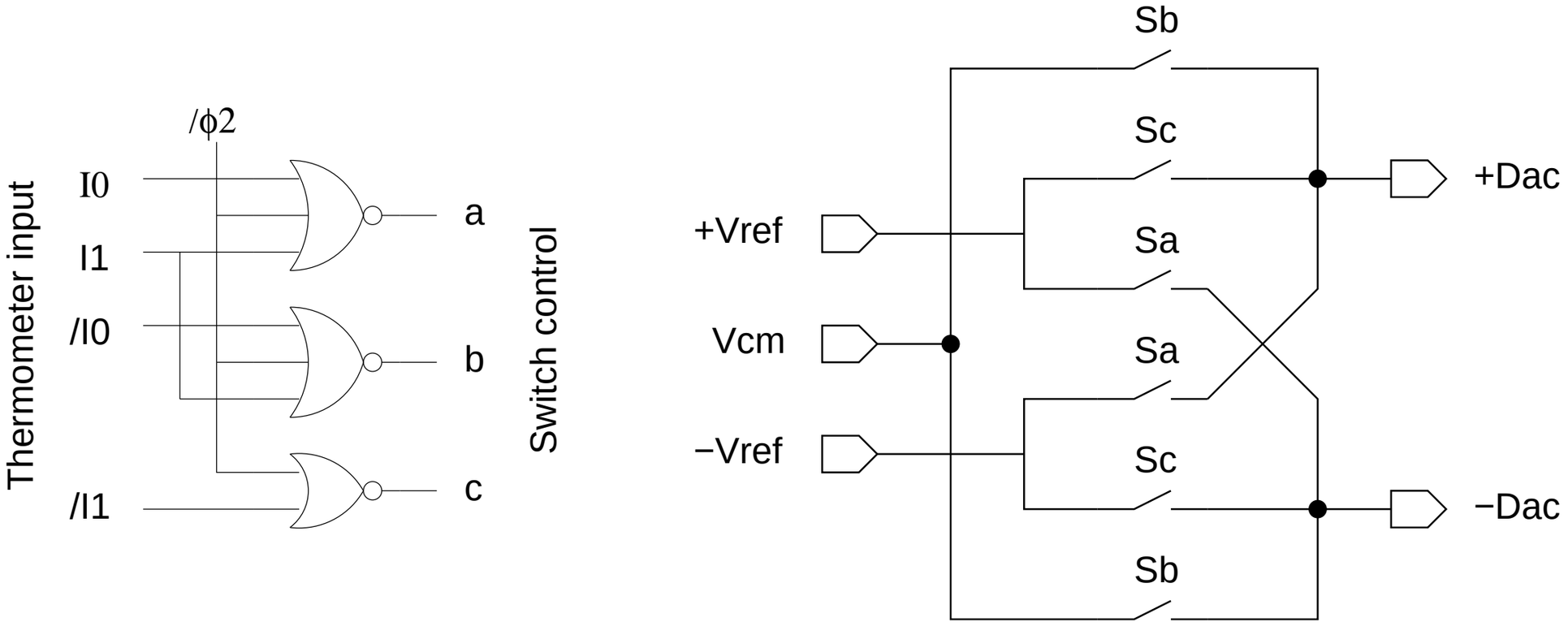
Full−Swing Latch

- Fast regeneration. No metastability
- Rail−to−rail output

Clocked output

- Avoids non−CMOS levels

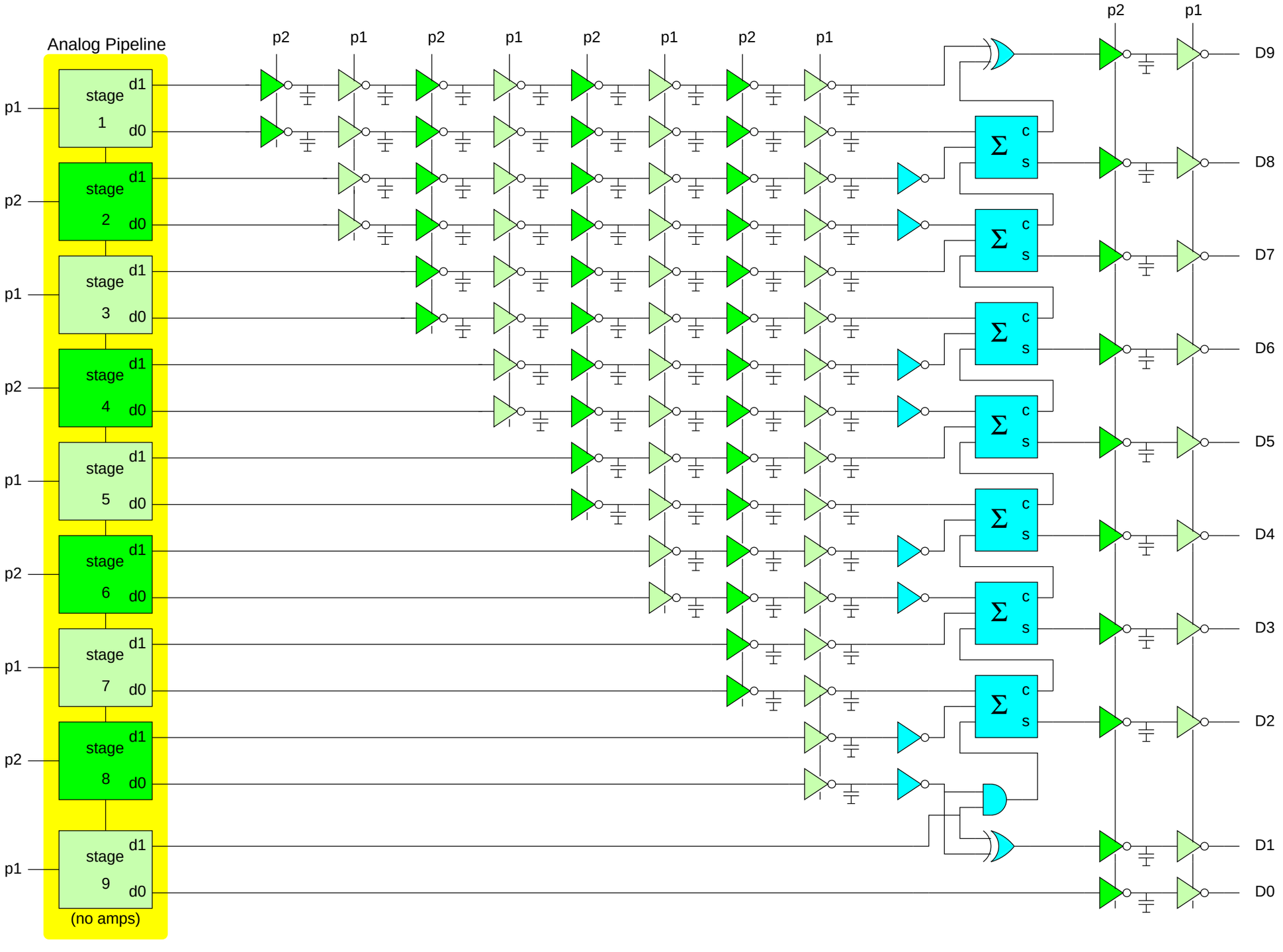
1.5−Bit sub−DAC



− High impedance output during phase 1. This saves 2 series−switches in the S&H circuit

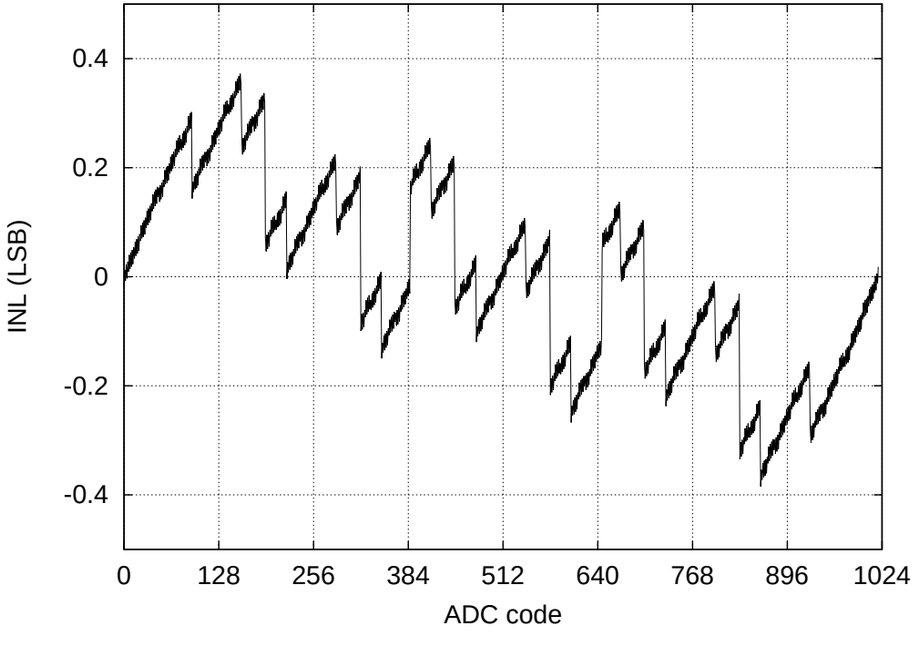
− High linearity thanks to wire−crossing inversion

Digital Delay and Correction Circuit

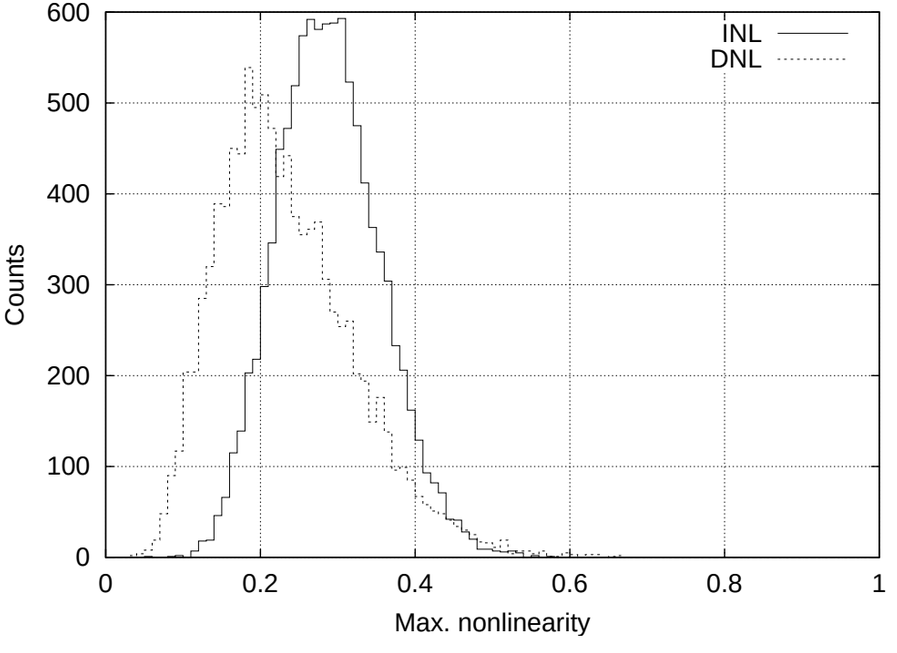


System−level Simulation

Single INL run



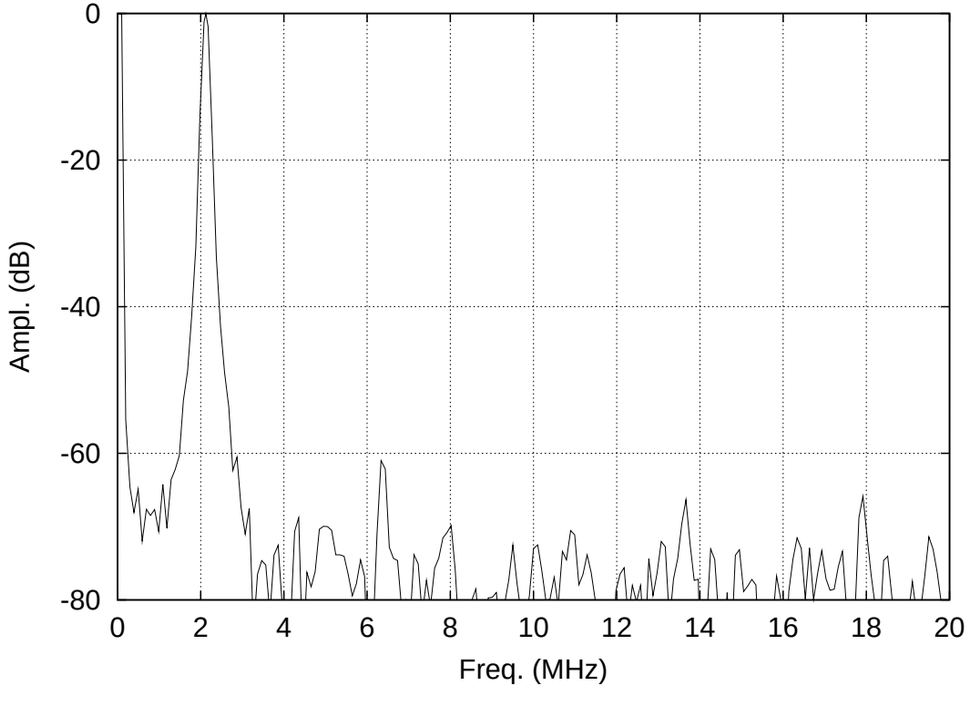
Monte−Carlo



Effects simulated:

− Capacitor mismatch
− Comparator offset
− Finite opamp gain
− Digital correction logic.

Transistor−level Simulation (Spectre)

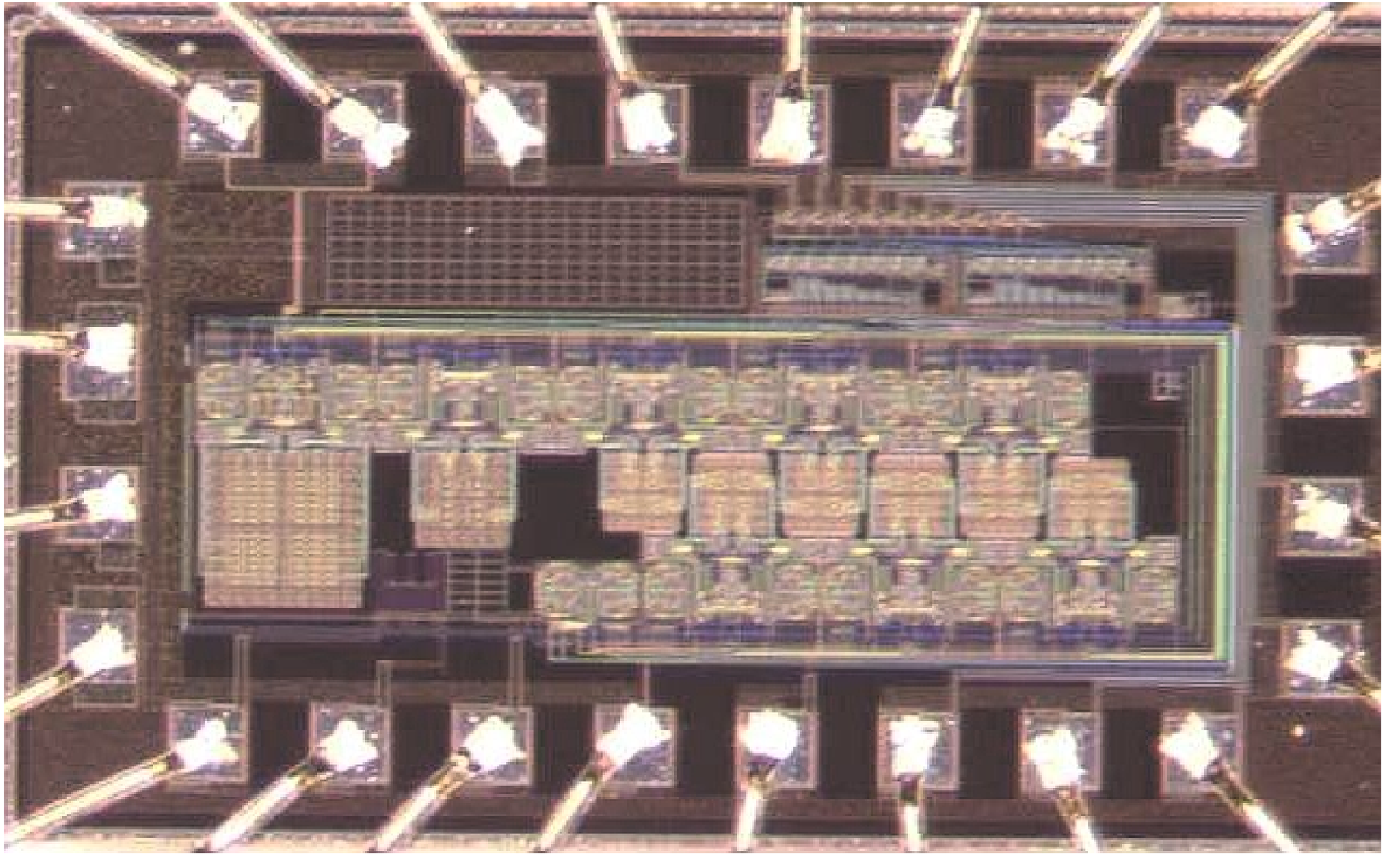


- Simulated from extracted circuit
- Distortion < −60 dB
- Power: 11.5 mW
  - Analog: 9.75 mW
  - Digital: 1.75 mW

Effects not included:

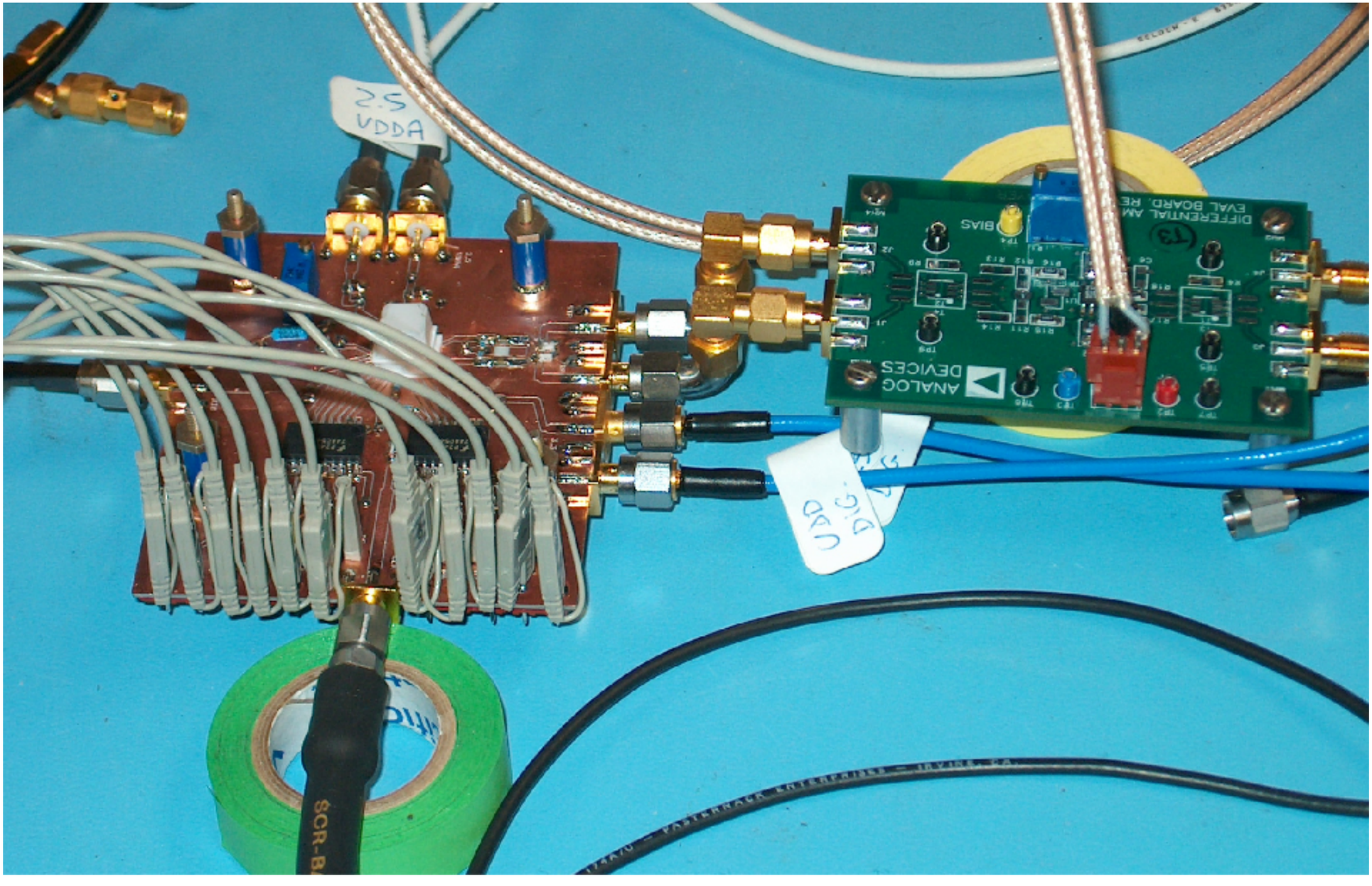
- Mismatch
- Circuit noise

Chip photograph

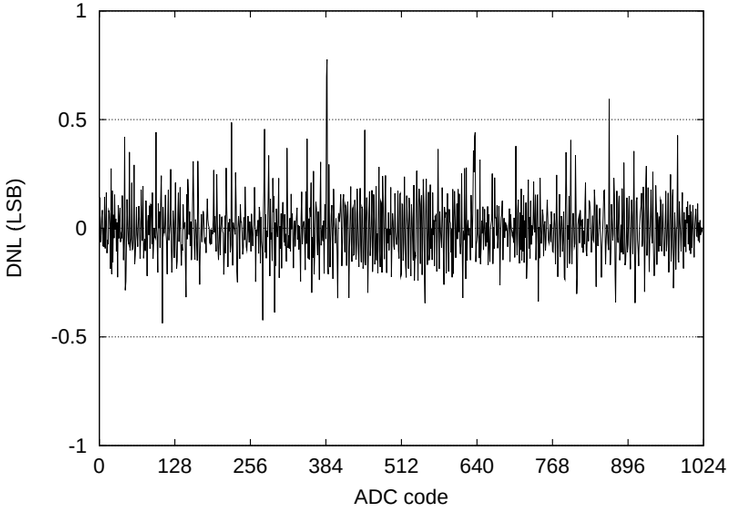


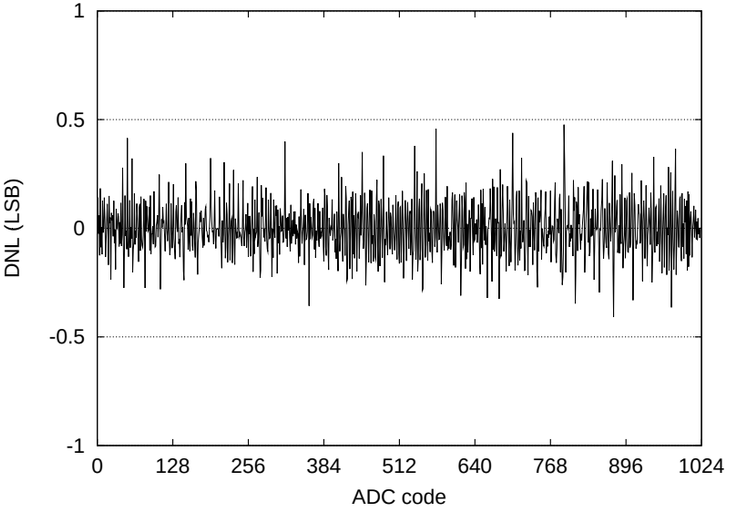
Area: 1500 x 880 μm^2, including pads.

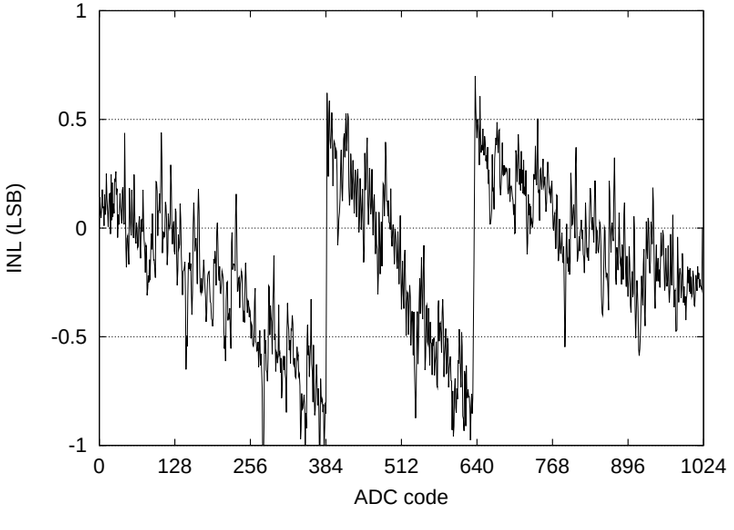
Measurements

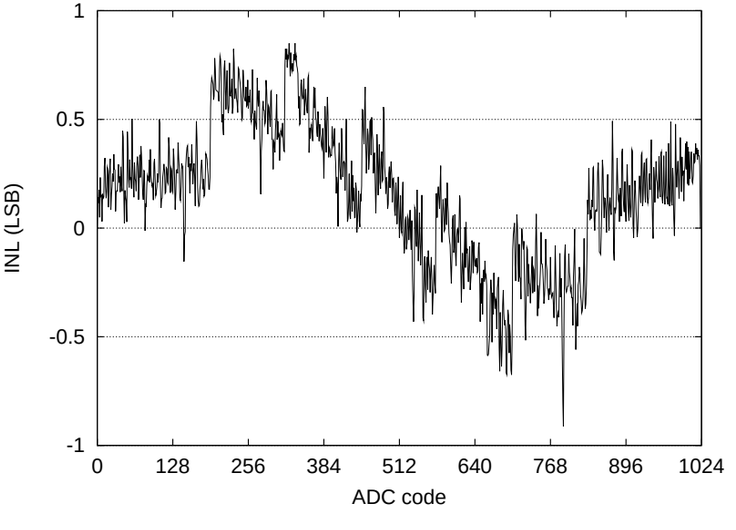


Measured Nonlinearity Graphs



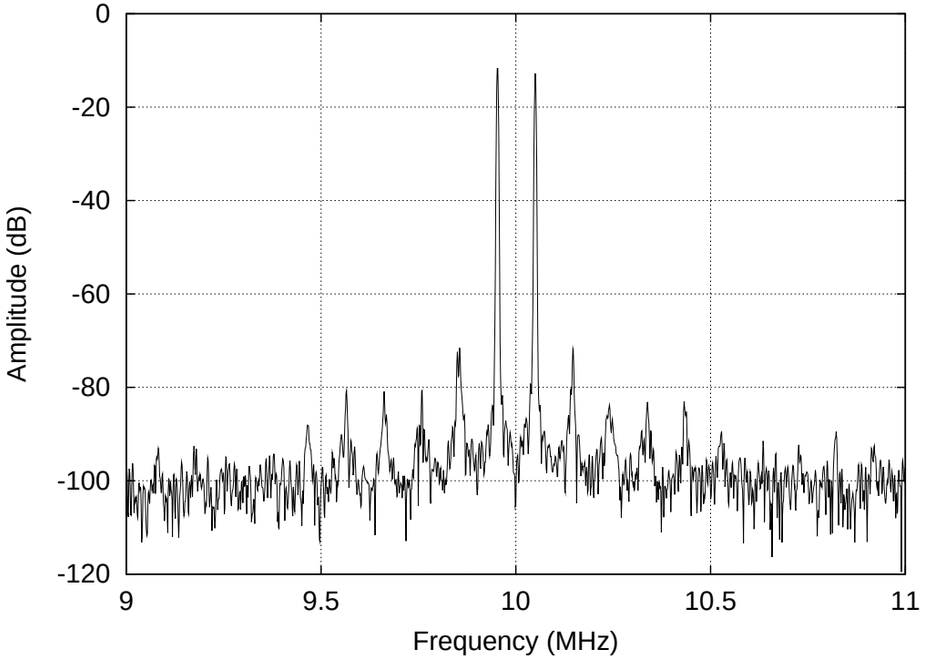


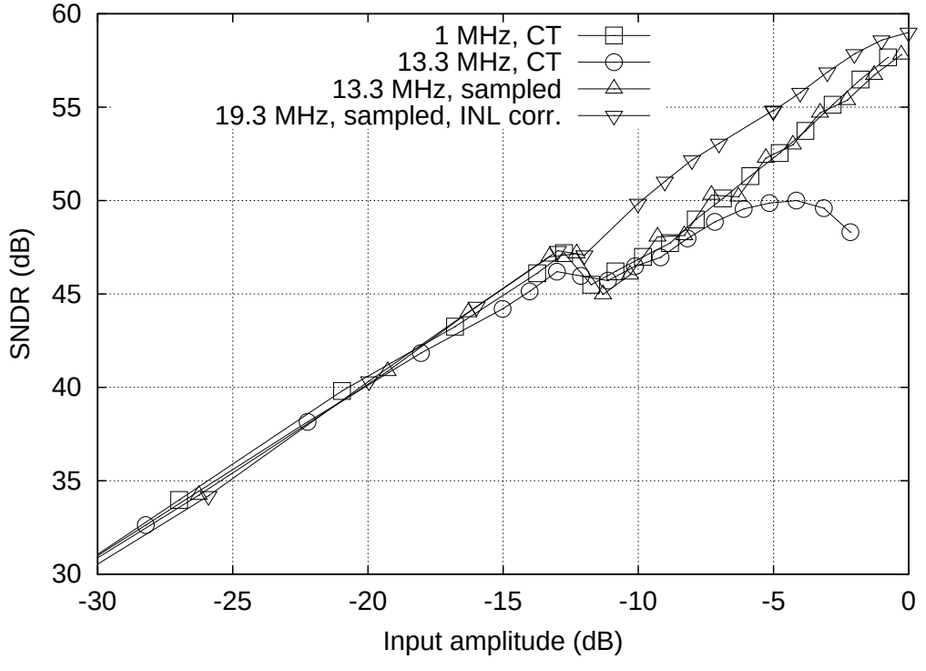




- Code density measurement with sinusoidal input.

Frequency-domain measurements

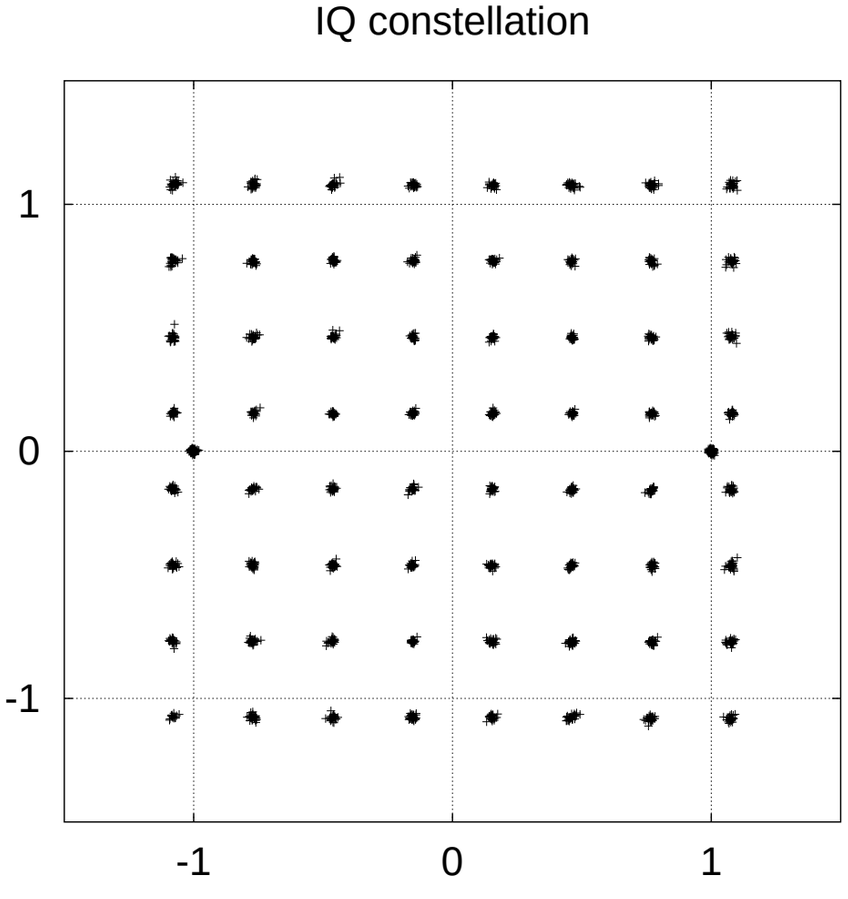


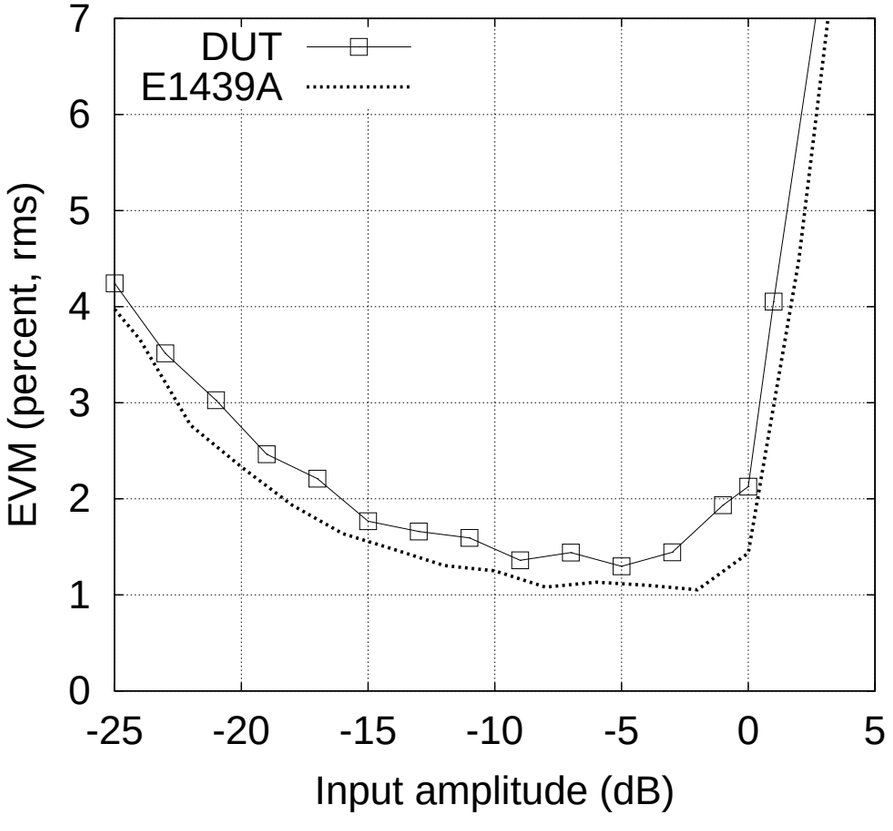


- Single and two-tone tests

- Continuous time and sampled sinusoids.

EVM measurements with real OFDM signals





- 54-Mbit/s OFDM signal (IEEE 802.11a/g). 10 MHz carrier.

- Agilent’s EVM test equipment & software.

Performance summary

Resolution	10 bits
Sampling Rate	40 MHz
Power consumption	ADC: 11.7 mW
	Pin drivers: 1.3 mW ($C_L \approx 4.5$ pF)
Technology	2.5-V, 0.25-μm, CMOS (MOM cap.)
Chip Area (w. pads)	1.5×0.88 mm^2
(wo. pads)	1.2×0.58 mm^2
Nonlinearity (max)	DNL: 0.77 LSB
	INL: 1.15 LSB
SNR	61.3 dB
SNDR	57.6 dB
ENOB	9.3 bit

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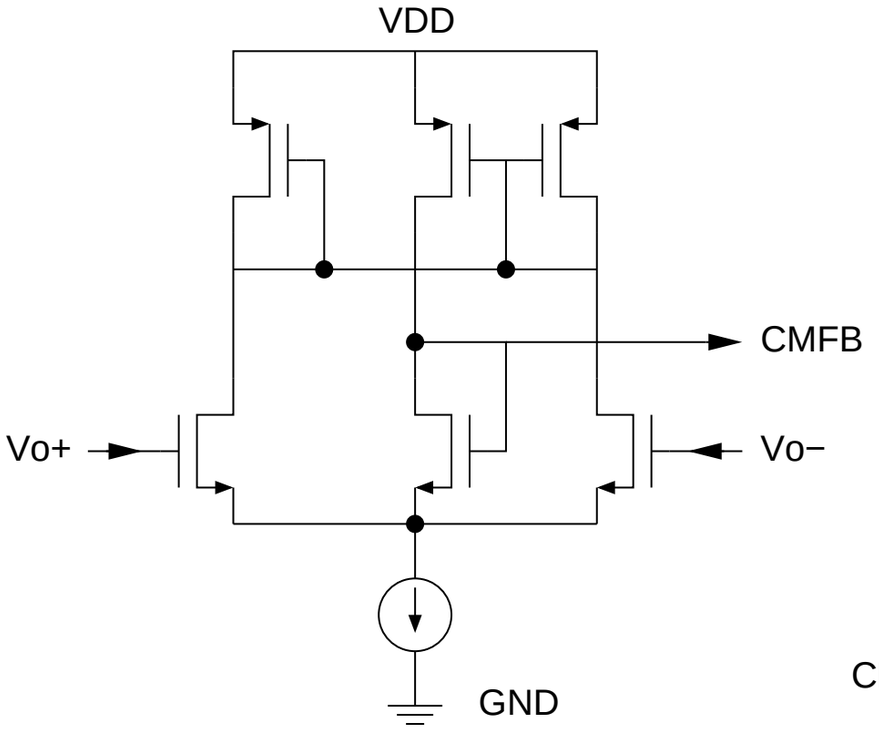
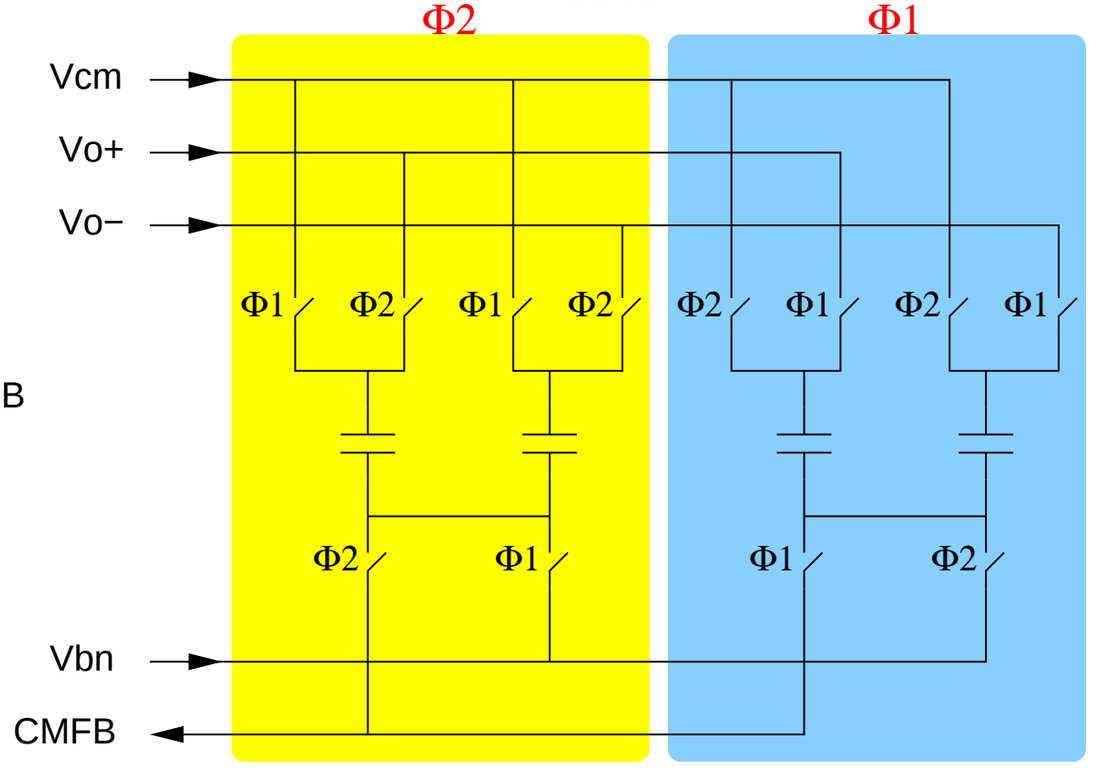
Operational Amplifiers

Inner CMFB Circuit



- Continuous−time
- Diff. pair + level shifter
- Small differential−input range

Outer CMFB Circuit



- Discrete−time
- Highly linear. Large input range
- Two circuits operate on alternate clock phases

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(wo. pads)	1.2 $\times$ 0.58 mm^2
Nonlinearity	DNL: 0.77 LSB
	INL: 1.15 LSB
SNR (max)	61.3 dB @ 10.6 MHz
SNDR (max)	57.6 dB @ 1 MHz
	57.8 dB @ 19.3 MHz†
	59.0 dB @ 19.3 MHz††
ENOB (max)	9.3 bit @ 1 MHz
	9.3 bit @ 19.3 MHz†
	9.6 bit @ 19.3 MHz††

Notes:

† Sampled input.

†† Sampled input and static INL correction.

OFDM modulation

⇨ Large number of subcarriers per channel.

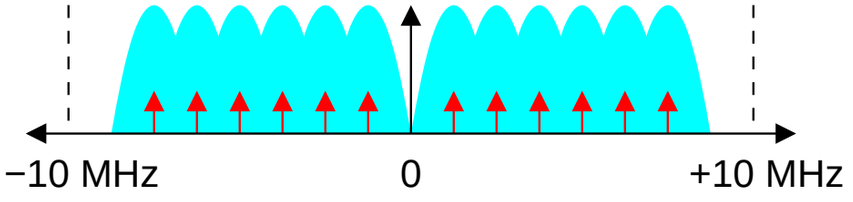
⇨ Orthogonality = No interference bw. subcarriers.

$$\int_0^{T_s} A_i \cos(\omega_i t + \varphi_i) \times A_j \cos(\omega_j t + \varphi_j)\, dt = 0$$

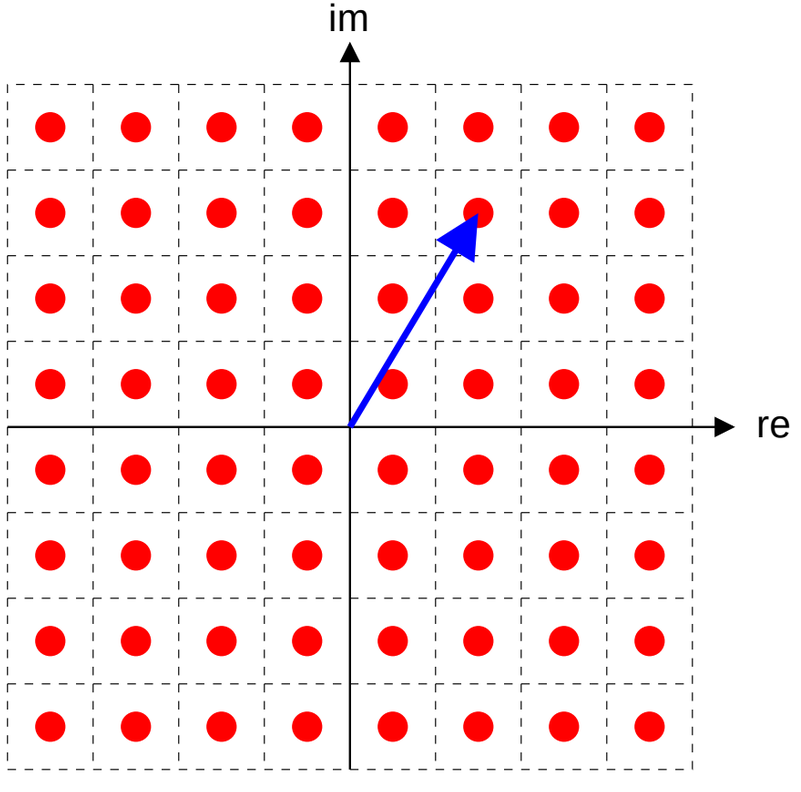
⇨ OFDM modulation and demodulation are done via Fast Fourier Transforms (FFT).

OFDM (standard IEEE 802.11a/g)

OFDM channel spectrum



64−QAM subcarrier



- 64 sub−carriers, but
  - − No DC carrier (f=0 Hz)
  - − No carriers close to adjadcent channels
- 54 used subcarriers.
- 48 carriers for data.

- Subcarrier modulation: QAM
- QAM constellations:

  64 (54 mb/s), 16 or 4 points.