Low-Power Pipelined ADC Design for Wireless LANs

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***Abstract*— In this paper a 10-bit, 40-Msample/sec analog-to-digital converter (ADC) is presented. A power consumption of 12 mW was achieved by using time-interleaved and pipelined architecture with shared operational amplifiers. This circuit was designed for a 2.5-V 0.25-μm technology with metal-oxide-metal capacitors. The proposed design can be a solution for high-speed, low-power applications like portable wireless-LAN cards.**

***Index Terms*— Low-power, data converter, pipeline ADC.**

I. Introduction

The new generation of wireless-LAN adapters based on the IEEE 802.11a standard [1] imposes a significant challenge to circuit designers. The wide signal bandwidth demands a high sampling rate for ADCs and DACs, however, the power consumption must be kept low in order to extend the battery life of portable wireless devices. The ADC specifications depend on the receiver architecture. For direct-conversion receivers two 20 Msample/sec ADCs are needed, while, for low-IF receivers only one 40 Msample/sec ADC might be sufficient. The OFDM modulation used in the IEEE 802.11a standard [1] also demands a high resolution for these converters. At least 10 bits are needed in typical receiver designs in order to avoid an increased bit error rate due to ADC's quantization errors.

The power consumption of state-of-the-art ADCs is on the order of 50 to 100 mW [2–5]. This is a significant portion of the total receiver power. One should also take into account that the receiver is active during periods much longer than the transmitter for client devices, so the total transceiver power is directly affected by the choice of the ADC.

There are several types of ADC capable of operating at video-rate frequencies. These includes flash converters, folding and interpolating converters and subranging converters. flash ADCs are too costly for high resolutions because their complexity increases exponentially with the number of bits. A 10 bit flash ADC will require 1023, low-offset, comparators. The folding and interpolating ADCs use a much reduced number of comparators, but offset specifications are still stringent. In this paper, we will focus on the architecture of the pipelined subranging ADCs. These ADCs can use a digital correction technique [6] to deal with comparator offsets, relaxing substantially the comparator design and reducing the total required power.

Following this introduction, Section II describes the ADC's architecture. Section III details the CMOS implementation of its building blocks. Results from Monte-Carlo and transistor-level simulations are presented in Section IV and experimental results are provided in section V. This paper ends with the VI section.

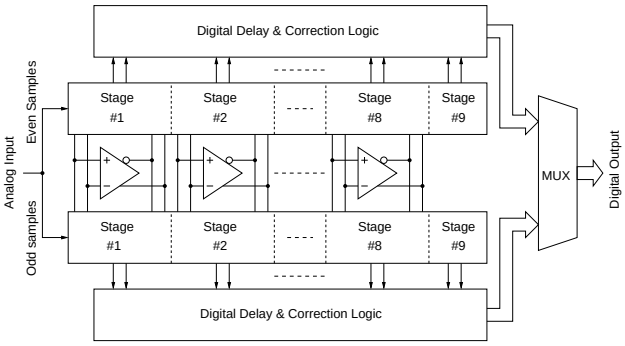

Fig. 1. Block diagram of the ADC.

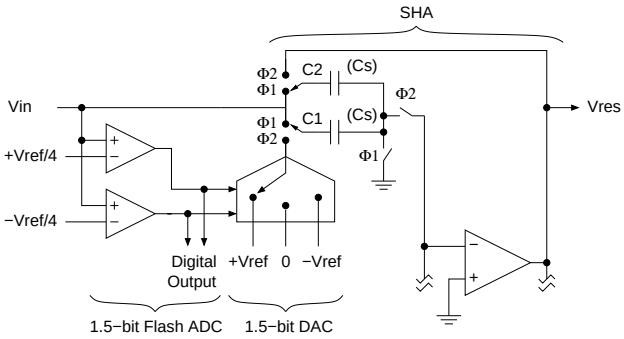

Fig. 2. Simplified, single-ended, schematic of stages #1 to #8. Stage #9 only includes the flash ADC.

II. ADC Architecture

The ADC presented in this paper is basen on switched-capacitor (SC) circuits. These circuits can achieve very good accuracy which is a key factor for an ADC that cannot tolerate relative errors bigger than 0.1%. The drawback of SC circuits is their requirement for linear capacitors. However, these capacitors are available in most CMOS technologies as an option.

In our converter the power supply voltage is 2.5 V, high enough to operate conventional CMOS switches without bootstrapping circuits. The circuit uses a non-overlapping, two-phases, 20-MHz clock that is generated from the 40-MHz clock input via toggling flip-flop.

The block diagram of the ADC is shown in Fig. 1. It is a nine-stage, 1.5-bit/stage, time interleaved, dual pipeline converter. One pipeline processes the even samples, while

the other pipeline works on odd samples. Both pipelines share their operational amplifiers [7]. This constitutes a big power saving, because operational amplifiers are the most power-demanding blocks, and helps to minimize offset and gain mismatches between pipelines that could degrade the ADC's performance [8]. Each stage provides two bits but the LSB bit is redundant allowing the implementation of a digital correction circuit that removes the effect of comparator's offsets [6].

In Fig. 2 a simplified pipeline stage schematic is shown. While this schematic shows a single-ended circuit for clarity, the actual implementation uses fully-differential circuits in order to reduce the effects of supply and substrate noise. Each stage includes a 3-level flash ADC, a 3-level DAC and a sample and hold amplifier (SHA). The flash ADC only needs two low-accuracy comparators to generate the 1.5-bit digital output of the stage. The 1.5-bit DAC is basically an analog multiplexer controlled by the flash ADC's output. It must be noted that, in the fully-differential circuit, the voltage $-V_{ref}$ is obtained by swapping the two V_{ref} lines and, therefore it is accurate giving a linear DAC. The SHA provides the analog memory needed for pipelining and does some analog arithmetic. Its output voltage, assuming ideal components, is:

$$V_{res} = \begin{cases} 2V_{in} + V_{ref} & \text{for } V_{in} < -V_{ref}/4 \\ 2Vin & \text{for } -V_{ref}/4 < V_{in} < V_{ref}/4 \\ 2V_{in} - V_{ref} & \text{for } V_{in} > V_{ref}/4 \end{cases}$$

The input gain of the SHA must be 2 for a proper ADC operation, but this only happens if the two capacitors C_s are perfectly matched and the open-loop gain of the opamp is infinite. Gain errors bigger than 0.1% will give an unacceptable high ADC nonlinearity. Therefore, great care must be taken to ensure the best possible matching between capacitors and high-gain opamps are needed.

The value of the sampling capacitor C_s is obtained from noise and matching constrains and it is different for each stage. First, we want a total sampling noise below the ADC quantization noise:

$$2\sqrt{\frac{KT}{C_s}} \ll \frac{1}{\sqrt{12}} \frac{V_{swing}}{2^{N-i}}$$

In this inequality V_{swing} is the maximum signal amplitude ($2V_{ref}$) that is limited by the supply voltage and the operational amplifier design, N is the number of bits of the ADC and i is the stage number. Note that, the minimum value of C_s is divided by 4 each time we go to the next pipeline stage.

On the other hand, the relative statistical error of N identical, parallel-connected capacitors is:

$$\sigma_N = \frac{\sigma_{unit}}{\sqrt{N}}$$

This means that the relative accuracy improves with the square root of the capacitance, and therefore, the minimum required capacitance is also divided by 4 when we go to the next pipeline stage.

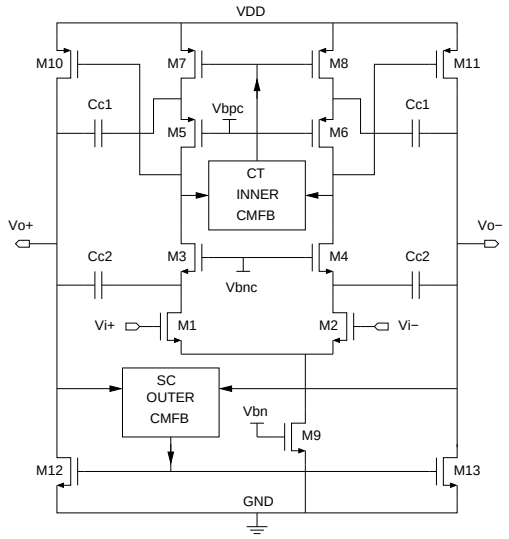

Fig. 3. Operational amplifier schematic.

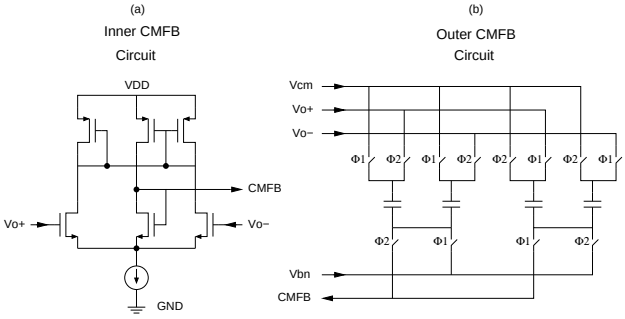

Fig. 4. Common-mode feedback circuits for operational amplifiers. Left: Input stage CMFB circuit. Right: Output stage CMFB circuit.

In our design the sampling capacitance is limited by matching rather than noise because we still have a high voltage swing ($2V_{swing}$= 3.2 V peak-to-peak, differential). According to our technology matching data, the sampling capacitors were chosen as 0.8 pF for the first stage, 0.2 pF for the second stage and 0.1 pF for the remaining stages. These values give a 3σ mismatch of about 0.05% for the first stage, and therefore they guarantee a maximum nonlinearity of about 0.5 LSB without any calibration technique. The minimum 0.1 pF capacitor value was selected to be still substantially larger than the parasitic input capacitance of opamps, thus avoiding the degradation of the opamp's bandwidth.

III. Functional Blocks Description

A. Operational Amplifiers

Operational amplifiers must meet several specifications:

- Open-loop gain: A_v > 60 dB. Low gain gives high ADC nonlinearity.
- Slew rate: SR > 128 V/μs. This allows a full output excursion during 1/4th of a clock cycle (12.5 ns).
- Gain-bandwidth product: GBW > 200 MHz. This gives a small-signal settling time shorter than 1/4th of a clock cycle with better than 0.1% accuracy.

- Total input-referred noise: $V_n < 2^{i-1}\frac{1}{\sqrt{12}}V_{LSB}$. This noise must be lower than the i-stage quantization noise.

These parameters depends on the loading capacitance, which, in turn, depends on the pipeline stage number. Thus, three different operational amplifiers were designed: one for first stage, one for second stage, and one for the remaining stages.

The operational amplifier schematic is shown in Fig. 3. It is a two-stage fully-differential opamp with cascoded Miller compensation. The input stage is a telescopic cascode amplifier, which gives a reasonable high gain with short-channel devices. This stage is followed by inverters which provides a rail-to-rail output swing and 30 dB additional gain. The typical opamp open-loop gain exceeds 80dB. It is well known that cascoded Miller compensation improve the GBW with respect to a conventional Miller compensation [9]. Splitting the compensation capacitor into two capacitors, C_{C1} and C_{C2}, connected to $M3$ and $M5$ sources, we can achieve a further GBW improvement. If $g_{m5}/C_{C1} = g_{m3}/C_{C2}$, we can represent the opamp by an equivalent circuit with a single compensation capacitor $C_C = C_{C1} + C_{C2}$ and a single cascode transistor with total transconductance $g_m = g_{m5} + g_{m3}$. Thus, having a bigger transconductance for a given compensation capacitance helps to move non-dominant poles towards high frequency, improving the stability. Alternatively, we can use a smaller compensation capacitance for the same stability specifitations obtaining a higher GBW.

The operational amplifiers are fully differential circuits, therefore, they require common-mode feedback (CMFB). Each opamp stage has its own CMFB circuit. These circuits are shown in Fig. 4. Having a CMFB loop on each stage gives very stable CMFB response without any compensation capacitors. The input stage CMFB circuit is a differential amplifier-like circuit that only works properly for low amplitude differential signals. This circuit is not appropriate for the output stage because there the voltage swing is much higher. In this case two highly linear switched-capacitor networks are used. During one clock phase one network provides the common-mode feedback while the other is refreshing its capacitor voltages and roles changes during the other clock phase.

Spectre simulations show that the first stage opamp consume about 1.93 mW. This is about 16% of the total ADC power. The power consumption of all opamps is 6.43 mW. Sharing the opamps between the two ADC pipelines we are saving about 55% of the final ADC power.

From our simulations we also know that the first stage opamp noise is about 15 dB below the ADC quantization noise.

B. Flash ADCs and Comparators

Each stage includes a 3-level flash ADC whose schematic is shown in Fig. 5. The circuit complexity is due to the fact that both reference and input are differential signals. A switched-capacitor network is used to subtract

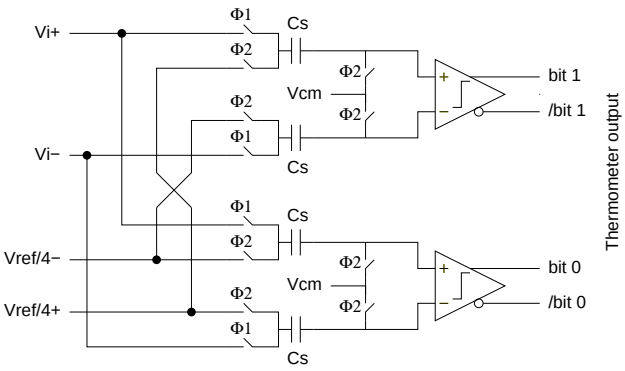

Fig. 5. Differential, 3-level, flash ADC.

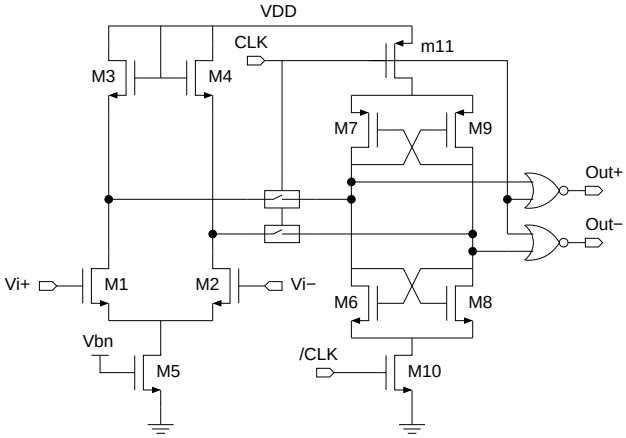

Fig. 6. Regenerative comparator.

the reference from the input and, then, a comparator decides if the result is positive or negative. This circuit has the advantage that the subtracting capacitors, C_S, remain charged from one cycle to the next. Therefore, there is not charge-pumping through capacitors, so, a very little current flows even for large capacitors. On the other hand, this circuit is sensitive to clock feedtrough from switches, but this problem is minimized thanks to digital correction. The value of C_S is 0.1 pF.

The comparator circuit is shown in Fig. 6. It consists of a low-gain preamplifier, a full-swing latch, and two NOR gates. The main purpose of the preamplifier is to isolate the subtracting capacitors from the large voltage pulses of the latch. Its gain is not much bigger than one, because bigger gains would require too much GBW and power consumption, and we can tolerate large comparator offsets. Latch regeneration is very fast due to the big overdrive voltages of m6 and m7 and the small loading capacitance. Its time-constant, τ, is about 70 ps. Therefore, the chances of metastability, that are proportional to $\exp(-t_{setup}/\tau)$, with $t_{setup} \approx 25$ ns, are totally negligible [10]. The NOR gates gives a logic-one output during the sampling period, avoiding intermediate voltage levels that otherwise will increase the power consumption of the following digital circuitry.

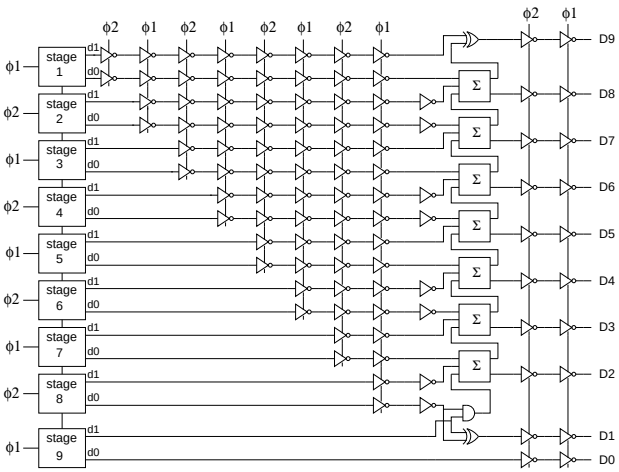

Fig. 7. Digital delay and correction logic schematic. Only one circuit is shown.

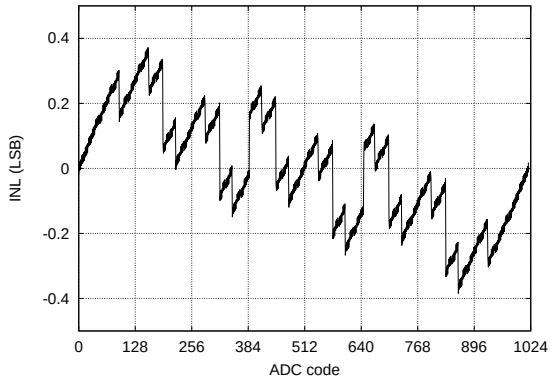

Fig. 8. Typical INL curve of the ADC.

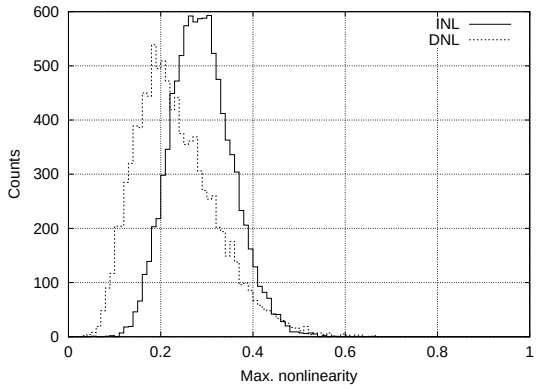

Fig. 9. Monte-Carlo results for the ADC's maximum nonlinearity. Solid line: INL. Dotted line: DNL.

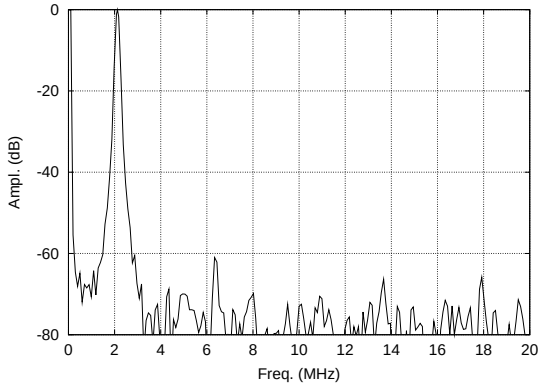

Fig. 10. Spectrum of a digitally converted sinusoid obtained from a transistor-level simulation.

C. Digital circuitry

Digital circuitry includes delay equalizing registers and digital correction for each ADC pipeline. Fig. 7 shows the schematic of these circuits. All registers are dynamic, of C^2MOS type, allowing a very compact layout and low-power operation. The digital correction algorithm is merely the addition of all redundant bits together. These circuits are implemented as 9-bit, serial-carry, adders. No fast-carry logic is needed for this clock frequency.

Digital circuitry runs on a separate power bus. An additional 3.3 V power line is provided for pin drivers. The power consumption of the digital logic, excluding pin drivers, was estimated at 1.75 mW from extracted circuit simulation.

IV. Simulation results.

Two different types of simulation were carried out in order to test the design robustness. First, a behavioral model simulator was written in C language. This simulator includes the effects of capacitor mismatching, finite opamp gain and comparator offset. The digital correction algorithm was also included in the simulation. A Monte-Carlo simulation was carried out by simulating a large number (10000) of different ADCs with Gaussian random variations in their capacitor values and comparator offsets. In this simulation the key component values were:

C_s , Fist stage	0.8 pF
C_s , Second stage	0.2 pF
C_s, Stages 3-8	0.1 pF
opamp's DC gain	70 dB
comparator offset	σ = 10 mV

The nonlinearity of each ADC was analyzed by finding the threshold voltage of each ADC code. Fig 8 shows a typical integral nonlinearity graph (INL) for an ADC with random variations in its component values. The histograms of Fig. 9 were built by finding the maximum absolute nonlinearity of each ADC. This figure shows that, using the proposed design parameters, the 99% of ADCs have a maximum INL and DNL below 0.5 LSB.

Other simulations were carried out after the completion of the test chip layout by using Spectre and an extracted netlist from the layout. This netlist included about 45000 devices, most of them parasitic capacitances, and, therefore, these simulations were very time consuming. The correct behavior of the ADC, at the transistor level, was proven in this way. Fig. 10 shows the output spectrum after A-to-D conversion for a full-scale, single tone input. Due to the long time required, only 400 ADC samples were recorded, but they are enough to show that the harmonic distortion is less than -60 dB. In this simulation the capacitor mismatching was not included. The observed distor-

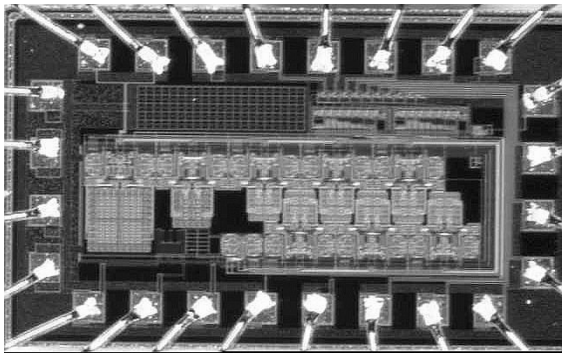

Fig. 11. Chip photograph.

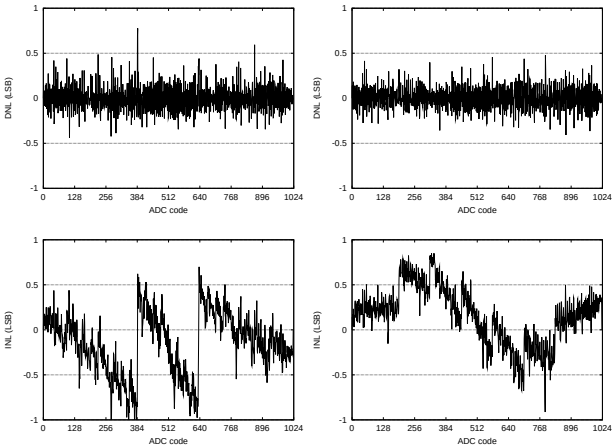

Fig. 12. Differential nonlinearity (DNL) and integral nonlinearity (INL) for the two pipelines of the ADC.

tion is due to finite opamp gain, incomplete opamp settling due to finite bandwidth, and other dynamic fenomena like charge injection from switches. The extracted circuit simulation also gave us a confident estimation of the power consumption of the chip.

V. Experimental results

The proposed ADC was fabricated in the Agere's 0.25-μm CMOS technology. The chip photograph is shown in Fig. 11. The unpackaged die was bonded to a PCB board that included, among other components, decoupling capacitors for power supplies and buffers for digital outputs. several test were carried-out to measure the ADCś performance.

First, the linearity of both ADC's pipelines were measured following the code-density approach [11]. The results are displayed on Fig 12. The measured nonlinearities have an average value about 0.5 LSB, but the peak values are higher. These curves shows that the ADC is monotonic and there are no missing codes. The mismatch between the INL of the two pipelines can generate tones at frequencies $f_n = f_s/2 - n \cdot f_{in}$. The offset and gain differences are responsible for tones at $f_s/2$ and $f_s/2 - f_{in}$ respectively [8] while higher order mismatches generate spur tones farther apart from the Nyquist frequency. Because the INL error is lower than 1 LSB these spurs are always lower than -60 dB. The INL tables of Fig 12 can be used to correct the linearity of the converter in the digital domain by subtracting the measured linearity error to the output. This technique can achieve an improved linearity and matching between pipelines, but requires calibration.

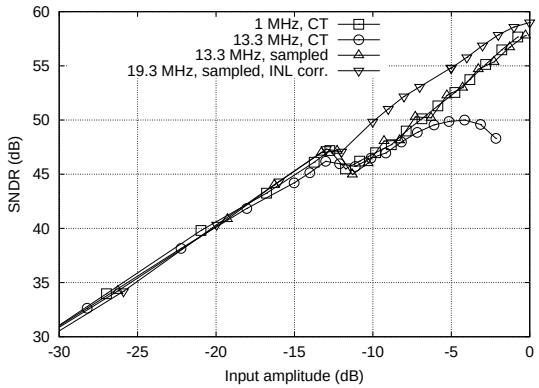

Fig. 13. Measured signal to noise and distortion ratios (SNDR) for several input frequencies and conditions.

TABLE I
ADC performance

Resolution	10 bits
Sampling Rate	40 MHz
Power consumption	ADC: 11.7 mW
	Pin drivers: 1.3 mW ($C_L \approx 4.5$ pF)
Technology	2.5 V 0.25-μm CMOS (MOM cap.)
Chip Area (w. pads)	1.5×0.88 mm^2
Nonlinearity (max)	DNL: 0.77 LSB
	INL: 1.15 LSB
SNR (max)	61.3 dB @ 10.6 MHz
SNDR (max)	57.6 dB @ 1 MHz
	57.8 dB @ 19.3 MHz†
ENOB (max)	9.3 bits @ 1 MHz
	9.3 bits @ 19.3 MHz†

† Sampled input, without static INL correction.

The dynamic performance of the ADC was measured by applying a single tone to the inputs and analyzing the recorded code stream in the frequency domain. Fig 13 shows the measured signal to noise and distortion ratio (SNDR) for several input frequencies and conditions. The SNDR curves shows an abrupt drop for input amplitudes around -12 dB. This is due to the big INL transitions of one pipeline for input amplitudes of 1/4 of full scale. The SNDR also drops gradually for high frequency inputs. This problem was found to be due to the nonlinear resistance of the switches in the first pipeline stage, and it is only present if the input is a continuous-time (CT) signal. To prove this point a sampled sinusoid was applied to the input and the resulting SNDR curve showed no performance drop. Finally, after applying the INL correction mentioned before, the obtained SNDR curve shows a very little performance loss, even for input frequencies close to Nyquist, if the input signal is sampled.

The measured ADC performance is summarized on Table I. It worth mention the low power achieved.

VI. Conclusions

In this work a dual-pipeline, time-interleaved, CMOS ADC is designed in a 0.25 μm CMOS technology with metal-oxide-metal capacitor option. This ADC has a sampling rate of 40 MHz, and it provides 10 bits of resolution. The power consumption is only 12 mW. This low power is achieved mainly by sharing operational amplifiers between pipelines and by the use of digital correction for comparator offsets. Our simulations shows that good linearity and high yield can be achieved without applying any calibration technique.

The experimental results were close to simulations when the input signal is sampled. In order to improve the linearity for high-frequency, continuous-time inputs a SHA must be inserted before the ADC. Our power estimation for such SHA is about 4 mW. Alternatively, the switches of the first pipeline stages can be replaced with highly linear, bootstrapped switches. The matching between pipelines and the linearity of the ADC can be improved by using INL correction. This technique can raise the resolution of the measured converter by about 0.5 effective bits. Because the INL of the converter have to be measured before the correction can be implemented, the increased circuit complexity would be only justified for critical applications.

VII. Acknowledgment

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