Low-Power Pipeline ADC for Wireless LANs

J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla

***Abstract*—In this paper, a 10-bit 40-MS/s analog-to-digital converter (ADC) is presented. A power consumption of 12 mW was achieved by using a time-interleaved and pipelined architecture with shared operational amplifiers. This circuit was fabricated in a 2.5-V 0.25-μm technology with metal–oxide–metal capacitors. Experimental results are within design ranges and are in good agreement with simulation data. It turns out that the proposed Nyquist-rate ADC provides a potential solution for low-power high-speed applications, e.g., wireless LANs.**

***Index Terms*—CMOS, data converter, low power, pipelined ADC, switched capacitor, time-interleaved.**

I. Introduction

THE NEW GENERATION of wireless-LAN adapters based on the IEEE 802.11 a/g standards [1] imposes a significant challenge to circuit designers. The wide signal bandwidth demands a high sampling rate for ADCs and DACs while, on the other hand, the power consumption must be kept low in order to extend the battery life of portable wireless devices. The ADC specifications depend on the receiver architecture. For direct-conversion receivers, two 20-MS/s ADCs are needed, while, for low-IF receivers only one 40-MS/s ADC might be sufficient. The OFDM modulation used in the IEEE 802.11a standard [1] also demands a high resolution for these converters. At least 10 bits are needed in typical receiver designs in order to avoid an increased bit-error rate due to ADC's quantization. The power consumption of state-of-the-art 10-bit ADCs is on the order of 1–3.7 mW per MHz [2]–[7]. This is a significant portion of the total receiver power.

In this paper, a low-power, time-interleaved, pipeline ADC is presented. Section II describes the ADC's architecture and details the CMOS implementation of its building blocks. Experimental results are presented in Section III, and Section IV concludes this paper.

II. ADC Architecture

The ADC presented in this paper is designed and built around a 0.25-μm CMOS technology with highly linear, metal–oxide–metal capacitors. The supply voltage is 2.5 V and the ADC runs from a nonoverlapping two-phase 20-MHz clock that is derived from the 40-MHz clock input.

The block diagram of the ADC is shown in Fig. 1(a). It is a nine-stage 1.5-bit/stage time-interleaved dual-pipeline converter [8]. One pipeline processes the even samples, while the other pipeline works on odd samples. Both pipelines share their operational amplifiers (opamps) [9]. This constitutes a large power saving, because opamps are the most power-demanding blocks, and helps to minimize offset and gain mismatches between pipelines that could degrade the ADC's performance [10]. The schematic of each stage is shown in Fig. 1(b). It includes a sample and hold amplifier (SHA), 3-level flash ADC, and a 3-level DAC, and provides two output bits, although the LSB bit is redundant. This allows the implementation of a digital correction circuit that removes the effect of comparator's offsets [11]. The sharing of the opamp is done by including the switch S1 in series with the opamp input.

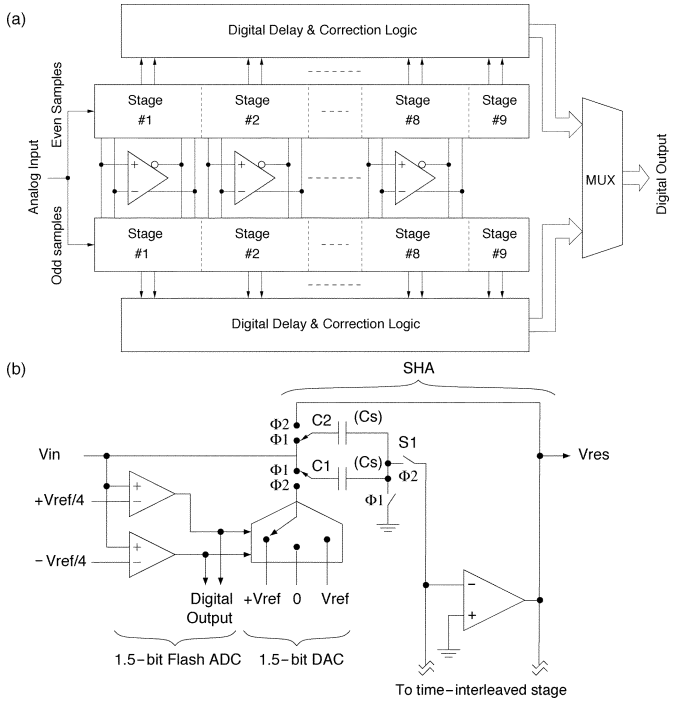

Fig. 1. (a) Block diagram of the ADC. (b) Simplified schematic of stages #1 to #8. Stage #9 only includes the flash ADC.

The value of the sampling capacitor of the SHA, C_s, is obtained from noise and matching constrains and it is different for each stage. The minimum value of C_s is divided by 4 each time we go to the next pipeline stage in order to achieve maximum power savings. This scaling was done for the two first pipeline stages. The remaining stages are identical, but they have a little impact to the total ADC power consumption [12]. In our design, C_s is limited by matching rather than noise because a relatively large voltage swing is available. According to our technology matching data, the sampling capacitors were chosen as 0.8 pF for the first stage, 0.2 pF for the second stage, and 0.1 pF for the remaining stages. These values give a 3σ mismatch of about 0.05% for the first stage, which is low enough to operate

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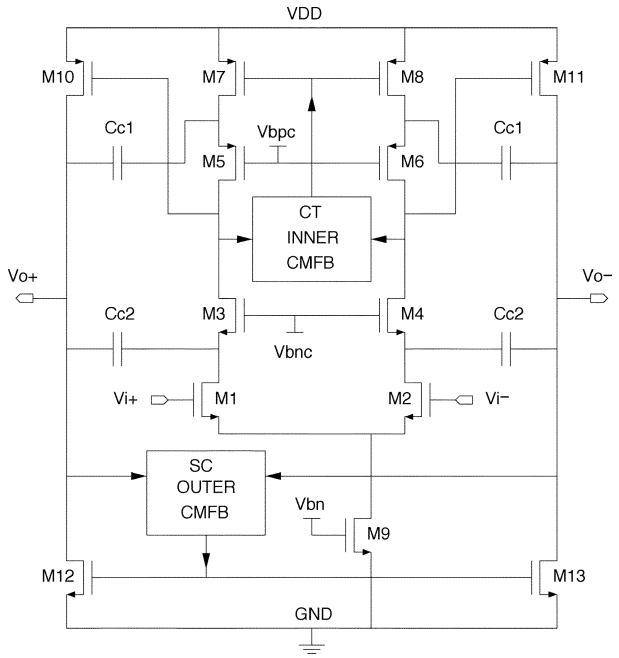

Fig. 2. Operational amplifier schematic.

without any calibration. The minimum capacitor value, 0.1 pF, was chosen to be still substantially larger than related parasitic capacitances.

The opamps used in the SHA are shown in Fig. 2. They are two-stage class-A fully differential opamps with cascode Miller compensation [13] where the input stage is a telescopic cascode. A common-mode feedback circuit has been used for each stage, providing an improved common-mode stability. Spectre simulations show that the first-stage opamp consumes about 1.9 mW. The power consumption of all opamps is 6.4 mW, while the total ADC power is about 12 mW.

Each pipeline stage includes a 3-level flash ADC. This ADC is based on a switched-capacitor (SC) circuit, which subtracts $\pm 1/4$th of the reference from the input voltage, followed by a comparator. The comparator consists of a preamplifier and a full-swing, regenerative, latch. The DAC is just a differential analog multiplexor.

Digital circuitry includes delay equalizing registers and digital correction for each ADC pipeline. All registers are dynamic, of C^2MOS type, allowing a very compact layout and low-power operation. The digital correction algorithm is merely the addition of all redundant bits together.

Digital circuitry runs on a separate power bus. An additional 3.3-V power line is provided for pin drivers. The power consumption of the digital logic, excluding pin drivers, was estimated at 1.75 mW from simulation.

III. Experimental Results

The ADC was fabricated in a standard 0.25-μm CMOS technology with an additional metal–oxide–metal analog-capacitor option. The chip photograph is shown in Fig. 3. The total chip area, including pads, is 1.5×0.8 mm^2. The chip was bonded to a PCB board using a room-temperature conductive glue.

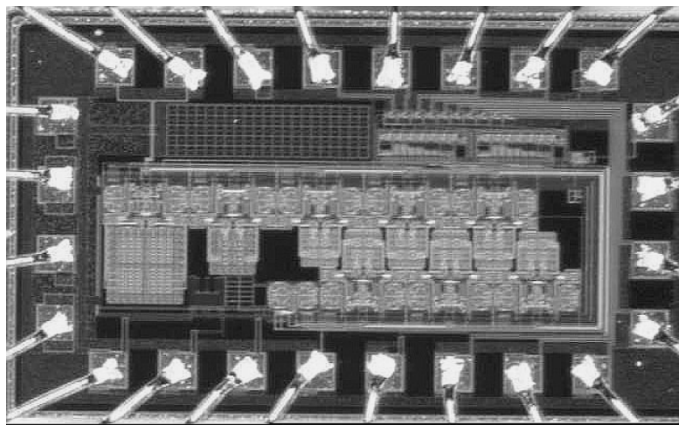

Fig. 3. Die photo of ADC.

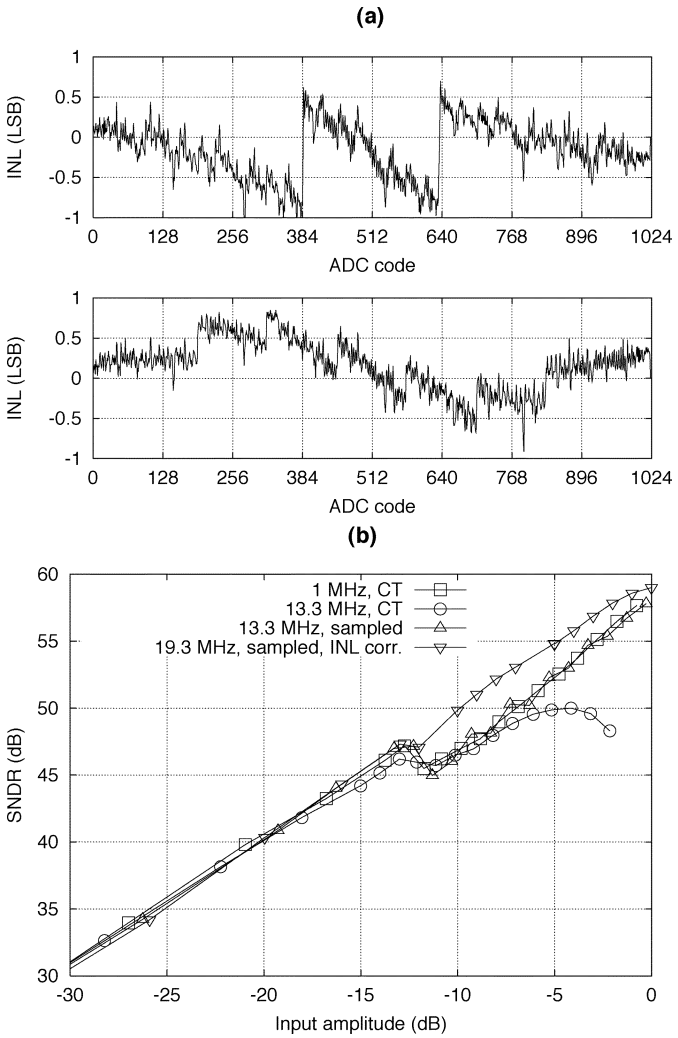

Fig. 4. Experimental results. (a) INL graphs for the two time-interleaved pipelines of the ADC. (b) SNDR versus input amplitude for different conditions (see text).

Fig. 4(a) shows the integral nonlinearity (INL) graphs of the converter. These graphs were obtained using code density analysis [14]. This figure shows a different INL for each pipeline of the ADC. While one pipeline shows big transitions for codes at $\pm 1/4$ of the input range (suggesting a gain error in the first

TABLE I
MEASURED ADC PERFORMANCE

Resolution	10 bits
Sampling Rate	40 MHz
Power consumption	ADC: 11.7 mW
	Pin drivers: 1.3 mW ($C_L \approx 4.5$ pF)
Technology	2.5-V, 0.25-μm, CMOS (MOM cap.)
Chip Area (w. pads)	1.5×0.88 mm^2
(wo. pads)	1.2 × 0.58 mm^2
Nonlinearity	DNL: 0.77 LSB
	INL: 1.15 LSB
SNR (max)	61.3 dB @ 10.6 MHz
SNDR (max)	57.6 dB @ 1 MHz
	57.8 dB @ 19.3 MHz†
	59.0 dB @ 19.3 MHz††
ENOB (max)	9.3 bit @ 1 MHz
	9.3 bit @ 19.3 MHz†
	9.6 bit @ 19.3 MHz††

Notes:
† Sampled input.
†† Sampled input and static INL correction.

stage), the other pipeline has a smoother INL graph. The INL mismatch is responsible for high-frequency spurs at frequencies $f_n = f_s/2 - n \cdot f_{in}$. The spur tone for $n = 0$ is due to offset mismatch between pipelines, while the tone for $n = 1$ is due to gain mismatch [10]. These mismatches can be obtained from INL graphs. We obtained an offset mismatch of about 0.3 LSB and a gain mismatch of about 0.56 LSB/full scale. It is worth mentioning that the static nonlinearity of the ADC can be corrected in the digital domain, as long as the ADC is monotonic. In this case, two INL calibration tables would be required due to the interleaved architecture of this ADC.

Several tests were also performed in the frequency domain. The signal-to-noise-and-distortion ratio (SNDR) of the converter is plotted for several input frequencies and amplitudes in Fig. 4(b). This graph shows a performance drop at -12-dB input amplitude that is due to the nonlinearity of one ADC pipeline witch presents big transitions for amplitudes about $\pm 1/4$ of the full-scale input [Fig. 4(a)]. We can also see a performance degradation for high input frequencies (13.3-MHz curve). This dynamic nonlinearity can be related to the nonlinear resistance of the input switches and to the acquisition bandwidth mismatch in the flash ADC and the SHA. Spectre simulations show that the dominant effect is the former. In any case, this performance drop is not present if the input signal is sampled before the A/D conversion (13.3 MHz, sampled). If the static INL correction is also applied, the obtained SNDR curve is almost that of an ideal ADC.

Finally, an error-vector magnitude (EVM) test was carried out in order to test the ADC's performance under real modulated signals. A 54-Mbit/s, 10-MHz carrier (IF), continuous-time, OFDM signal was generated using an Agilent E4438C ESG vector signal generator and applied to the ADC's input. The measured ADC's EVM is close to that of the Agilent vector signal analyzer (with E1439A 95-MS/s ADC), and well below the maximum allowed for 54-Mbit/s OFDM detection (5.6%). These results were obtained with no INL correction.

IV. CONCLUSION

In this work, a 10-bit dual-pipeline time-interleaved CMOS ADC is developed in a 0.25-μm CMOS technology with metal–oxide–metal capacitor option. This ADC has a sampling rate of 40 MHz, and it provides 9.3 effective bits of resolution for low input frequencies and 8.0 effective bits for high input frequencies. The power consumption is only 12 mW (0.3 mW per MHz). This low power is achieved mainly by sharing opamps between pipelines and by the use of digital correction for comparator offsets. A prototype was fabricated and measured. The experimental results are in good agreement with simulations. The ADC exhibits a good performance for the demodulation of OFDM signals. For other general-purpose applications, the ADC input should be preceded by an additional SHA if high-frequency distortion is relevant. Alternatively, improvements of the input switches can be considered.

The ADC performance is summarized in Table I.

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REFERENCES

[1] *IEEE Std., Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications*, 2000.
[2] B. P. Brandt and J. Lutsky, "A 75-mW, 10-b, 20-MSPS CMOS subranging ADC with 9.5 effective bits at Nyquist," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1788–1792, Dec. 1999.
[3] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 318–325, Mar. 2000.
[4] G. Hoogzaad and R. Roovers, "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm^2," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1796–1800, Dec. 1999.
[5] D. G. Nairn, "A 10-bit, 3 V, 100 MS/s pipelined ADC," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2000, pp. 257–260.
[6] A. M. Abo and P. R. Gray, "A 1.5 V, 10 bit, 14.3 Ms/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.
[7] K. Nakamura, R. Carley, and D. Allstot, "A 85-mW, 10-bit 40-Ms/s ADC with decimated parallel architecture," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1994, pp. 495–499.
[8] J. Arias, D. Bisbal, J. San Pablo, L. Quintanilla, L. Enriquez, J. Vicente, and J. Barbolla, "Low power pipelined ADC design for wireless LANs," in *Proc. XVIII Conf. Design of Circuits and Integrated Systems (DCIS 2003)*, Nov. 2003, pp. 399–404.
[9] L. Sumanen, M. Waltari, and K. A. I. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1048–1055, July 2001.
[10] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 261–272, Mar. 2001.
[11] S. H. Lewis, "Optimizing the stage resolution in pipelined, multi-stage, analog-to-digital converters for video rate applications," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 516–523, Aug. 1992.
[12] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelines analog-to-digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294–303, Mar. 1996.
[13] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 629–633, Dec. 1983.
[14] J. Doernberg, H. S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 820–827, Dec. 1984.