agere systems

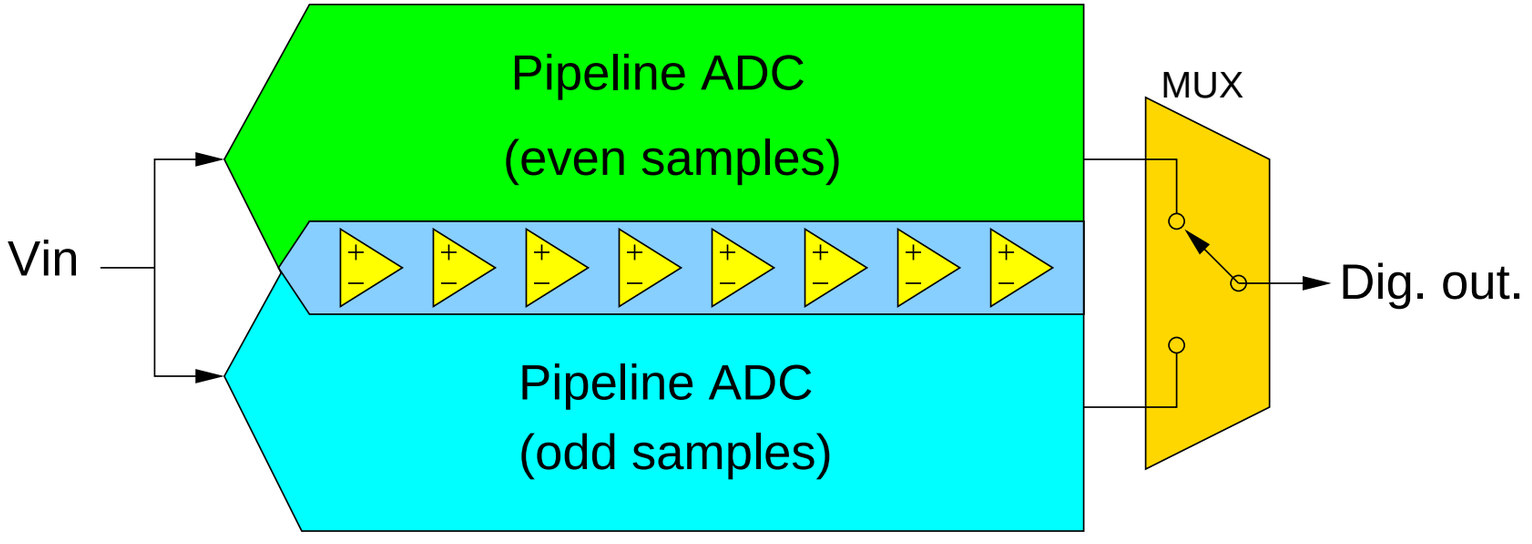
Low Power Nyquist-Rate ADCs

10 bit, 40 Ms/s, pipeline ADC design.

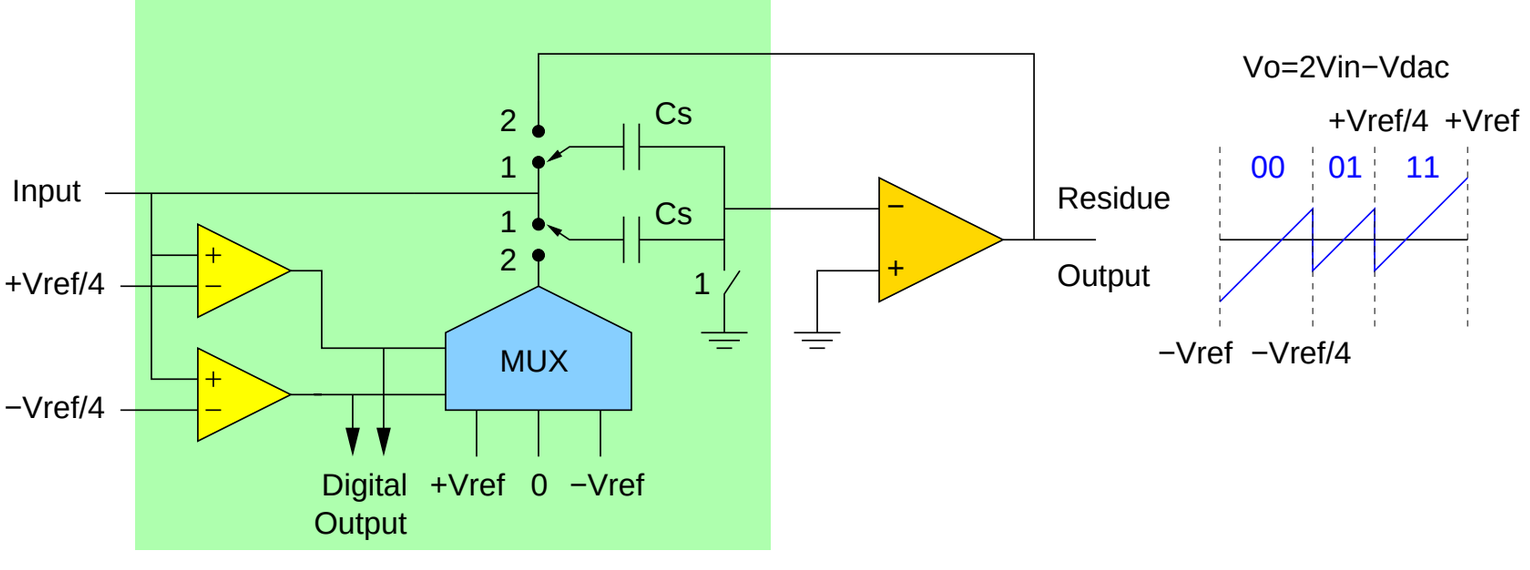
2.5 V, 0.25 μm CMOS.

J. Arias

Global ADC achitecture:



1.5 bits pipeline stage.



Modifications to previous design

⇨ Lower supply voltage: No enough room for a single cascode stage.

⇨ New opamps are two-stages. This gives more DC gain and output swing, but stability demands the use of compensation capacitors.

⇨ Comparators need a new design to accommodate the new input range.

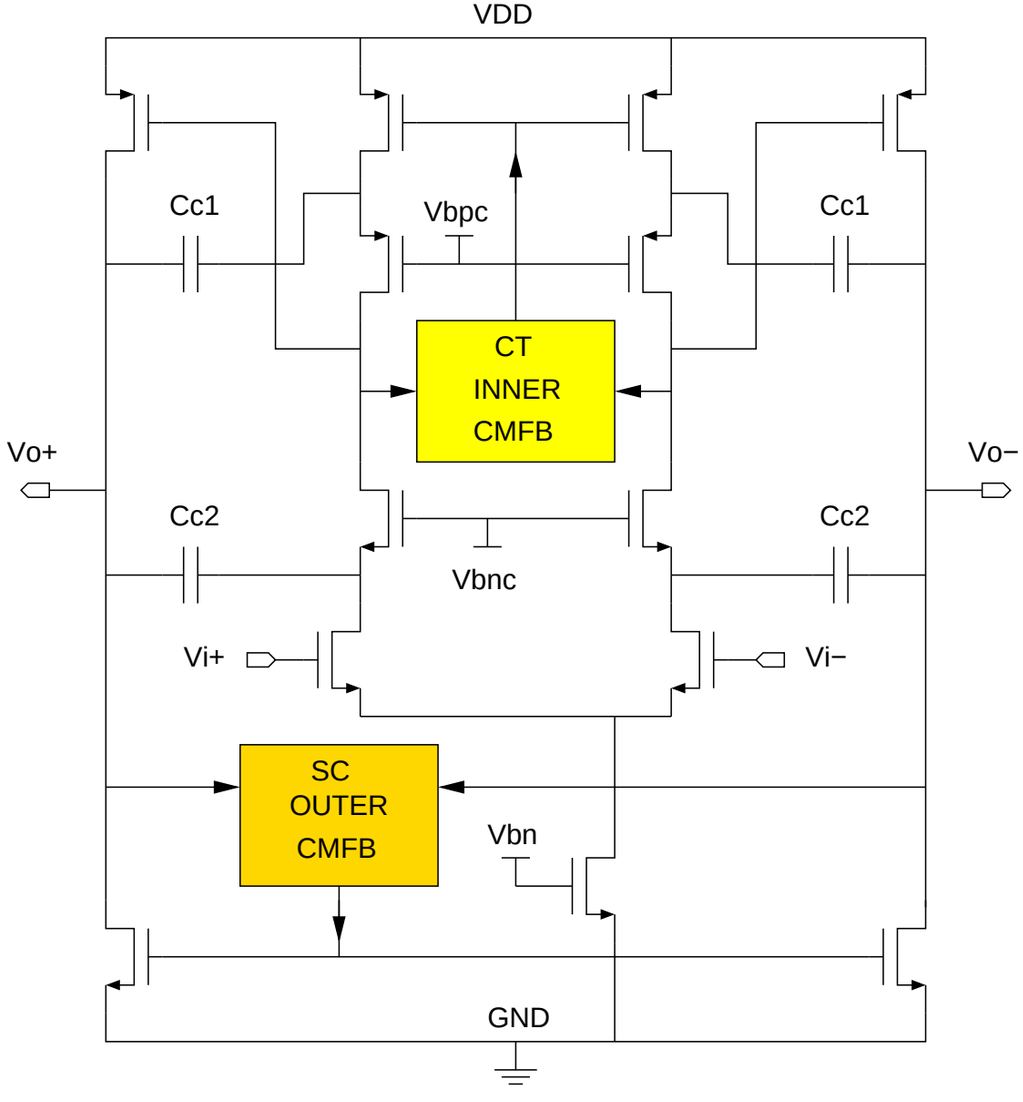
⇨ Switches are fully CMOS transmission gates.

Opamps:

⇨ Specs:

- ✔ Slew-rate high enough to charge the load capacitances in 1/4 of sampling period. ($SR = 4V_{swing} f_s = 166V/\mu s$)
- ✔ Enough Unit-Gain Bandwidth to allow settling to 2^{-N} relative error in 1/4 of sampling period. ($GB \simeq 10\, f_s = 200MHz$)
- ✔ DC gain well over 2^N to get good ADC linearity. (Gain>5000)
- ✔ Must be stable with a feedback factor about 1/2 (gain=2).
- ✔ Total opamp noise below quantization noise.

Rail-to-rail output opamp (2 stages)



First stage is a telescopic cascode:

- Large DC gain:
  - Shorter channel devices.
    - Low Parasitics
- 2 cascode nodes available for compensation:
  - Splitted Compensation Capacitors gives more Gain−Bandwidth or Phase−Margin

Two Common−Mode−Feedback loops:

- Good stability
- Outer loop is a SC circuit due to linearity requirements.

Main Specs:

- Slew rate: 166 V/µs
- Gain−Bandwidth: 200 MHz

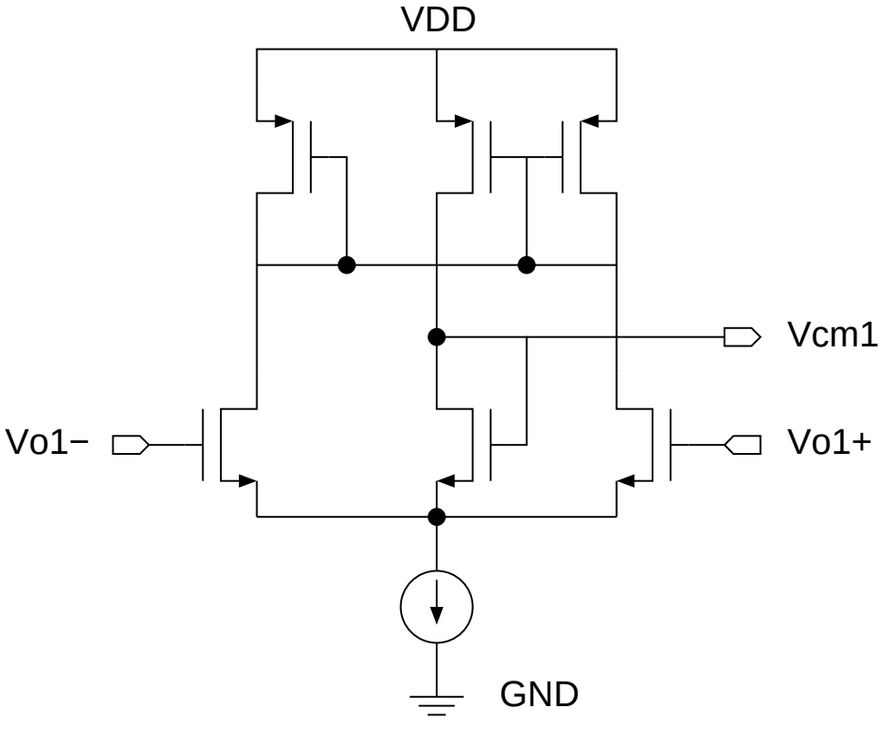
Opamp noise (simulation)

- ⇨ Small, N-channel, input devices can generate large $1/f$ noise, but the total noise integral is dominated by thermal noise due to the big bandwidth.

- ⇨ $1/f$ noise corner below 100 KHz.

- ⇨ Total integrated input noise (BW=200MHz) about $200\mu V$ rms. (15 dB below quantization noise)

Inner Common Mode Feedback

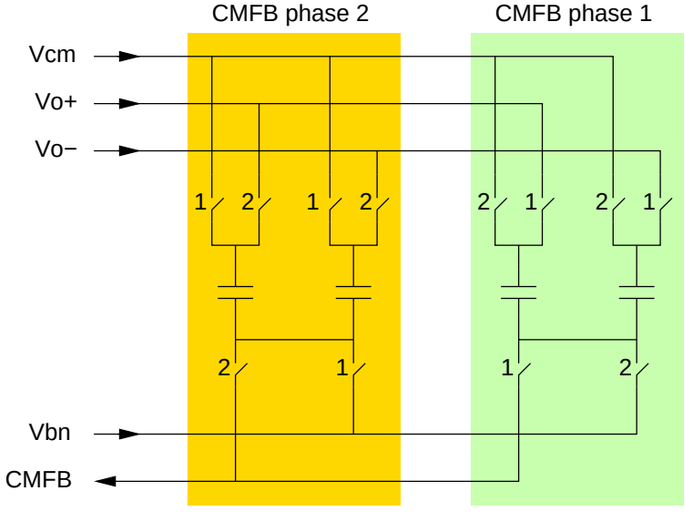


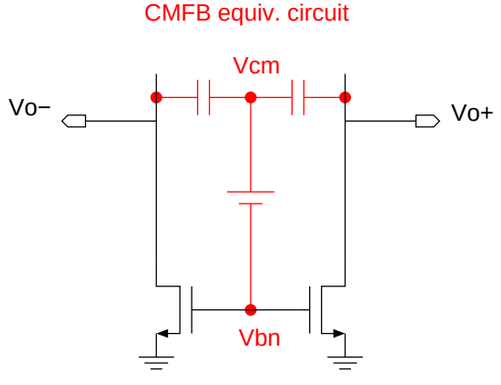
- Continuous-Time CMFB possible because the output voltage swing of first stage is small.

- The circuit is a combination of source followers and level-shifter. It is a small load for the first stage.

- Small devices generate somewhat large noise, but this noise is mainly a common-mode signal.

Outer Common-Mode Feedback

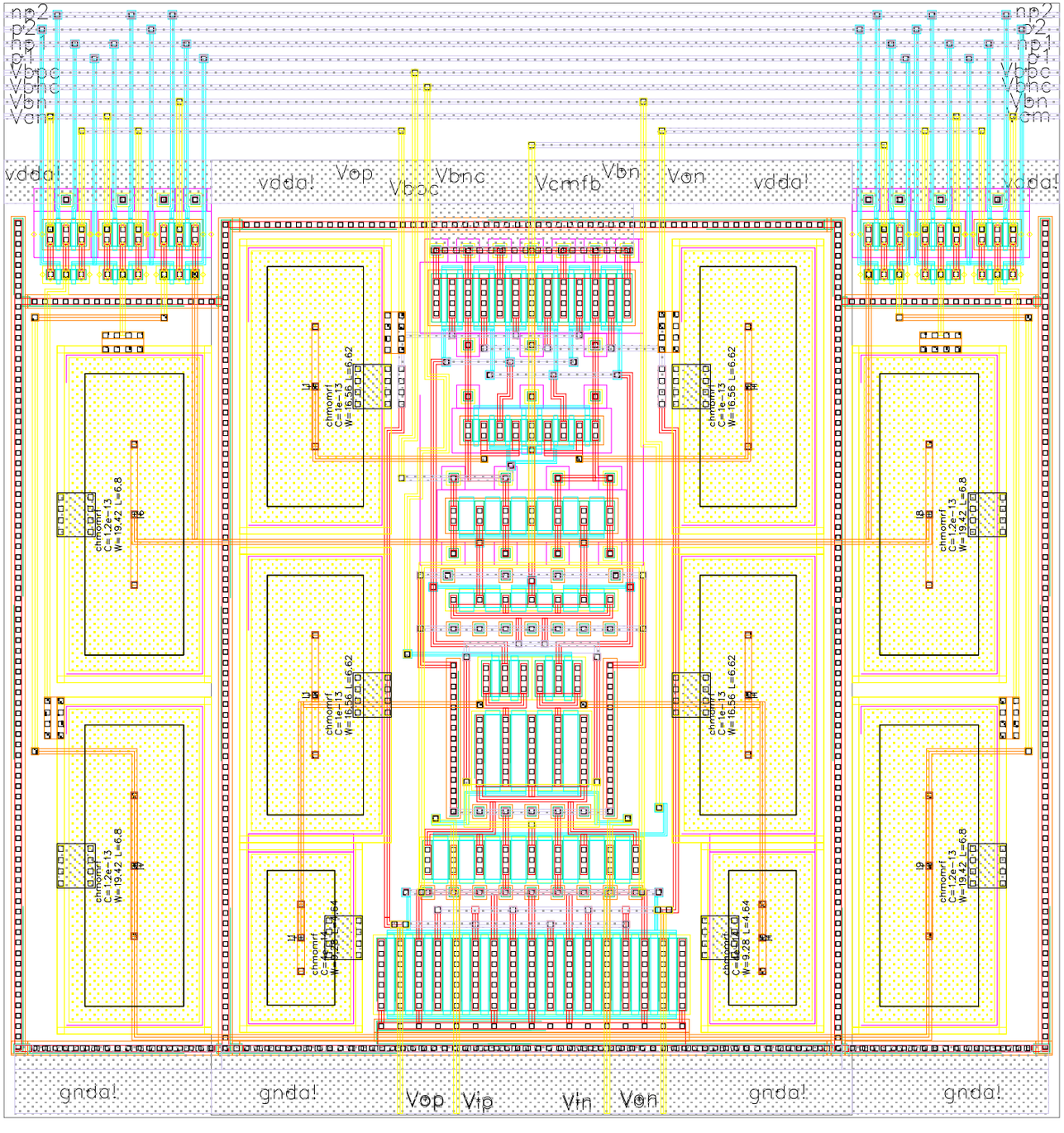




- Two Switched Capacitor sets working on alternate clock phases.

- Highly linear. Linearity is needed because of the high output voltage swing.

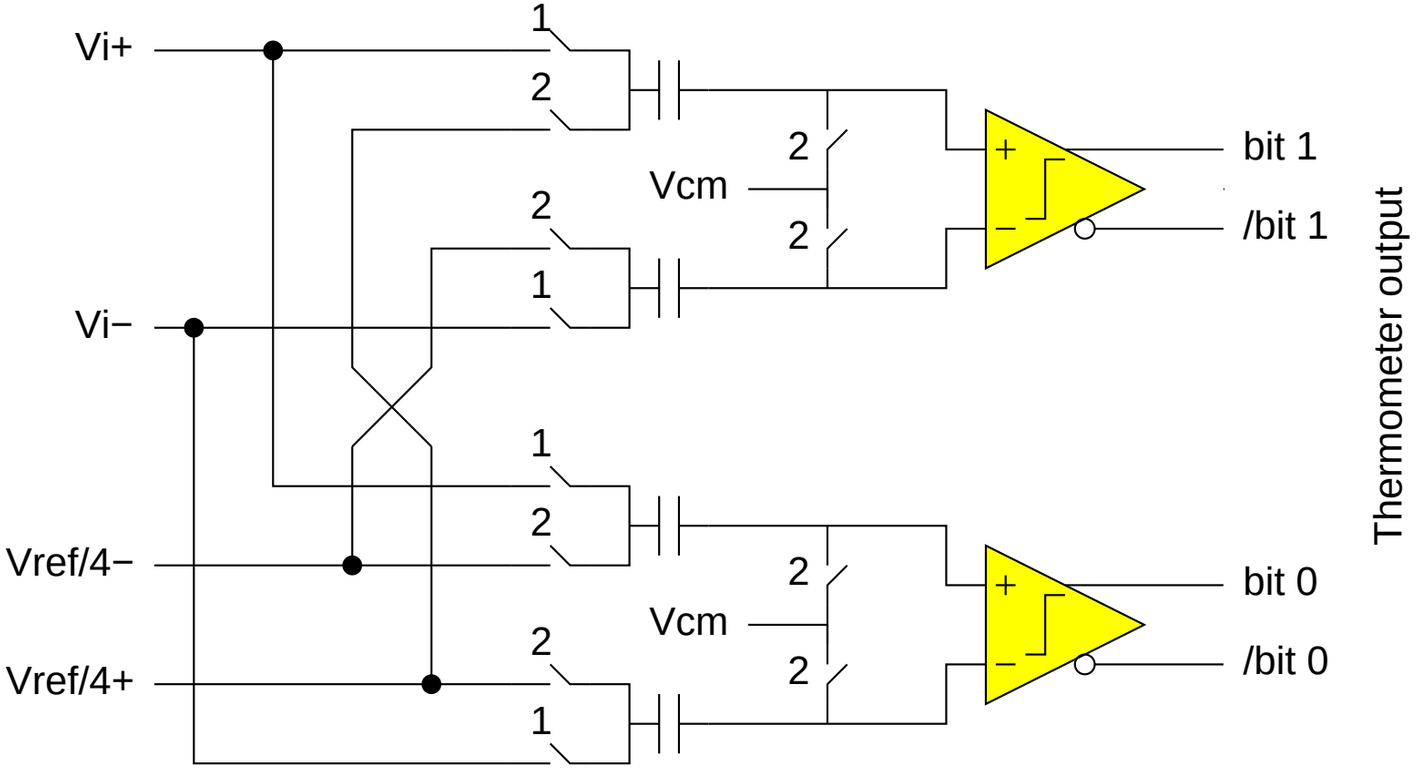
- Output stage can drive large capacitors. CMFB circuit does not load the opamp significantly.


np2
p2
np1
p1
Vbpc
Vbnc
Vcm
Vcmfb
Vbn
Von
Vop
Vip
Vin
vdda!
gnda!
chmomrf
C=12e-13
W=19.42 L=6.8
W=16.56 L=6.62
W=9.28 L=4.64

Switches

- ⇨ Rail-to-rail signals demands a fully complementary switch.
- ⇨ Low ON resistance required when charging large capacitors. ($R_{ON} < 2K\Omega$ for 800fF capacitors).
- ⇨ Switch resistance varies with temperature and and process. Worst case scenario must be taken into account.
- ⇨ Biggest switch: 7/0.28 μm(P-channel), 2.6/0.26 (N-channel). R_{ON} always below $1K\Omega$. Switches are scaled depending on load capacitance. Minimum size switch resistance: 26 $K\Omega$.

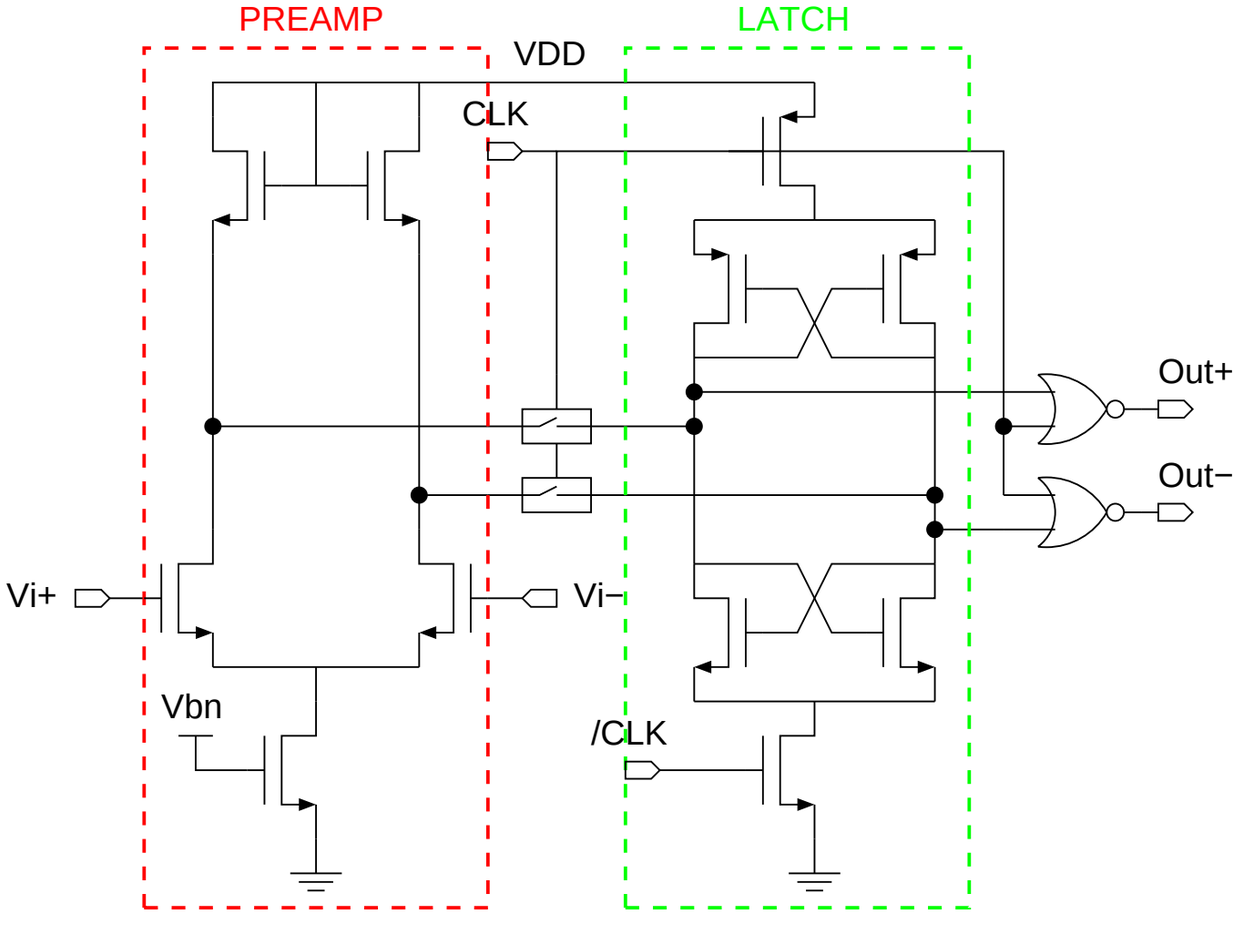
Flash ADCs:



- Thanks to digital correction these ADCs do not need to be very accurate.

- 100pF level-shifting capacitors. These capacitors always remains charged.

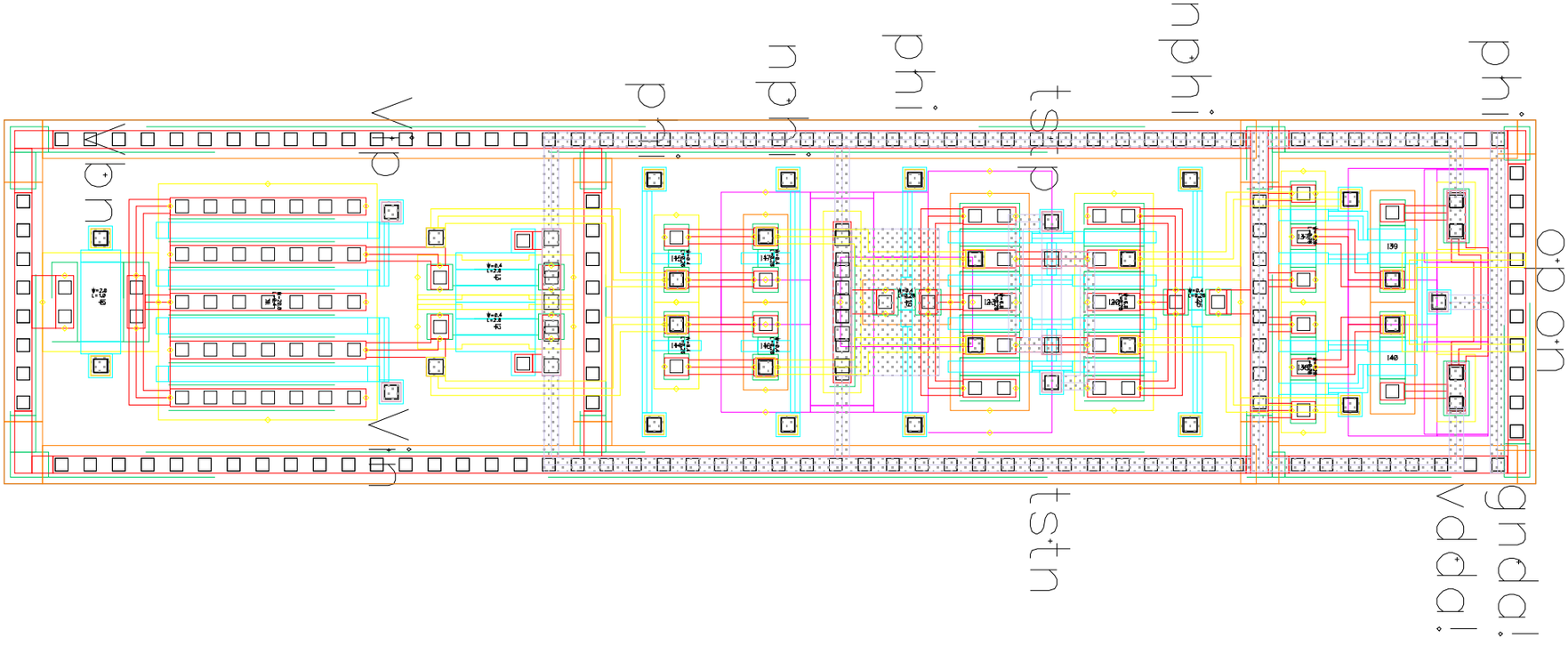
Comparators



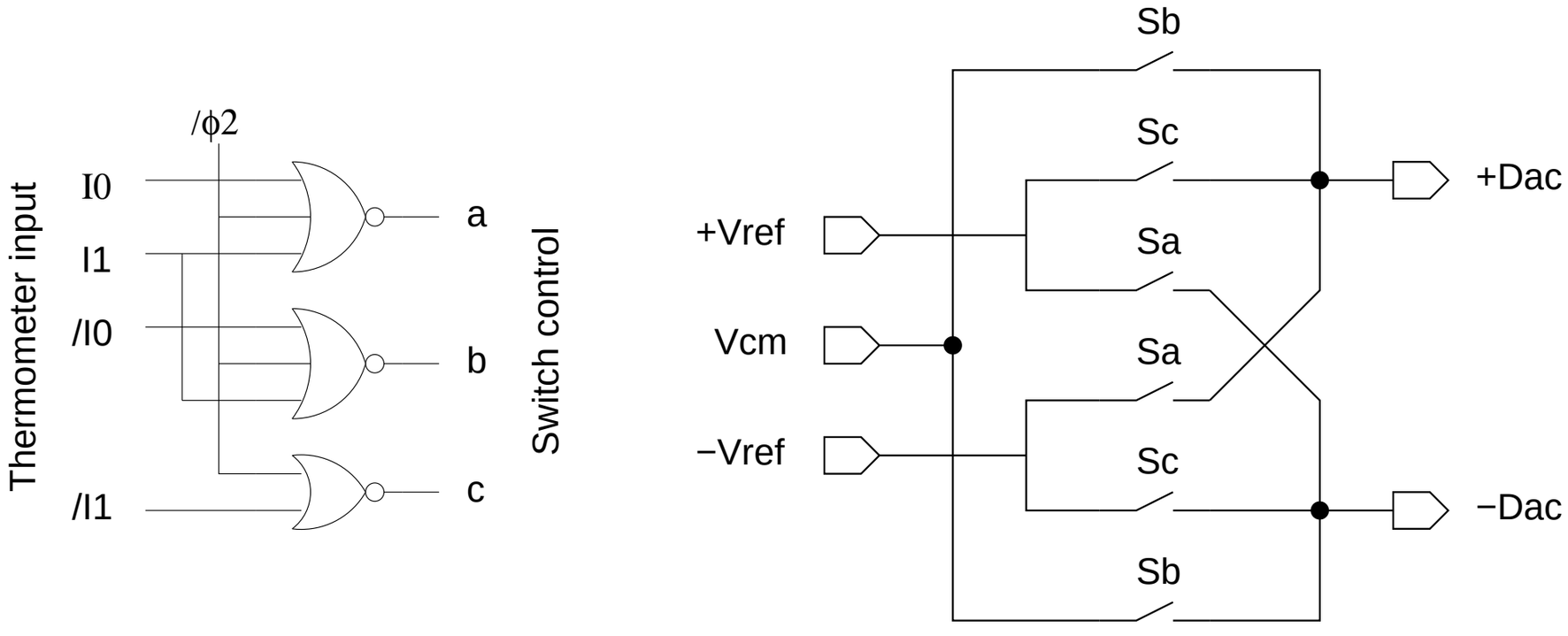
- Regenerative comparator: Low gain preamp + Full swing latch.

- Fast regeneration (<1ns typ.): small chances of metastability.

Comparator layout



DACs



- High impedance output during phase 1. This saves 2 series−switches in the S&H circuit.
- Switch size depends on pipeline position.

Stage scaling

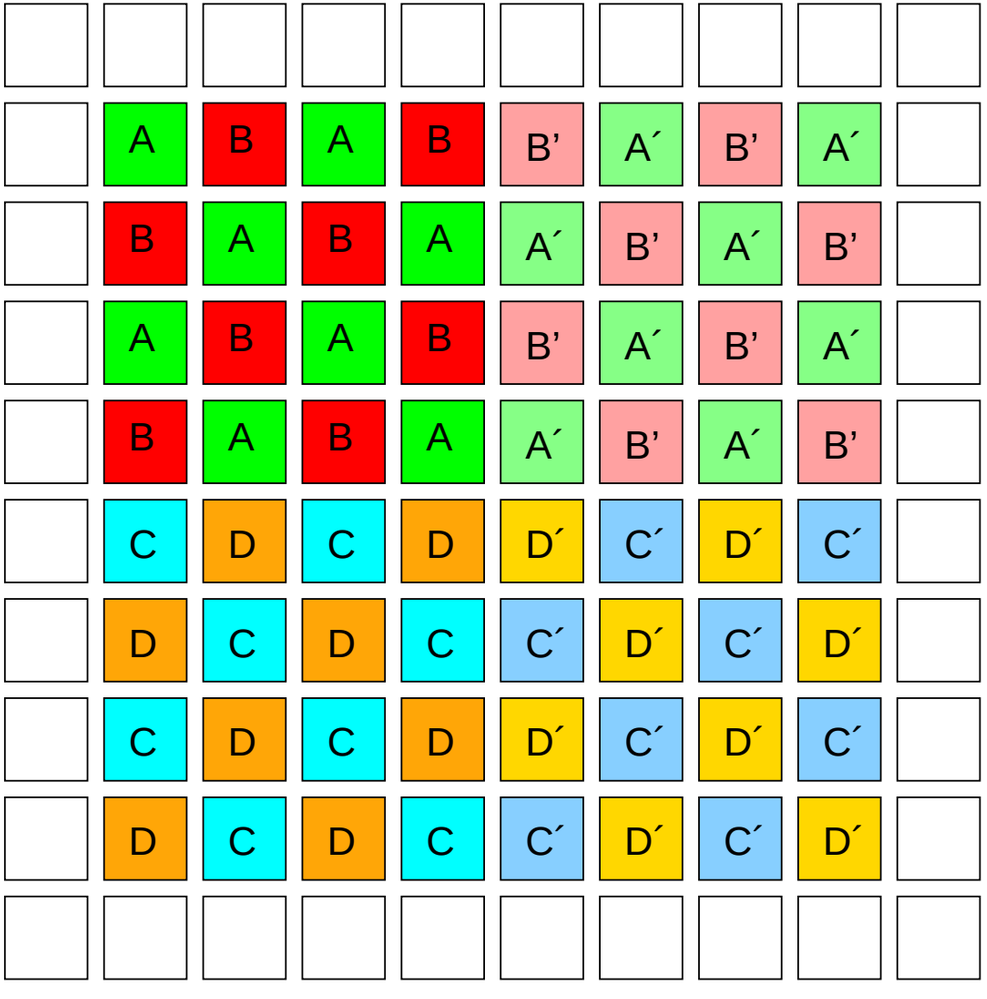
Stage	Cap. load (fF)	Scale factor	Comments
1	1200	1	Reference design
2	400	1/3	-
3-8	300	1/4	-
9	-	-	Flash ADC only

⇨ Things scaled:

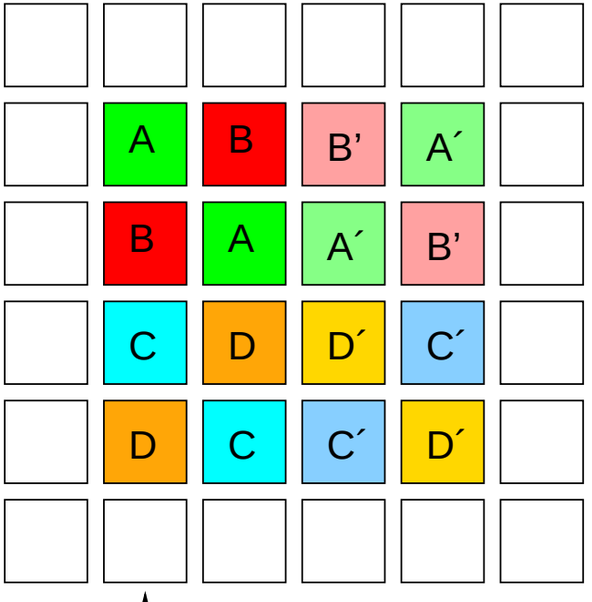
- ✔ Opamp currents, transistors and capacitors.
- ✔ Sampling capacitors.
- ✔ S&H switches and DAC switches.

S&H capacitor layout

First Stage layout

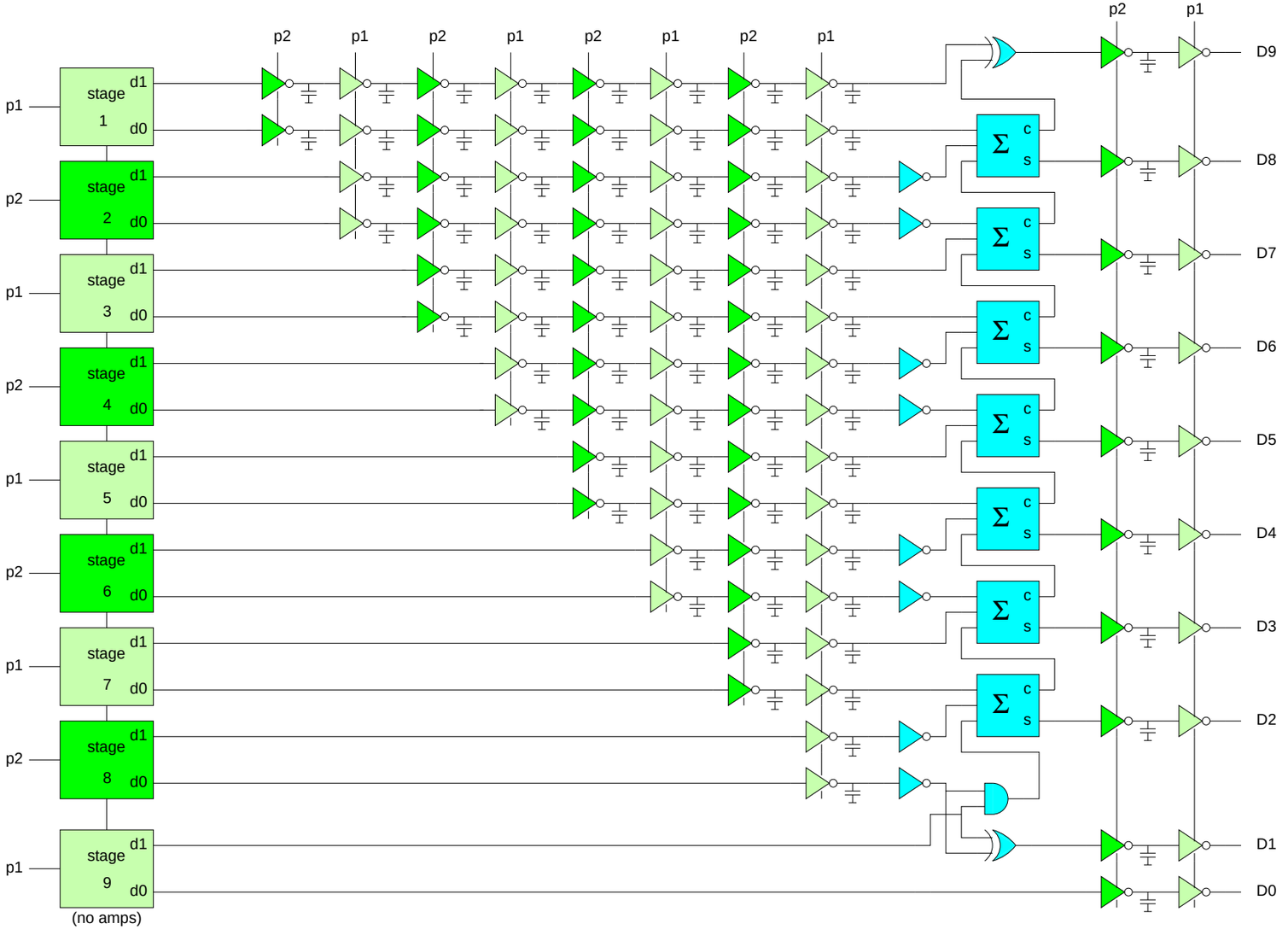


Other stages

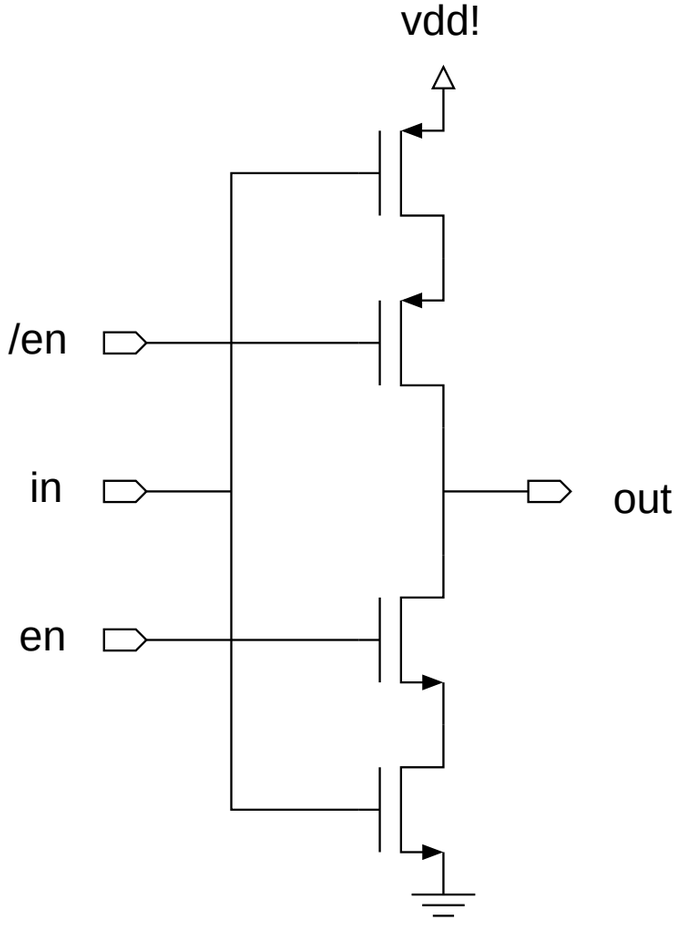


Dummy capacitors used as power supply decoupling.

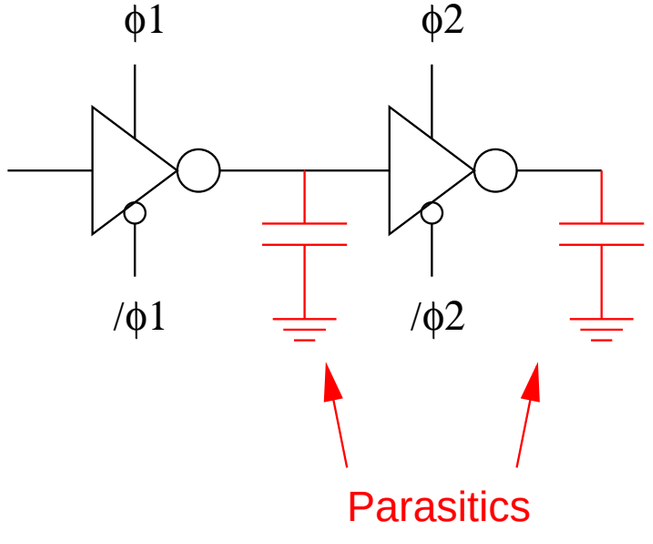
Digital delay & correction logic



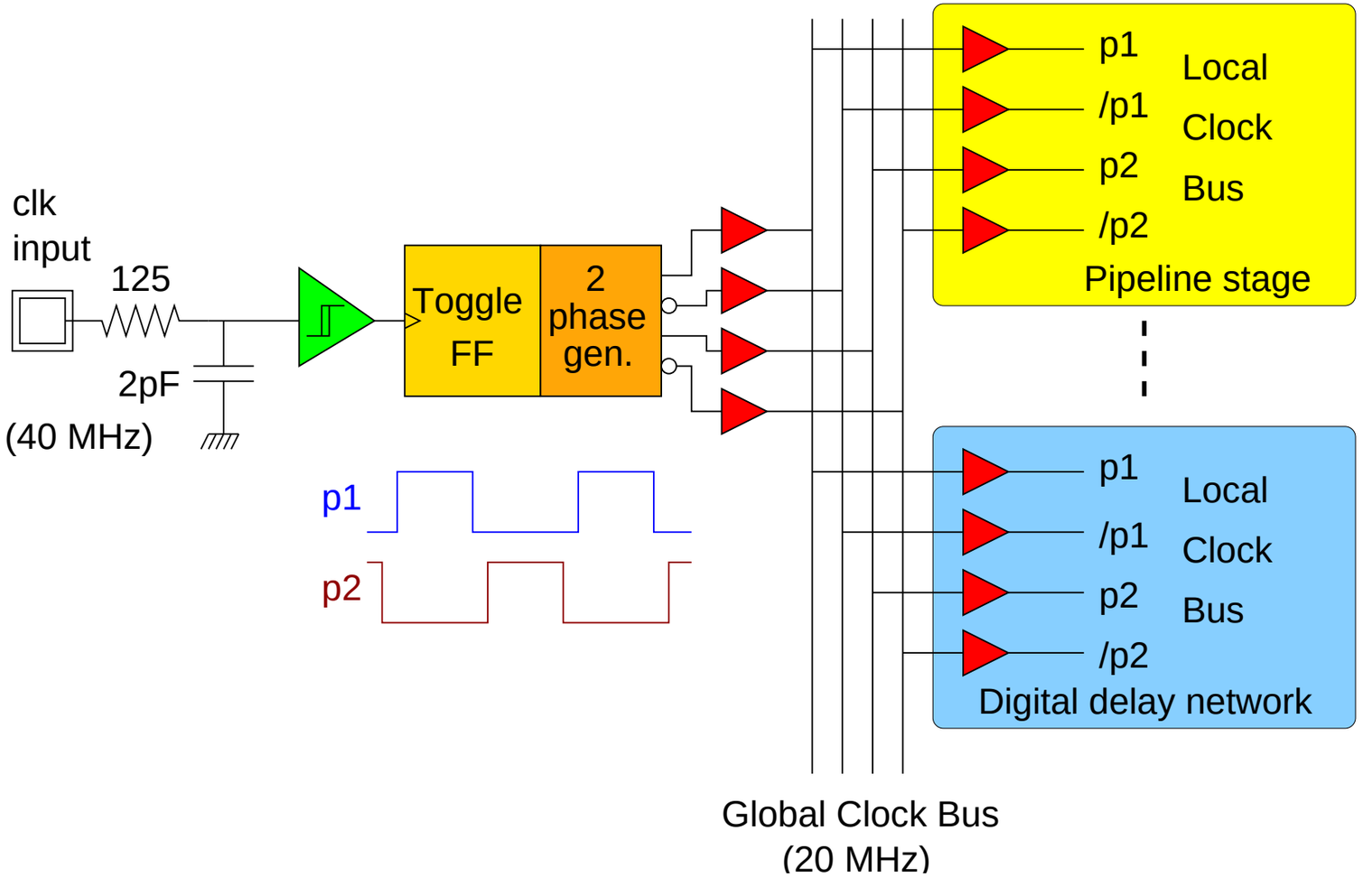
Tristate inverter



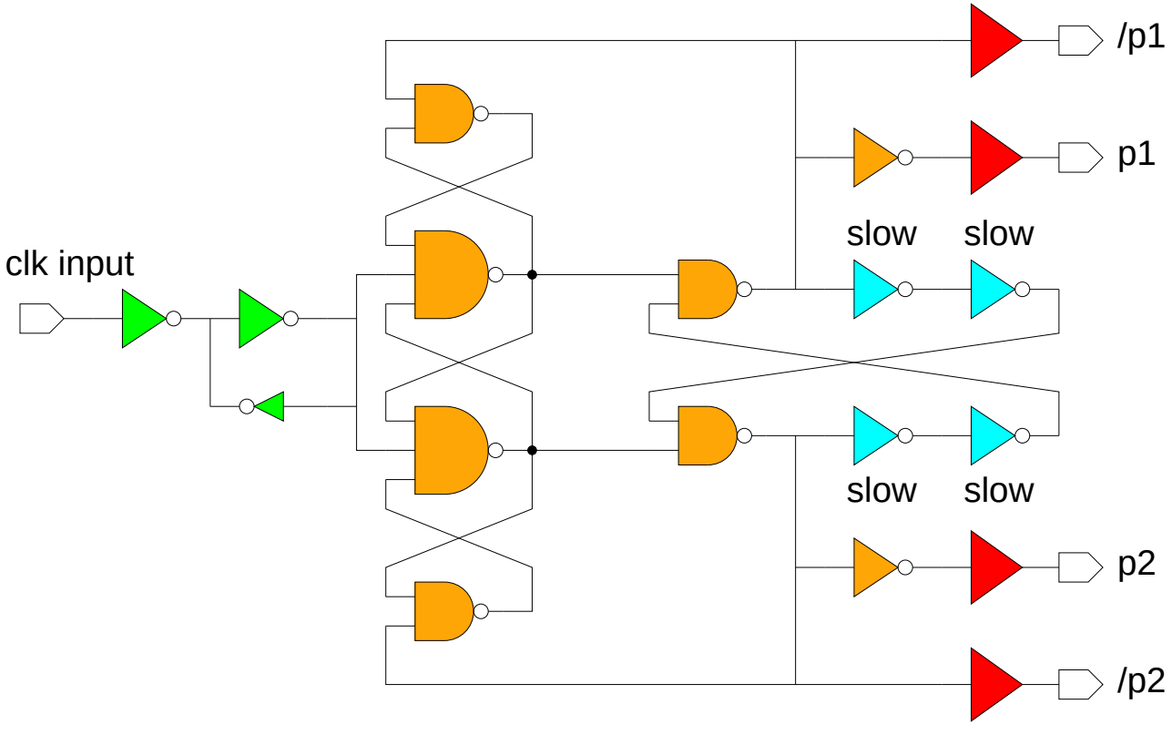
C^{2}MOS Flip−Flop

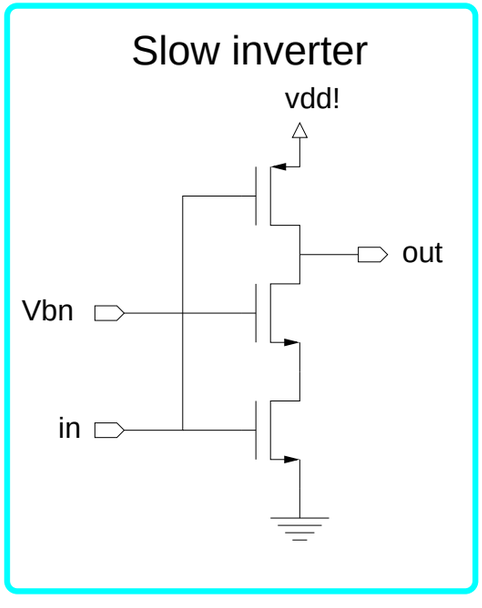


Clock tree

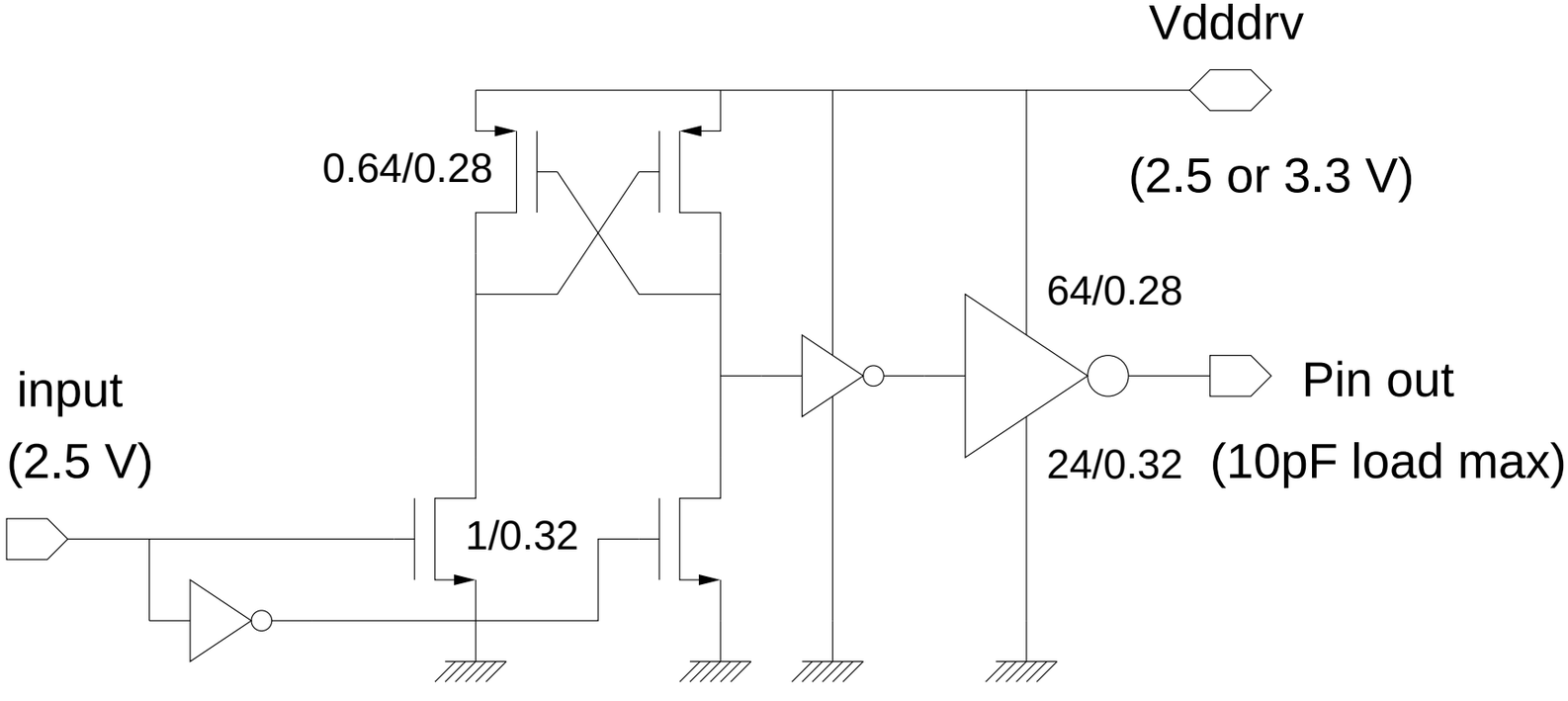

clk
input
125
2pF
(40 MHz)
Toggle
FF
2
phase
gen.
p1
p2
p1
/p1
p2
/p2
Local
Clock
Bus
Pipeline stage
p1
/p1
p2
/p2
Local
Clock
Bus
Digital delay network
Global Clock Bus
(20 MHz)

Clock divider & 2-phase generator

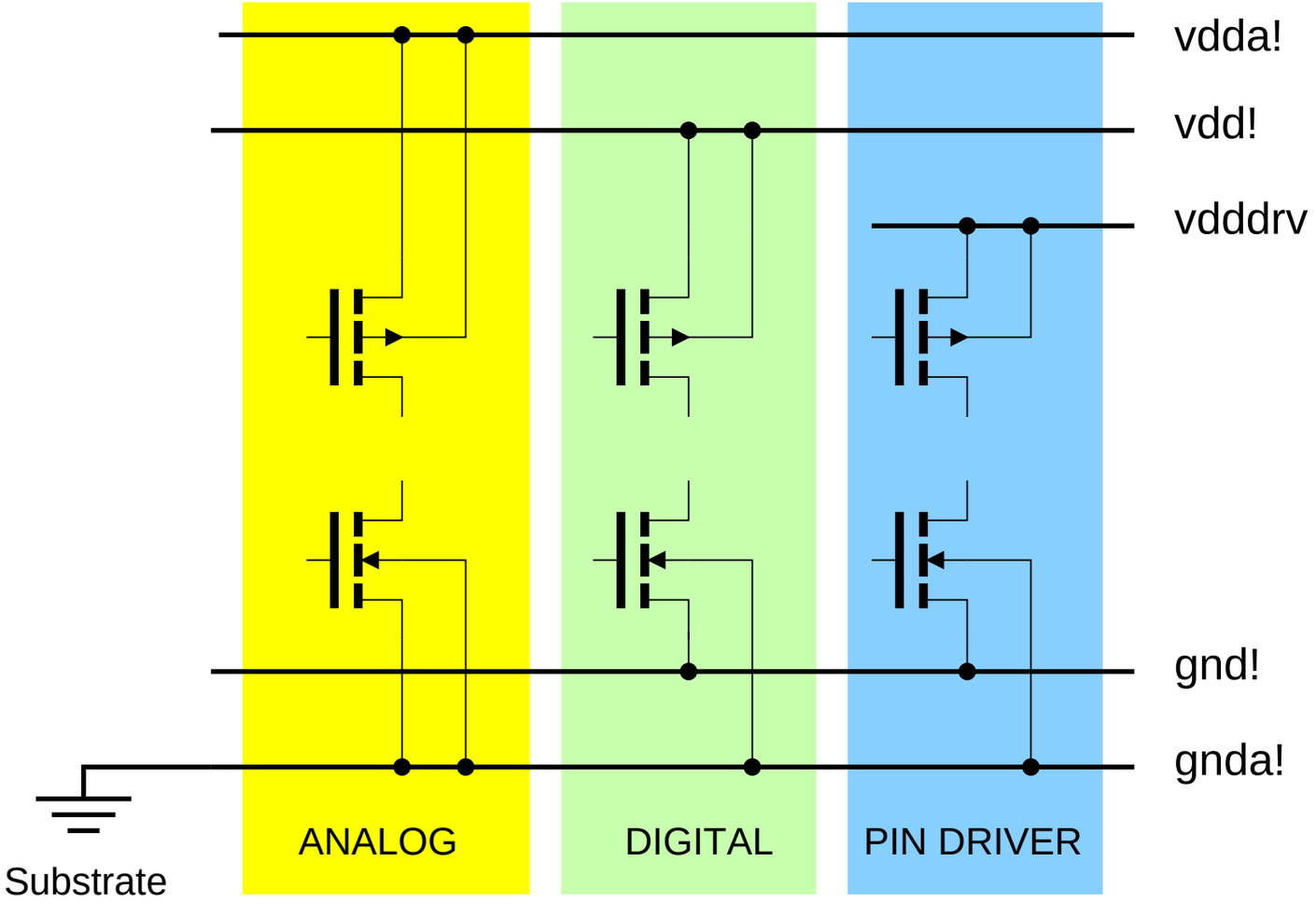




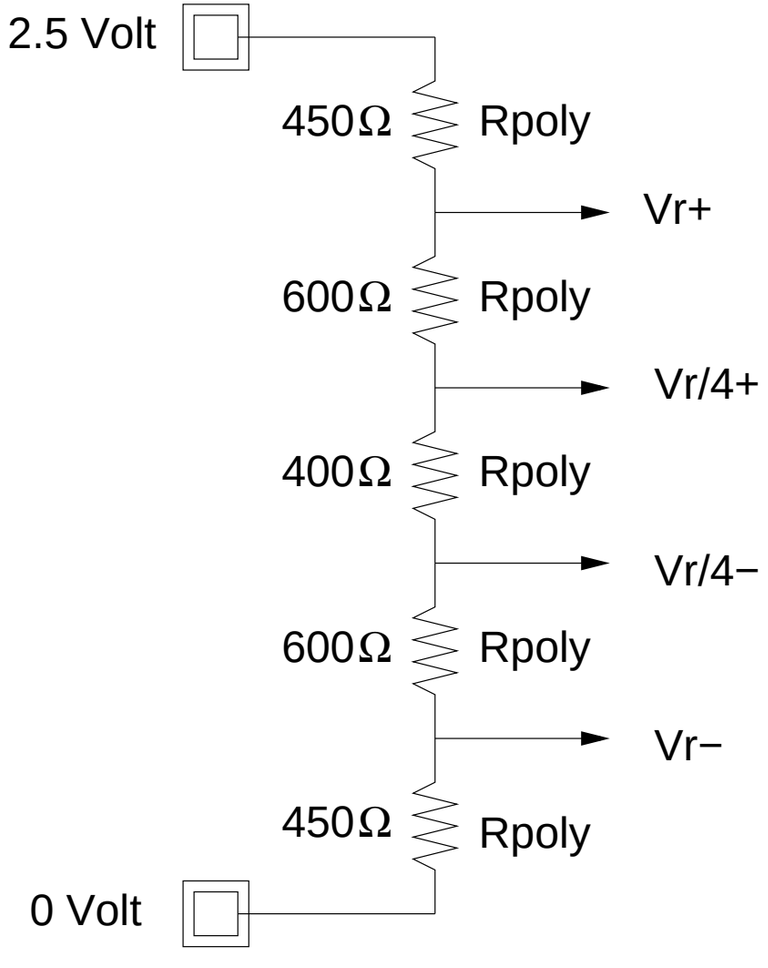
Pin drivers


Vdddrv
(2.5 or 3.3 V)
0.64/0.28
64/0.28
input
(2.5 V)
Pin out
(10pF load max)
24/0.32
1/0.32

Power supply isolation

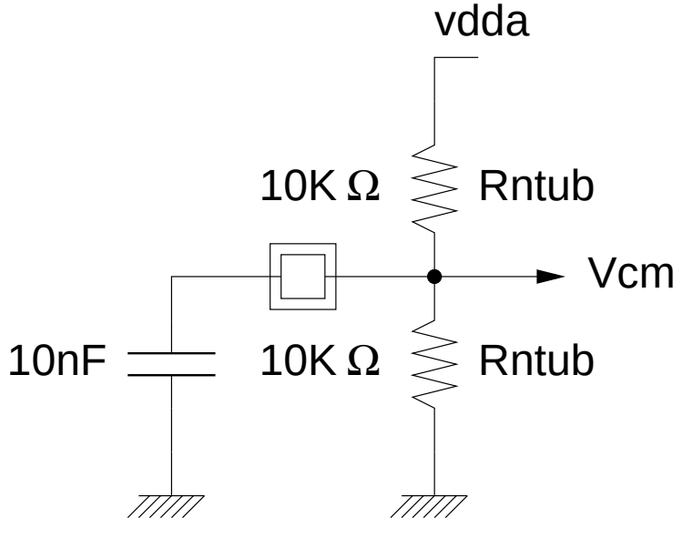


Reference Voltages

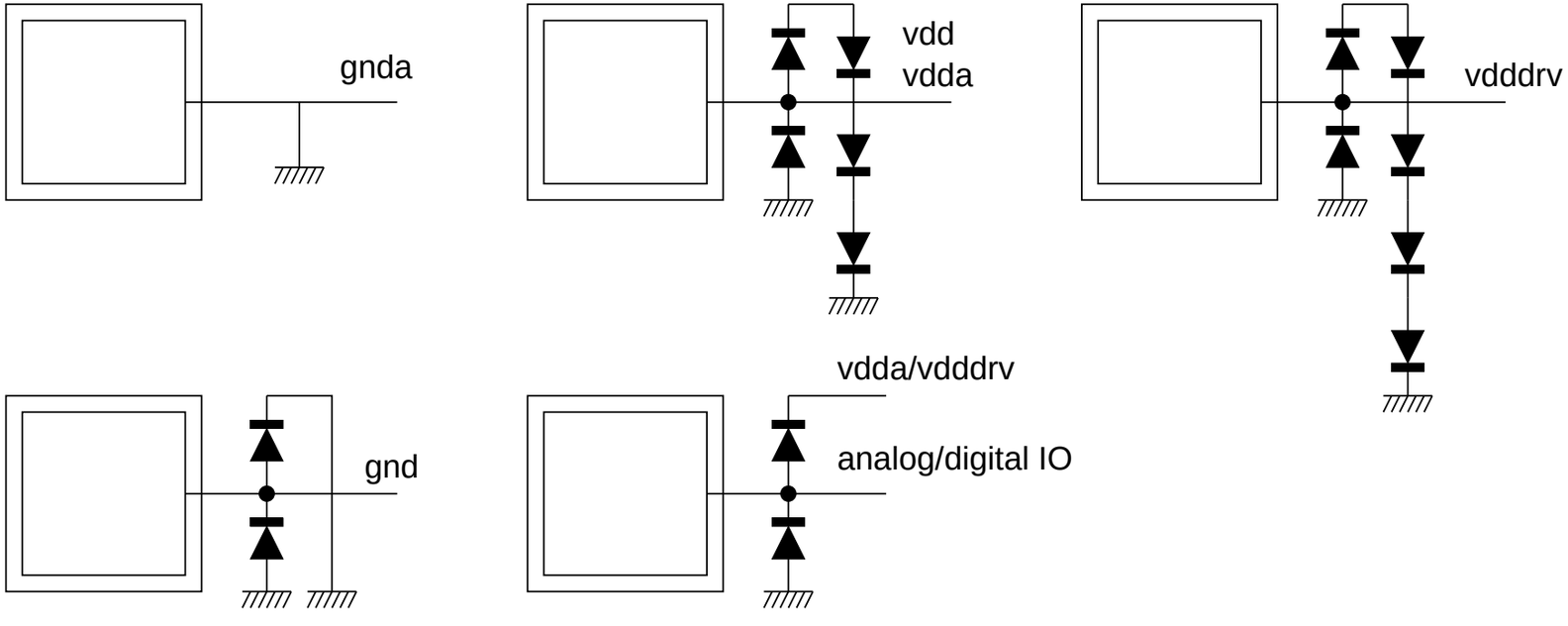


- Short settling time: Small R.
- Power drain: 2.5 mW
- Common−mode reference

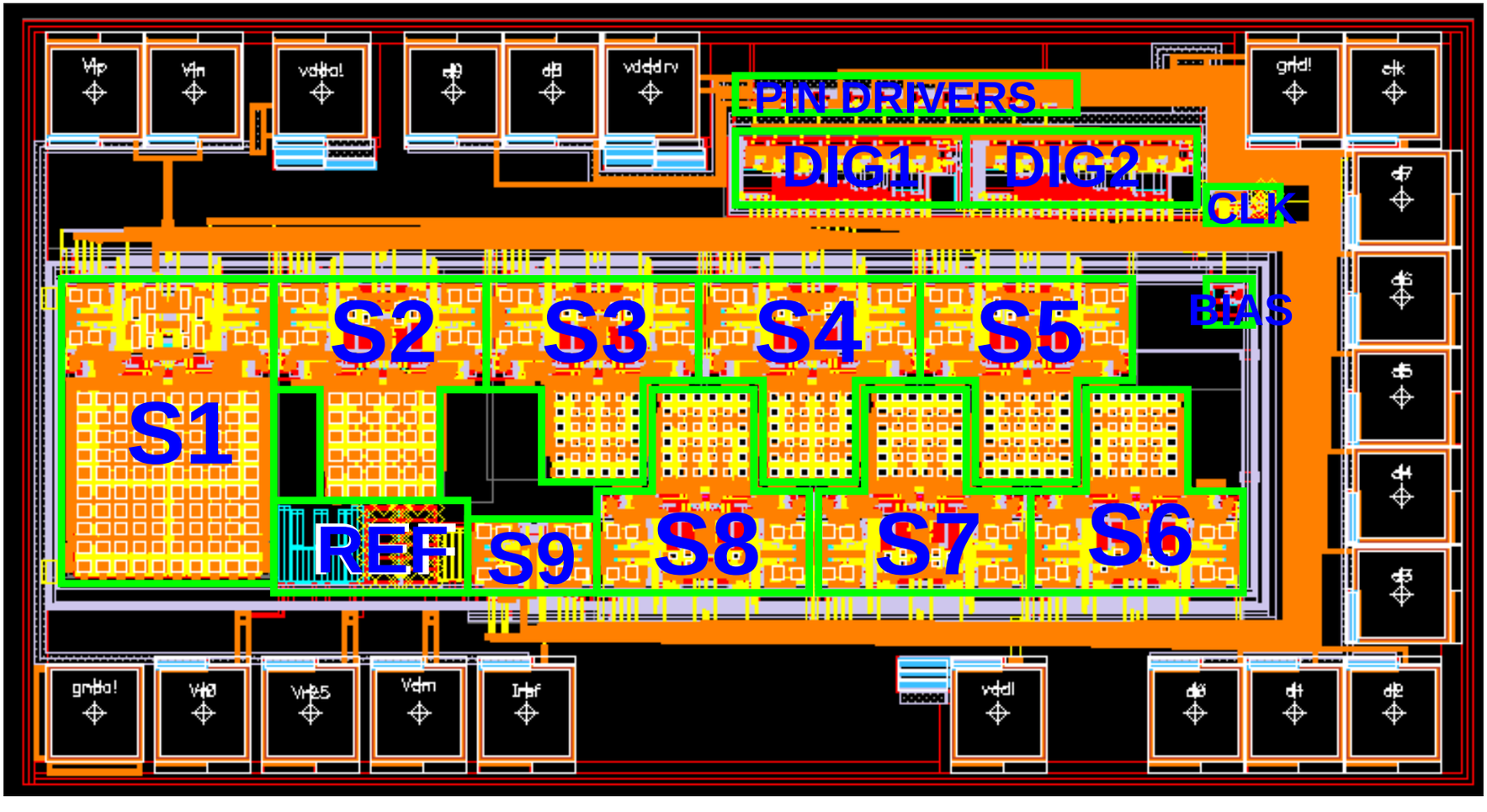
  does not need to be very accurate:
  - Big resistor divider
  - External decoupling capacitor



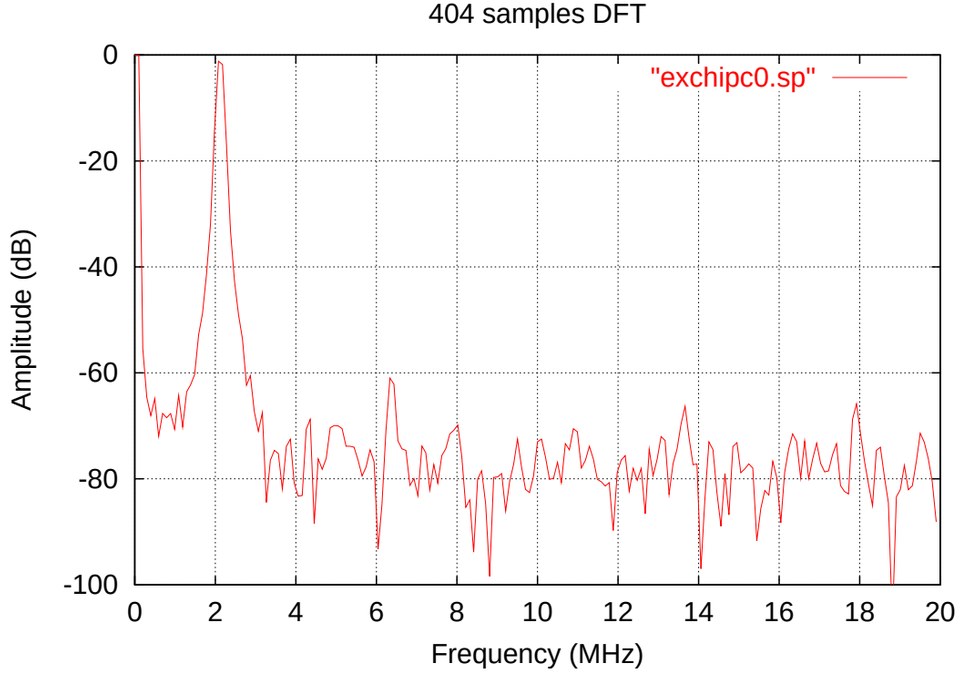
Pads



ADC layout



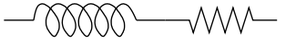
Linearity Simulation



Simulation conditions:

- Fully extracted circuit with parasitic capacitances (~50000 extracted devices)
- Pads & Bonding wires:

3nH 1Ω



ADC performance summary

Parameter	Value
Sampling Rate	40 MHz
Resolution	9.99 bits (1023 codes)
Technology	0.25 μm CMOS
Metal Layers	4
Chip Area (with pads)	1275μm x 670μm (0.85 mm^2)
Pin Count	22
Supply Voltage	2.5 V
3^{rd} Harmonic Distortion	< -60dB
Data Latency	300 ns

Power Bill

Source	Type	Current (mA)	Power (mW)
vdda! (2.5V)	Analog	3.9	9.75
vdd! (2.5V)	Digital. Core	0.7	1.75
ADC (2.5V)	TOTAL	4.6	11.5
Vdddrv (3.3 V) Vdddrv (2.5V)	Digital. Pin drivers (see notes)	3.47 2.57	11.45 6.44

Notes:

- Load capacitance = 10 pF

- Random data modulated OFDM (no guard time), 10 MHz shifted spectrum, full scale input, assumed.

- Bit transition power from pin driver circuit simulation.

To Do

⇨ Empty areas:

- More decoupling capacitors.

- More ground pads.

⇨ Chip completion:

- Antenna check OK.

- General Fill Pattern: Help needed.

⇨ Submission.

⇨ Package selection.

Last modifications

⇨ Dummy capacitors.

✔ Both plates are now connected to ground in order to avoid Vdd noise coupling to signal lines.

⇨ Protection diodes in Vdd pads.

✔ Vdd pads now only include one reverse-biased diode to ground. Forward-biased diode strings are removed because they seem to be not needed.

⇨ Pad spacing increased to 150 μm.

⇨ No pads in chip corners

⇨ Two more analog Vdd and ground pads.

⇨ Big decoupling capacitor for analog power supply added.

More data from simulation.

⇨ Integral non-linearity: 0.38 LSB (nominal corner)

⇨ 20 Ms/s operation @ Iref = 5 μA (nominal Iref = 10 μA)

- ✔ ADC power: 7.125 mW.
- ✔ Non-linearity: 0.3 LSB

⇨ Chip area, with pads: 1500 x 880 μm^2