DESIGN OF A CMOS FULLY DIFFERENTIAL SWITCHED-OPAMP FOR SC CIRCUITS AT VERY LOW POWER SUPPLY VOLTAGES

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Abstract

This paper presents a fully differential opamp desing based on the switched-opamp approach. The common mode feedback of the proposed opamp only works on the output stage in order to allow a fast turn-on. The opamp was designed in a 0.35 μm CMOS technology and is able to operate from a single 1V supply.

1. INTRODUCTION

The demand for circuits operating at very low power supply voltages (i.e., between 1 and 2V) is very high as a consequence of the continuous expansion of the market for portable systems such as wireless communication devices, medical equipment, consumer electronics, and so on. Both the battery-operated systems and the new submicron technologies require the use of a decreased power supply voltage.

The switched capacitor (SC) technique has been proved to be an excellent analogue technique which shows superior features in various applications. However, some difficulties and limitations related to the continuing trend towards lower supply voltage were to be solved because reducing this voltage decreases the overdrive of the MOS switches eventually preventing the switch from being turned on. A review of these problems can be found in Reference [1].

Three solutions to this problem has been proposed in the bibliography. Using an on-chip voltage multiplier [2], [3] or using low V_{th} transistors [4], [5] were initially considered. Nevertheless, the future deep submicron technologies will not sustain the multiplied voltage, whereas the leakage current of low V_{th} transistors is significantly increased causing large harmonic distortion.

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The third alternative was proposed by Crols and Steyaert [6] : this is the switched opamp approach. In this technique, critical switches are eliminated and replaced by opamps which are switched on and off. Bashirotto and Castello [7] further developed the technique by making the circuit fully differential and separating the input and output common mode levels.

The aim of this paper is the design of a switched opamp realized in a 0.35 μm CMOS technology for SC circuits which operates at 1V with an open loop gain higher than 70 dB, unity gain bandwidth (load, 5 pF) of 10 MHz and clocked at 1 MHz. In order to maximize the signal-to-noise ratio, the opamp was designed with an output voltage range from rail-to-rail. To avoid power supply noise a practical switched-opamp circuit has to be fully differential, which requires that a common mode feedback (CMFB) circuit be included in the amplifier. A dynamic CMFB circuit has been used, and in order to ensure fast recovery of the opamp from the high impedance state the CMFB circuit only works on the output stage of the opamp.

Finally, the opamp cell has been used in a filter application and a second-order fully differential biquad bandpass filter for a Radio Data System (RDS) demodulator has been designed.

2. LOW VOLTAGE SWITCHED-OPAMP DESIGN

The opamp core used in this work is a 0.35 μm implementation of the switched opamp proposed by Waltari and Halonen [8] which is based on a folded cascode amplifier with cross-coupled active loads. However, our CMFB circuit was accomplished according to a different approach in order to get a higher performance over a wide temperature and power supply ranges.

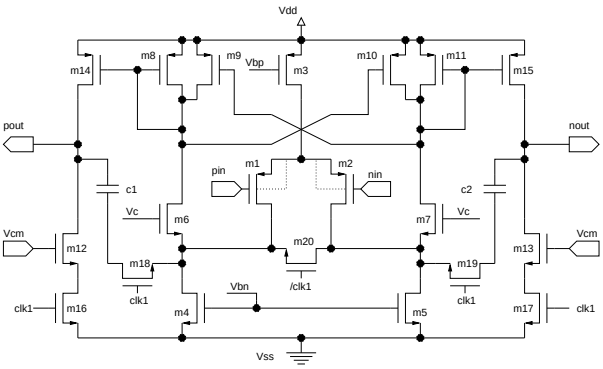

Figure 1: Fully differential switched-opamp core. Refer to Table 1 for device sizes.

The proposed opamp core and the common-mode feedback circuit are shown in Figures 1 and 2, respectively. The corresponding device geometries have been listed in Table 1.

The opamp core is a two stage folded cascode structure with cascode Miller compensation (C_1 and C_2, 1 pF each). The differential input pair is based on P-channel devices (m_1, m_2) and, therefore, the negative supply rail, V_{ss}, is included into the input voltage range. As a consequence, the overdrive of N-MOS switches located at the input of integrator topologies is maximized.

The load of the first stage is composed by four cross-coupled transistors (m_8, m_9, m_{10}, m_{11}). Whereas this load presents a low impedance for common-mode signals ($1/2g_{m8}$), for differential signals the load impedance can be quite high due to g_m cancellation [8]. Thus, the input stage shows a high common-mode rejection ratio.

During the opamp inactive phase, the opamp output is disconnected by using the m_{16} and m_{17} switches. In order to obtain a fast turn-on of the opamp only the output stage is switched off. We must point out that the output nodes does not remain floating during the inactive phase. Instead, the output terminals are connected to V_{DD} through m_{14} and m_{15} that are not switched off. As a consequence, two P-channel switches in the opamp are avoided and, furthermore no external switches are needed to connect the output to V_{DD} .

m_{18} and m_{19} prevent the discharge of the compensation capacitors during the inactive phase, allowing for a fast recovery. m_{20} shorts the differential pair during the inactive phase, avoiding the saturation of the first stage due to the lack of feedback during this phase, and also guaranteeing that m_{14} and m_{15} are both on.

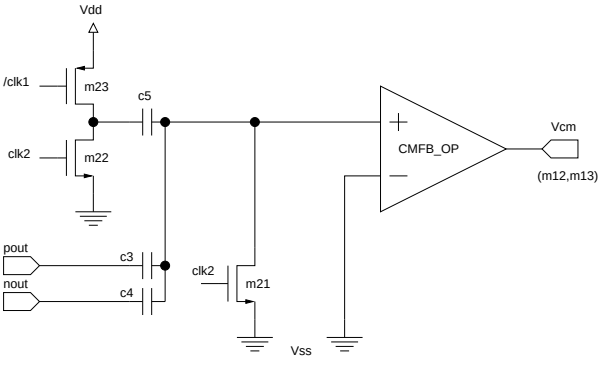

Figure 2: Common mode feedback circuit (CMFB)

Transistor	Size (μm/μm)
m1, m2	25/1
m3	40/1
m4, m5	20/1
m6, m7	100/1
m8, m9, m10, m11	14.2/1
m12, m13	49/1
m14, m15	188/1

Table 1: Transistor sizes.

The minimum power supply voltage is dictated by the m_4, m_6, m_8 device stack, giving:

$$V_{DD} - V_{SS} = V_{thP} + 3V_{DSsat}$$

With a (worst case) P-channel threshold voltage about 700 mV, and operating the devices close to the weak inversion region with saturation voltages estimated at 100 mV, the opamp can work with only 1 Volt supply. On the other hand, a supply independent bias circuit allows for a proper operation at high supply voltages up to the maximum technology limit of 3.3 Volts.

Although the input stage of the opamp has a high common-mode signal rejection, the further signal amplification in the output stage gives an overall common-mode gain that is too high and very sensitive to device mismatching and, then, a common-mode feedback circuit is needed. This circuit must guarantee that the output common-mode signal is about $(V_{DD}+V_{SS})/2$ in order to maximize the output swing. The common-mode feedback only needs to be applied to the output stage because the first stage already has a high CMRR. Thus, the stability of the CMFB circuit can be easily achieved without the use of any sophisticated compensation technique.

Similar to References [1], [7], [8], a switched-capacitor solution for the CMFB circuit has been chosen due to the highly linear features that provides (Figure 2). The use of the switched opamp in SC circuits supports this choice. The circuit includes an averaging capacitive network (C_3 and C_4), a DC shifting capacitor (C_5) and a single-ended feedback opamp. The input stage of this later opamp is based on P-channel devices that allows operation with input voltages close to V_{SS}. A folded cascode structure was used in order to keep the power supply voltage as low as in the main fully-differential opamp. Two 0.26 pF compensation capacitors, not shown in the figure, are included between the input nodes, p_{out} and n_{out} (Figure 2), and an internal opamp node. The compensation capacitors provide stability to the CMFB loop.

This circuit works as follows. During the inactive clock phase of the opamp the capacitors C_3 and C_4 are

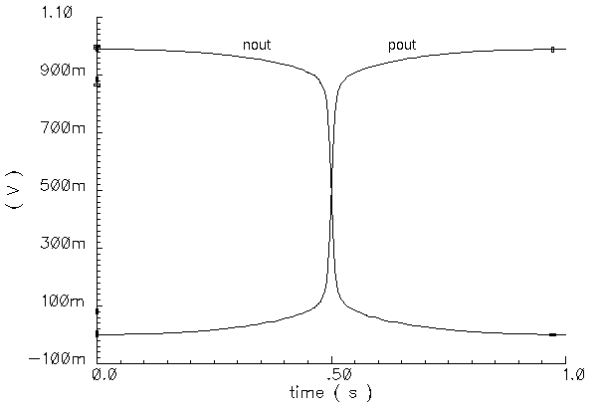

Figure 3: Open loop DC differential transfer characteristic (DC gain $\approx$ 86 dB). The curves correspond to the positive (pout), and negative (nout) output voltages.

precharged up to V_{DD}, and C_5 is discharged down to V_{SS}. During the active phase of the opamp, the negative feedback holds the voltage in the positive input of the CMFB opamp close to V_{SS}. As C_5 is now connected to the positive supply rail, V_{DD}, the charge balance is:

$$(V_{pout} - V_{DD})C_3 \\ +(V_{nout} - V_{DD})C_4 \quad +(V_{DD} - V_{SS})C_5 = 0$$

If the capacitors are selected $C_3 = C_4 = C_5 \equiv C$ (in particular, we have chosen a value of 0.26 pF), it can be obtained:

$$V_{CMO} \equiv (V_{pout} + V_{nout})/2 = (V_{DD} + V_{SS})/2$$

In consequence, the output common-mode voltage, V_{CMO}, corresponds to the desired value. The passive feedback factor is 2/3 that is high enough to yield a fast settling time without a high gain-bandwidth in the CMFB opamp.

3. SIMULATION RESULTS

The switched opamp was simulated with the Spectre program. All the simulations were carried out by using the

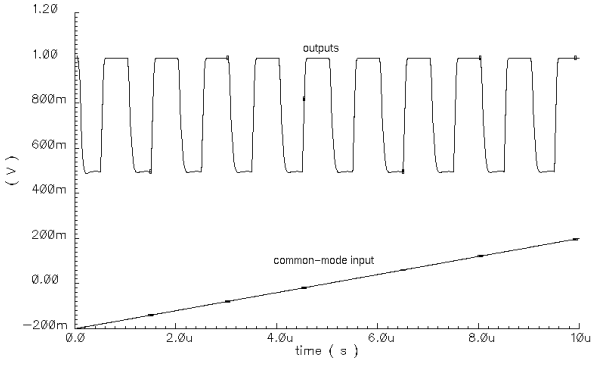

Figure 4: Transient response to a common mode input ramp. During the active phase of the opamp the output remains very close to 500 mV (V_{DD}= 1V).

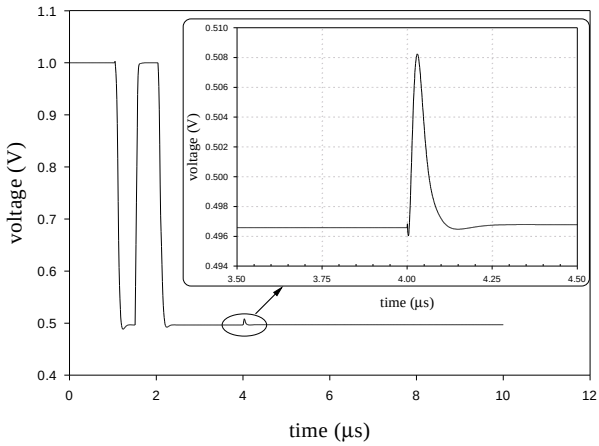

Figure 5: Transient response to a common mode input step (from -200 mV to +200 mV at 4 μs). In the insert, a zoom of the step-induced transient has been included.

extracted circuit from the layout. A load capacitor is taken equivalent to 5 pF. The main opamp characteristics are listed in Table 2.

In Figure 3, the open loop DC differential transfer characteristic is shown. This graph was obtained by applying a slow ramp (2 mV/s) in the differential input and, then, the x-axis is measured in seconds. From the slope of the linear region of the characteristic the DC gain was determined to be about 86 dB. This linear region ranges from 100 mV to 900 mV as corresponds to rail-to-rail output opamps.

Next, the response of the CMFB circuit has been tested and the results are included in the following two figures. In Figure 4, in spite of the ramp in the common mode voltage applied to the input no change in the opamp response during its active phase can be observed. This level is very close to 500 mV. In Figure 5, a step from -200 mV to +200 mV at 4 μs has been applied to the input. In the Figure insert, the step-induced transient is shown. As can be seen, this transient is extinguished in less than 250 ns. According to these results, it can be concluded that just one clock cycle is needed in order to stabilize the common mode output.

Finally, Figure 6 shows the output voltage of the opamp in a closed-loop inverter configuration (gain= -1). A 200 mV step was applied as input differential voltage. From this graph, the slew rate -both for the up and down transitions- can be calculated. In our opamp, both slew rates were quite similar and its corresponding values are included in Table 2. From this Figure, the slew rate time plus the settling time was determined to be around 155 ns, remaining below our maximum design limit (450 ns). In fact, the maximum sampling rate is determined by the opamp switching time which was estimated below 250 ns.

Currently, the fabrication of the designed switched opamp is in progress.

Finally, the opamp cell has been used in a filter application. A second order fully differential biquad band-

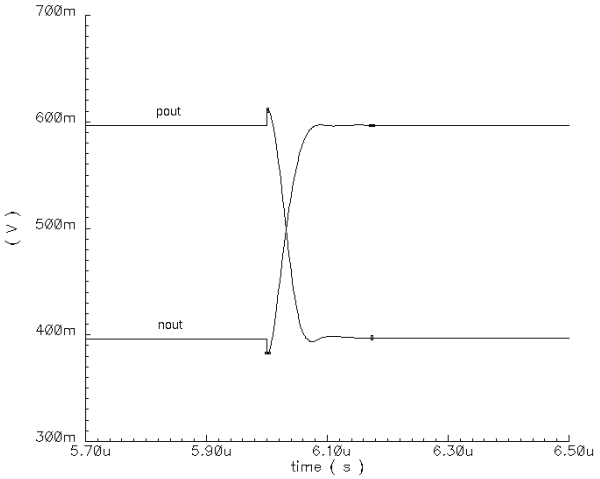

Figure 6: Transient response to a 200 mV differential input step. The opamp is disposed in a closed loop inverter configuration (gain = -1).

pass filter for a radio data system (RDS) demodulator has been designed in order to test the opamp capabilities under real working conditions. The specifications for this filter were the following: center frequency, 58 kHz; quality factor, Q, 20; and, gain, 20 dB. The corresponding simulation results obtained from the extracted opamp were, respectively, 58.002 kHz; 20.0007; and, 20.6 dB. It can be pointed out that these results are very similar to the initial specifications.

4. CONCLUSIONS

In this paper, a switched-opamp realized in a 0.35 μm CMOS technology for SC circuits which operates at 1V with an open loop gain higher than 70 dB, unity gain bandwidth of 10 MHz with a 5 pF capacitive load, and clocked at 1 MHz has been designed.

This opamp has a fully differential topology with a switched-capacitor common mode feedback that only operates on the output stage. In order to maximize the dynamic range the opamp provides a rail-to-rail output and an input voltage range that includes the negative supply rail.

Parameter	**Value**
Technology	0.35 μm CMOS
Power supply	1 V$\rightarrow$3.3 V
Power consumption	90 μW @ 1 V
Sampling frequency	1 MHz
Input voltage range	-500 mV$\rightarrow$+160 mV
GBW	12.8 MHz
Open loop gain	85.8 dB
CMRR	128 dB
SR_{up}	4.6 V/μs
SR_{down}	5 V/μs
Phase margin	45°
Cell area	0.02 mm^2

Table 2: Opamp performance obtained from the extracted circuit simulation. The load capacitor is taken equivalent to 5 pF.

The opamp was simulated with the Spectre program by using the extracted circuit from the layout. The results agree with the initial specifications.

Currently, the fabrication of the designed switched opamp, and a second order fully differential biquad band-pass filter based on the previous opamp are in progress.

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