Jitter effect comparison on continuous-time sigma-delta modulators with different feedback signal shapes

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ABSTRACT

A comparison is presented for three different feedback signal shapes on a current mode continuous-time second order sigma-delta modulator, although, it can be extended to systems of any order. The three shapes are: rectangular, exponential, and a new mixed waveform whose pulse starts being rectangular and after a fraction of the clock period changes to decaying ramp. Simulation results at system level, using a software model, are presented. Results show that using early return to zero feedback signal shapes (exponential, mixed) the modulator performance degradation due to pulse width variation is reduced with respect to rectangular signal shapes. In addition to that, the new mixed shaped do not present the high signal peak that the exponential does. This is important from the point of view of integrator input stage because it allows power saving as well as critical input noise reduction.

Keywords: Sigma-delta, continuous-time, current-mode, jitter

1. INTRODUCTION

Applications in the communications market are continuously demanding higher bandwidth and resolution, and many works have already proved that continuous-time (CT) sigma-delta modulators are a good choice to achieve it. One of the more important drawbacks is their sensitivity to clock jitter. This jitter affects directly to the amount of signal that is fed back, and the sensitivity is even higher if Return-to-Zero (RZ) signals are used[1]. Thus, for high speed and/or high accuracy converters, this represents a serious challenge to chip designers.

Another drawback is the excess loop delay[2] which is related to the non-instantaneous response of the quantizer. In order to overcome this problem, Return-to-Zero or Half-Delayed Return-to-Zero (HRZ) feedback signals have been proposed, instead of the traditional Nonreturn-to Zero (NRZ) signal[1].

To reduce the effect of clock jitter in CT sigma-delta modulators non-rectangular feedback signals can be used. In particular, a decaying ramp and a decaying exponential signal were theoretically considered by Aboushady[3] and a cosine pulse by Luschas[4]. Arbitrary feedback waveforms have also been considered theoretically[5]. A circuit with decaying exponential signals has been implemented by Van Veldhoven[6] and Ortmanns[7].

This paper presents a comparison of modulator performance for 3 different types of feedback signals in presence of clock jitter. Namely, HRZ rectangular signal, HRZ exponential and a new RZ shaped signal that we call Rect-Ramp signal.

The chosen architecture of the modulator used for the comparison is shown in Sec. 2 and the considerations relative to jitter are detailed in Sec. 3. System Simulations (using a software model) are presented in Sec. 4, and a specific circuit implementation is presented in Sec. 5.

2. SYSTEM ARCHITECTURE

A second order sigma-delta modulator with single bit feedback signal has been proposed. This architecture is shown in Fig. 1. Different signal shapes, obtained from different DAC circuits, have been used in order to compare the overall behavior of the modulator from the point of view of jitter. More precisely jitter in the duration of the DAC pulse. A more extensive discussion of jitter is given in Sec. 3.

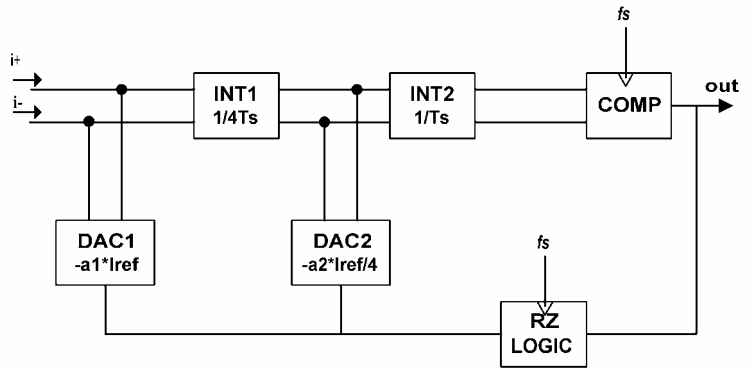


Figure 1: Blocks diagram for second-order continuous-time current-mode ΣΔ modulator.

The modulator has been designed to work with differential input signals in current mode. The target was to achieve above 60 dB of resolution, a signal bandwidth of 1MHz with an OSR of 64, thus the sampling frequency is 128 MHz. The maximum allowable input signal (reference current, Iref) is 25 μA.

Originally the gain of the two integrators was considered to be 1 but in order to reduce the power consumption a modified structure was considered introducing a gain factor of 1/4 in the last integrator. Reorganizing this gain factor over the rest of the circuit leads to a gain coefficient of 1 for the second integrator and a gain coefficient of 1/4 for the first integrator. The DAC coefficients are also affected by this reorganization and the final scaled coefficients are: a1_scl = a1 for DAC1, and a2_scl = a2/4 for DAC2.

DAC blocks will be different for each type of signal used, and so will be the DAC coefficients. The process followed to obtain the coefficients consists of the following stages: First of all, the DAC signal expression in the time domain of the continuous-time system was obtained. The expression in the time domain was converted into its correspondent frequency expression by applying the Laplace transform. Then, the loop gain transfer function was calculated. Finally, the modified-Z-transform method was used in order to obtain the loop gain transfer function in the Z domain[8]. This expression is matched to that of a discrete-time system of the same order, and from that comparison DACs coefficients are deduced.

Following the previous process of calculus for each different DAC signal, the DAC coefficients were obtained as a function of some intrinsic parameters of the signal shape.

In the case of RZ rectangular DAC signals (Fig. 2a), the specific shape parameters are the pulse delay with respect to the sampling instant (td) and the pulse width (W). T is the clock period, a1 and a2 are the DAC coefficients and Iref is the reference current. The expression obtained for the coefficients agree with the results found by Aboushady[8] and can be expressed as:

$$a1 = -\frac{T}{W} \tag{1}$$

$$a2 = -\left(\frac{1}{2} + \frac{T}{W} + \frac{td}{W}\right) \tag{2}$$

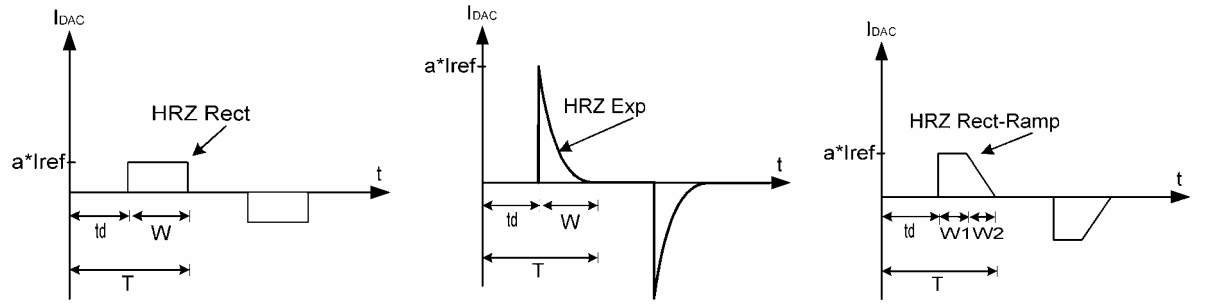
HRZ rectangular signals have been used for the present paper, which imply td=T/2 and W=T/2 and it leads to a1=-2 and a2=-3.5

When HRZ exponential DAC signals are used (Fig. 2b), the parameters are the time constant (τ), pulse delay and clock period. Considering T >> τ, the expressions can be approximated by:

$$a1 = -\frac{T}{\tau} \tag{3}$$

$$a2 = -\left(1 + \frac{T}{\tau} + \frac{td}{\tau}\right) \tag{4}$$

td=T/2 and τ=T/10 have been used for exponential DACs. It results in a1=-10 and a2=-16.



(a) (b) (c)

Figure 2: (a) HRZ rectangular DAC signal. (b) HRZ exponential DAC signal. (c) HRZ rect-ramp DAC signal.

The last of the three signal shapes considered is the Rect-Ramp signal, whose name comes from the fact that it is a mixture of rectangular and ramp signals (Fig. 2c). The parameters of this shape are the pulse delay, clock period, rectangular pulse width (W1) and ramp pulse width (W2). The resulting expressions are the following:

$$a1 = -\frac{-1}{\frac{W_1}{T} + \frac{1}{2}\left(\frac{W_2}{T} + \frac{2(td + W_1)}{T} - 3\right) + 1.5 - \frac{td + W_1}{T}} \tag{5}$$

$$a2 = -\frac{-\left(2T + \frac{a1}{T^2}\left(W_1\left(-\frac{W_1}{2} - td + T\right) + W_2\left(\frac{T}{2} - \frac{td + W_1}{2} - \frac{1}{6}\right) + \frac{T^2}{6} - \frac{(td + W_1)T}{3} + \frac{(td + W_1)^2}{6}\right)\right)}{W_1 + \frac{W_2}{2}} \tag{6}$$

When td=T/2, W1=T/4 and W2=T/4 the coefficients are a1= -2.6 and a2=-4.5.

3. JITTER CONSIDERATIONS

To study the effect of clock jitter in our circuit, Fig. 3 shows a period of the clock signal. Every period has two edges and both may suffer from uncertainty, that is, the time instant when they happen is not fixed. The time uncertainty of edge occurrence for this type of clock can be modelled as two different sources of noise[1]: random noise (causing independent jitter) and clock phase noise (causing accumulative jitter).

Independent jitter corresponds to the noise component which models the part of uncertainty that is completely independent of that suffered by previous edges. This type of noise is modelled as a random process which adds white noise to the output spectrum in the signal band when the input signal is sampled.

On the other hand, accumulative jitter corresponds to the noise component which models the part of uncertainty that depends on previous edges position. This type of noise adds non-white skirts to the output spectrum at both sides of the sampled input tone. Accumulative jitter is usually about two orders of magnitude below independent jitter.

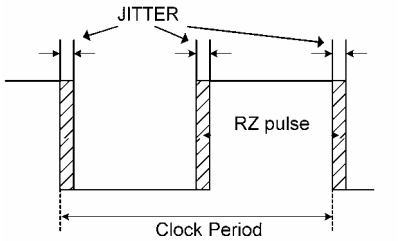


Figure 3: Clock signal and edge uncertainty.

The total clock noise due to edge uncertainty will be the sum of random noise and clock phase noise[9]. This is expressed as:

$$\sigma^2_{total} = \sigma^2_{acc} + \sigma^2_{ind} \tag{7}$$

Where σ is the standard deviation of jitter. Accumulative clock jitter (σ_{acc}) can be calculated as follows[9]:

$$\sigma_{acc} = \frac{f_{off} \cdot 10^{\frac{nph}{20}}}{f^{1.5}_{clk}} \tag{8}$$

Where nph is the phase noise, measured at a frequency offset (f_{off}) from the carrier (f_{clk}). It is usually normalized to 1 Hz-bandwidth resulting in a 1 dBc/Hz unit.

In a CT sigma-delta modulator clock noise has two fundamental consequences. One of them is related to the sampling instant. The modulator is a sampled circuit and the sampling instant is affected by the total clock noise, with both accumulative and independent contributions. The other consequence is related to the width of RZ pulse (see Fig. 2). A variation on the pulse-width causes a variation in the amount of charge that the feedback signals are able to pump into the integrators. Pulse-width uncertainty is the edge-to-edge jitter, and it corresponds to the independent contribution because the accumulated jitter will be practically the same for both edges so its contribution is not considered. Pulse-width uncertainty will be referred as *JitterW* and includes the uncertainty in the two edges that define the pulse width.

Only pulse width uncertainty has been considered for the comparison carried out in this paper because the sampling instant uncertainty affects equally to the three modulators, regardless the type of DAC signal.

4. SYSTEM SIMULATIONS

A software model has been developed to run fast simulations before going into circuit implementations and lengthy simulations. The model also allows the possibility of quick changes making the circuit debugging and refinement processes easier and shorter.

C++ language and *SystemC* libraries have been used to develop the model. *System*C is a discrete time *C++* oriented set of libraries that allows the implementation of a software model behaving as a real circuit. Software is inherently sequential but, for discrete time circuits, *SystemC* kernel allows different blocks of an electronic system to communicate as if they where working in parallel. In our design integrators are continuous time blocks, so to overcome this drawback they have been simulated as discrete time circuits with a time step much smaller than the sampling period used, namely T/64. The results obtained through this approach have proved to match quite accurately with those obtained from circuit simulation using Spectre.

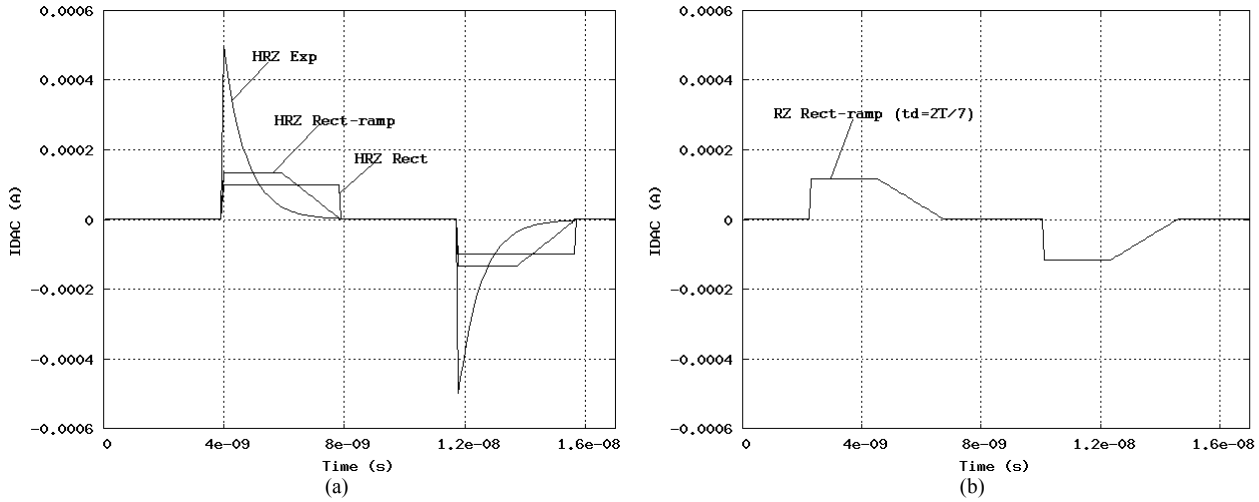
Integrators present current mode input and output. The impedances in the model have been considered to be zero at the input and very high at the output.

DACs implement the signal shapes with the corresponding coefficients detailed in Sec. 2.

The quantizer in the software model is considered to behave ideally. In addition, RZ feedback signals[1] have been used, thus, there is not necessity for including excess loop delay effects.

Neither thermal nor flicker noise have been considered and only independent jitter, which affects the pulse width uncertainty (JitterW), has been included. This allows establishing a direct relation between the simulation results for different values of JitterW and the different feedback signal shapes.

Fig. 4 shows the signal shapes used and Fig. 5 the modulator simulation results, signal-to-noise-ratio (SNR) versus the pulse width uncertainty (JitterW), for each of them.



(a) (b)

Figure 4: All signal shapes have been generated with the software model. The value of the reference current is 25 μA. (a) DAC signals for HRZ rectangular, HRZ exponential and HRZ rect-ramp cases. (b) DAC signal for RZ rect-ramp with td=2T/7.

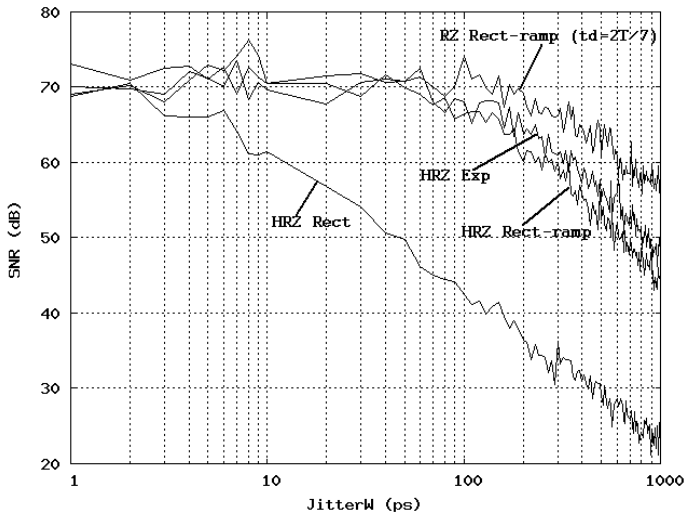


Figure 5: Effect of JitterW on the SNR of the proposed second order modulator for different DAC signal shapes. The four graphs correspond to a HRZ rectangular DAC signal, a HRZ exponential, HRZ rect-ramp and a RZ rect-ramp with td=2T/7. The input signal has been set to 0.5*Iref for all simulations.

The graph representing the simulations for the HRZ rectangular feedback signals confirms that the modulator performance is very sensitive to pulse width uncertainty when rectangular feedback signals are used. The SNR decreases monotonically with JitterW.

To avoid the problem of being limited to very low, and at the same time unreal values of JitterW, or to very modest SNR results, some other signal shapes can be used. Some papers[6,7] have already proved the advantages of using exponential feedback signals instead of rectangular. It can also be verified from the graph of HRZ exponential feedback signals of Fig. 5. However, the current peak of the HRZ exponential signal, Fig. 4a, is 4 times higher than that of the HRZ rectangular. This current peak forces the integrators to manage an instantaneous current 4 times greater, and it leads to a higher value of integrators power consumption. Higher values of thermal and flicker noise referred to the signal input are also expectable due to the resizing of integrators.

Considering all the arguments exposed so far, we propose the use of a new shaped signal that to our knowledge has not yet been used. This new shape that we have called rect-ramp was detailed in Sec. 2. Considering that the values of this signal near the end of the pulse are higher than those of the exponential signal (Fig. 4a), it can be expected that JitterW affects more severely to the SNR in this case. This result is also observable in Fig. 5. The graph HRZ rect-ramp shows that, even though the modulator performance in presence of JitterW is not as good as for the exponential case, it is still very robust to JitterW. In addition the current peak is considerably smaller.

To extend the insensitivity to JitterW even further, without degrading the power consumption figure, we propose the use of the rect-ramp signal shape with a pulse delay of 2T/7 instead of T/2 and W1=W2=2T/7 instead of T/4 (see Fig. 4b). Since the pulse ends T/7 before the period, it could be expected that for JitterW values smaller than (T/7)/1.73≈640ps (considering JitterW has rectangular distribution) the modulator SNR is not affected. In Fig. 5 can be appreciated that the simulation results for this last shape are better than any of the previously considered. Nonetheless, SNR is affected for JitterW values much smaller than expected. This is because clock independent noise in general and pulse width uncertainty in particular also affects the integration length and the time when the fed back signal is received. This is a second order effect and is appreciated only when the effect on the DAC signal shape is negligible.

A pure ramp signal shape could also be used, but from the point of view of JitterW, similar results of those of rect-ramp signal can be expected. Apart from that, the current peak would be greater and so would be the power consumption.

5. CIRCUIT IMPLEMENTATION

The modulator has been designed by using a 0.35 μm CMOS technology provided by AMS with a supply voltage of 2.5 V. Next, the implementation of the different blocks of the modulator will be considered.

The integrator is based on a differential architecture consisting of a folded-cascode topology (Fig. 6).

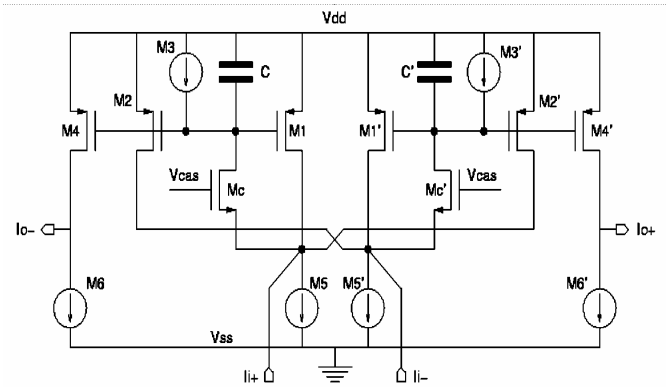


Figure 6: Circuit implementation of integrators. Input nodes common mode voltage is 1V. Integration capacitors have a value of 3.9pF for the first integrator and 1.95pF for the second.

The circuit of Fig. 6 provides both high gain and low-power consumption. Due to the current mode approach, the required low input impedance (in this case a few hundred of ohms) is achieved by using the appropriate cascode transistors. This configuration avoids the necessity of using an operational amplifier with feedback to achieve the required low input impedance. This last strategy was used by Van Veldhoven[6]. The circuit has been implemented to work properly with a maximum allowable input signal (reference current, Iref) of 25 μA.

Fig. 7 shows the comparator's circuit implementation. A differential architecture with current input and voltage output has been used. It is composed of three different stages: preamplifier, clocked regenerative latch and C^2MOS dynamic output latches. Preamplifier has been sized to be able to manage the maximum output current of the second integrator.

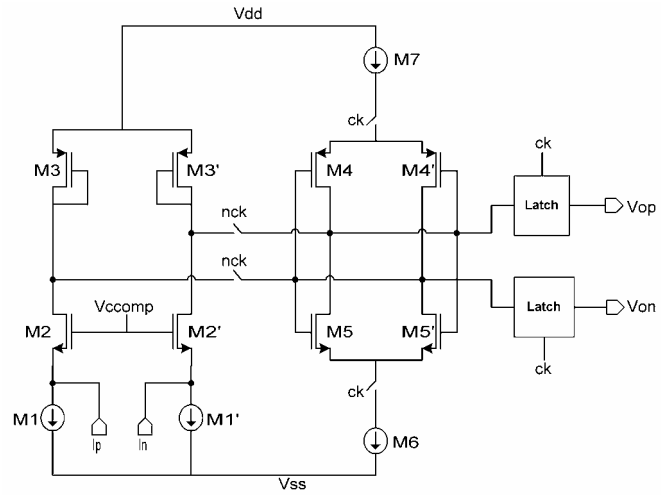


Figure 7: Circuit implementation of the regenerative comparator.

Since DAC circuit for the generation of HRZ rectangular signal are very well known, only DAC circuits for HRZ exponential and for rect-ramp signals (with td=T*2/7) have been implemented.

Fig. 8a shows the circuit that generates a differential HRZ exponential feedback signal. Its operation is as follows. First, the capacitor is precharged to the reference voltages. Next, the capacitor is connected to the output nodes, which are selected according to the logic circuit (clock phases, rzp and rzn). Then, the capacitor discharges and generates a positive and a negative current pulse whose integration corresponds to the charge accumulated during the precharge phase. The peak current of the exponential waveform has a value of:

$$I_{peak} = Iref \cdot a_i \_ scl \tag{9}$$

Where a_i_scl (i=1,2) is the corresponding scaled DAC coefficient.

The circuit-generated signal and the one obtained from the software model are depicted in Fig. 8b. Both are in differential mode.

A possible circuit implementation to obtain a fully differential rect-ramp signal is given in Fig. 9. It presents two phases. First the capacitors are pre-charged and the outputs are disconnected. Then the capacitors are dis-charged through a constant current source and the capacitor voltage is connected to the cascode transistors subscripted as 1. The cited transistors drive their gate voltage changes to changes in their source voltage to keep the same level of current flow. While transistor subscripted as 2, work in saturation the outputs current will be constant with a value equal to Mn2 and Mp2 saturation currents. After a period of time, Mn2 and Mp2 transistors will enter the triode region, generating a decreasing ramp output current. The output nodes are selected according to the logic circuit clock phases, rzp and rzn.

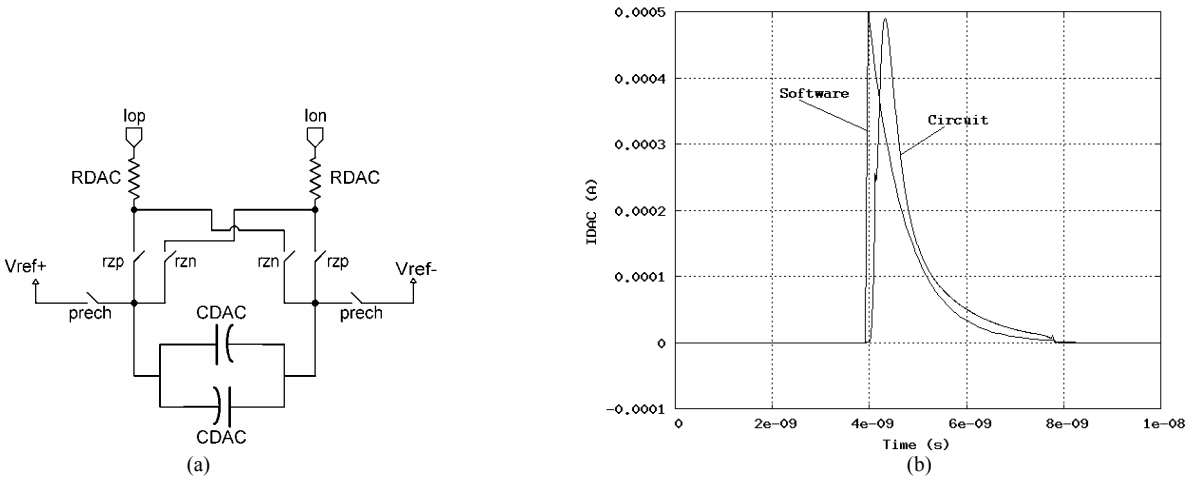


Figure 8: (a) HRZ exponential DAC. The values of CDAC and RDAC are: CDAC=200fF, RDAC=2KΩ for DAC1 and CDAC=80fF, RDAC=5KΩ for DAC2. (b) Comparison between the HRZ exponential DAC signal, in differential mode, generated with the software model and the one generated by the HRZ exponential DAC circuit.

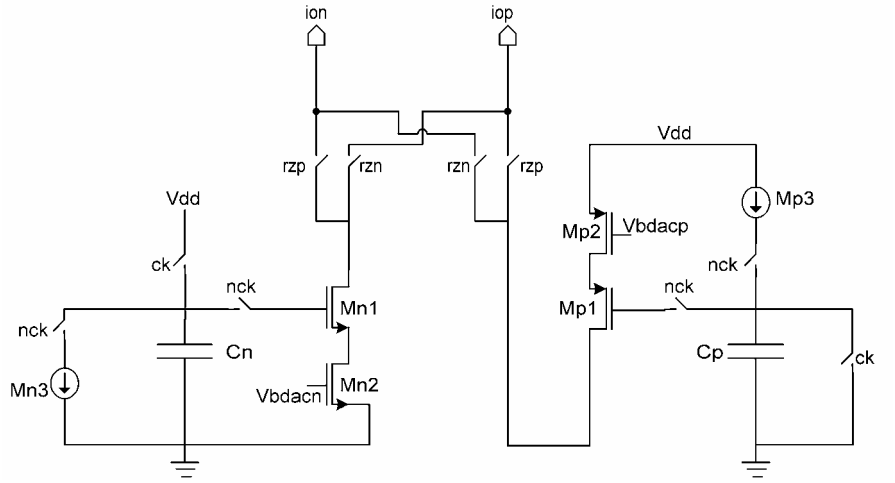


Figure 9: DAC circuit that generates a fully differential RZ rect-ramp signal with td=2T/7. Cn=Cp=200fF.

The differential output current for the proposed circuit together with the signal generated by the software model are presented in Fig. 10.

According to Fig. 8b and Fig. 10, circuit-generated signals present higher values at the end of the period, which can be directly traduce into a higher effect of JitterW. Thus, circuit results are expected to be worst than those predicted by the software model.

Fig. 11 shows the dynamic range graphs obtained from circuit simulations using Spectre. The two graphs correspond to the modulator with HRZ exponential and RZ rect-ramp (with td=T*2/7) feedback signals. In both cases the dynamic range of the modulator is greater than 70 dB and the SNDR peak is over 65 dB. Jitter has not been considered for these simulations.

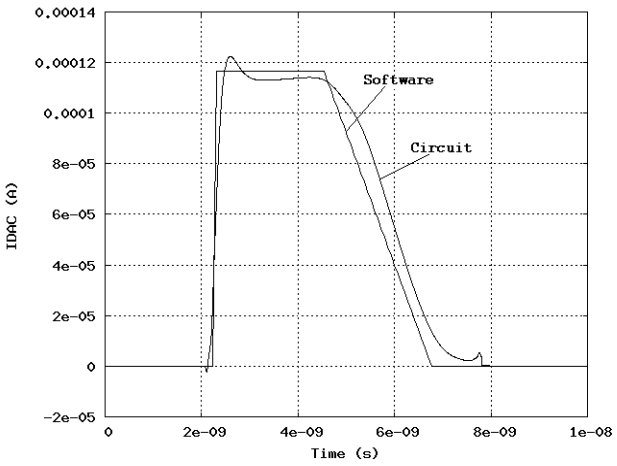


Figure 10: Comparison between the RZ rect-ramp DAC signal generated with the software model and the one generated by the RZ rect-ramp DAC circuit of Fig 9. Both signals are in differential mode and present td=2T/7.

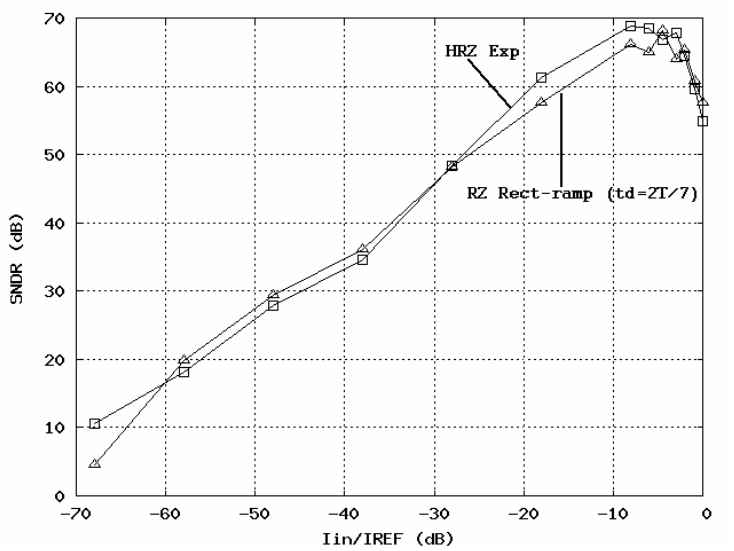


Figure 11: Dynamic Range obtained from circuit simulations as a function of the input tone amplitude. The input tone frequency is 250 KHz. Results of the modulator with HRZ exponential feedback and RZ rect-ramp (with td=2T/7) feedback signals are presented. No jitter has been considered.

6. CONCLUSION

A second order continuous-time sigma-delta modulator has been presented. Circuits for each of the blocks, including different DAC circuits for different feedback signals, have been provided. A comparison using a software model has been realized. It intends to show how modulator SNR is affected by JitterW when using HRZ rectangular, HRZ exponential, HRZ rect-ramp and RZ rect-ramp (with td=T*2/7) signals. It has been shown that a modulator using RZ rect-ramp (with td=T*2/7) feedback signals is more insensitive to JitterW than the same modulator using HRZ exponential. In addition lower integrator power consumption and input noise are expected for RZ rect-ramp (with td=T*2/7).

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