Continuous-time ΣΔ modulator with exponential feedback for reduced jitter sensitivity

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***Abstract*— A current-mode continuous-time Sigma Delta modulator with reduced jitter sensitivity has been analysed and designed in a 0.35 μm CMOS technology. The complete modulator has been implemented following a current-mode approach. This approach offers some advantages as: integrator blocks that present inherent low input impedance without the need of feedback, good stability and no necessity for common-mode circuit. Jitter rejection improvement was achieved by using an exponential decaying feedback current. Thus, the exponential-shaped DAC is based on a switched-capacitor circuit. Functional and transistor-level simulations have been carried out and the corresponding results are presented. A dynamic range of 67 dB (resolution of 10.8 bits), has been achieved for a second order modulator with an oversampling ratio of 64 and 1 MHz of bandwidth (sampling frequency of 128 MHz). In addition to distortion, quantization noise, clock jitter, thermal, and flicker noise have also been considered. The modulator consumes a power of 2.9 mW at a supply voltage of 2.5 V.**

***Index Terms*—Continuous-time ΣΔ modulator, jitter, current mode.**

I. Introduction

The design of Continuous-time (CT) Sigma-Delta must take into account two major problems. First, the excess loop delay [1] which is related to the non-instantaneous response of the quantizer. In order to reduce the sensitivity of the modulator to this problem a Return-to-Zero (RZ) or Half-Delayed Return-to-Zero (HRZ) feedback signals have been proposed, instead of the traditional Nonreturn-to Zero (NRZ) signal. Moreover, the RZ/HRZ signal also reduces the effect of rise and fall time asymmetry in the feedback signal. And second, timing error associated to clock jitter [1], [2], [3], [4] introduces noise into the in-band spectrum. The tolerable level of clock jitter decreases with increasing the oversampling ratio (OSR), and eventually jitter noise power will exceed quantization noise power. In addition to that, clock jitter affects RZ/HRZ modulators more severely than modulators employing NRZ feedback [2]. Thus, for high speed and/or high accuracy converters, this represents a serious challenge to chip designers.

Two strategies have been proposed to reduce the effect of clock jitter in CT Sigma-Delta modulators. Adams et al. [5] used a multibit converter, but the circuit is complicated by the need of scrambling to overcome the distortion caused by element mismatch. Another option is to use non-rectangular feedback signals. In particular, a decaying ramp and a decaying exponential signal were theoretically considered by Aboushady [3] and a cosine pulse by Luschas [6]. Arbitrary feedback waveforms have also been considered theoretically in [7]. A circuit with decaying exponential signal has been implemented by Van Veldhoven [8] and Ortmanns [9]. Indeed, both solutions, multibit and non-rectangular feedback signals, can be combined to obtain a higher performance.

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The aim of this paper is to design a ΣΔ modulator, working on current mode, with good jitter rejection, based on a Switched-Capacitor 1-bit DAC providing a decaying exponential feedback current. To our knowledge, there is not any reference in literature of previous CT ΣΔ modulators implemented completely in current mode. Current mode circuits are usually less complex and have less feedback which makes them faster, thus, their bandwidth is wider and they can work with higher frequency input signals. Moreover, the current input signal amplitude is not limited by the value of the supply voltage, which allows it to have a higher dynamic range and to be a good approach for low voltage applications. They are easily built to present low input impedance that is very useful in implementing operations such as addition/subtraction. Since CT ΣΔ modulators are based on feedback signals being added/subtracted to the signal path, the current mode is especially suitable for these modulators.

Simulations both at system level (using a software model) and circuit level (using Spectre simulator) have been carried out.

II. System Level Implementation

A fully differential second order CT modulator, working on current mode, has been designed (Fig. 1). For the feedback signals, a "short" decaying exponential pulse is used, namely an exponential pulse whose time constant is much lower than the used pulse-width (see Fig. 2). Thus, the majority of the switched-capacitor charge is transferred to the integrator at the beginning of the pulse-width.

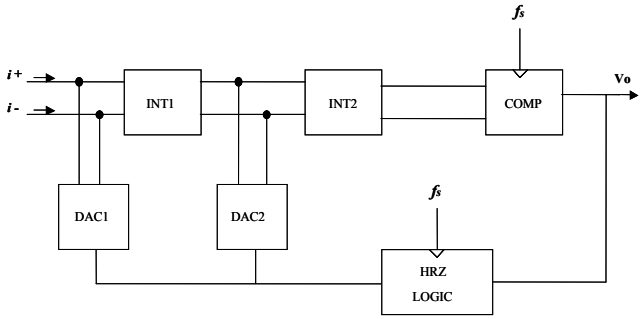

Fig. 1. Blocks diagram for second-order continuous-time ΣΔ modulator.

The exponential shaped feedback signal produces better results for a given pulse-width uncertainty owing to the error in the total transferred charge, due to the pulse-width uncertainty, is lower [8].

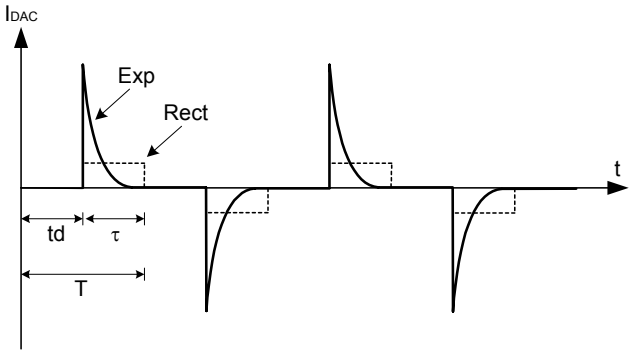

Fig. 2. DAC output current for exponential (Exp) and rectangular (Rect) HRZ feedback waveforms. td is the pulse delay, τ is the pulse width, and T is the sampling period.

In order to obtain the DAC1 and DAC2 coefficients (a_1 and a_2, respectively), the modified-Z transform of the continuous-time loop gain must be calculated [4]. For that purpose, the second order loop filter and the exponential waveform of the feedback signal must be considered. This later is:

$$h_{DAC}(t) = \exp\left(-\frac{(t - td)}{RC}\right) \cdot [u(t - td) - u(t - td - \tau)] \quad (1)$$

Where RC is the time constant, td is the pulse delay with respect to the sampling instant and τ is the pulse width.

After some calculations and equating to the loop gain of a second order discrete-time Sigma-Delta modulator, the coefficients are found to be:

$$a1 = -\frac{T}{RC} \quad (2)$$

$$a2 = -\left(1 + \frac{T}{RC} + \frac{td}{RC}\right) \quad (3)$$

In our system, we have chosen a HRZ feedback signal (td = T/2) to reduce the effect of excess loop delay [2], and RC = T/10. Then, a1 = -10, and a2 = -16. A modified structure for reduced power consumption can be proposed if a gain factor of ¼ is introduced in the last integrator. Reorganizing this gain factor over the rest of the circuit leads us to a gain factor of 1 for the second integrator, a gain factor of ¼ for the first integrator and scaled coefficients: a1_scl = a1, and a2_scl = a2/4.

As a first approach the modulator has been implemented in software. The aim was to find a reasonable tuning of the modulator before facing the circuit implementation. On the other hand, since the ΣΔ modulator is inherently a sampled circuit and circuit simulators usually do not allow adding thermal and flicker noise within a temporal analysis, the software model gives us the possibility of introducing it at the same time as distortion and quantization noise. "*C++*" language and "*SystemC*" libraries have been used to develop the model.

Thermal and flicker noise have been considered for every transistor, and modelled by using a noise current source between the drain and source terminals. Mathematical expressions for thermal and flicker noise, respectively, have been included in the following equations:

$$\overline{i^2_{th}} = 4KT\gamma g_m \quad (4)$$

$$\overline{i^2_{fl}} = \frac{Kf}{C_{ox}WL} \cdot \frac{1}{f} \cdot g_m^2 \quad (5)$$

Clock jitter noise is also included and has been modelled as two different sources of noise: clock phase noise, *JitterT*, and uncertainty in the pulse width, *JitterW*.

The main source of distortion, for intermediate frequencies, is related with the non-linearity of the integrators output branch transconductance.

Excess loop delay is not considered due to the use of HRZ feedback signals [2].

III. Circuit Level Implementation

The modulator has been implemented by using a 0.35 μm CMOS technology provided by AMS.

A. Integrator

The integrator is based on a fully differential architecture consisting of a folded-cascode topology (Fig. 3). It provides both high gain and low-power consumption. Due to the current mode approach, the required low input impedance (a few hundred of ohms) is achieved by using the appropriate cascode transistors. This configuration avoids the necessity of an operational amplifier with feedback to achieve the required low input impedance.

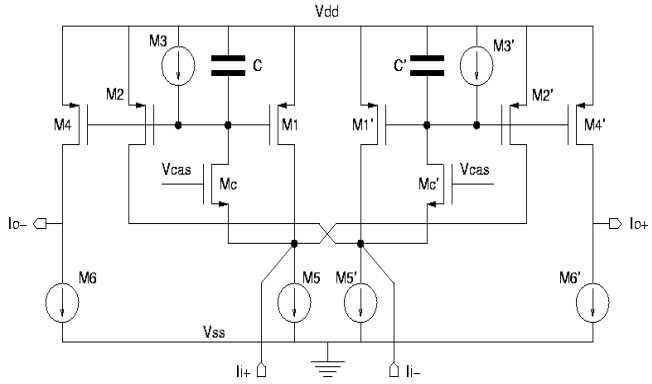

Fig. 3. Circuit implementation of integrators.

The circuit has been implemented to work properly with a maximum allowable input signal (reference current, Iref) of 25 μA.

Cascode branches have been sized to be able to work with 3/4 of DAC peak current defined in subsection B. Branches 1, 1', 2 and 2' of Fig. 3, drive 1/10 of cascode branches current. Output branches (M4, M4') drive 3/4*Iref and 3/2*Iref for the first and second integrators, respectively.

The transfer function of the integrator was calculated in a small signal analysis where the output impedance was considered for every transistor and the gate-source capacitance was included only for cascode transistors:

$$H(s) = -\frac{gm_4 \cdot ro_3 \cdot gm_c}{s^2 \cdot Cgsc \cdot C \cdot ro_3 + s \cdot \left(C \cdot ro_3 \cdot gm_c + Cgsc \cdot \frac{roc + ro_3}{roc}\right) + gm_c} \quad (6)$$

Where ro_x and gm_x are the output impedance and transconductance, respectively, of the transistors in Fig. 3. Cgsc is the gate-source capacitance of the cascode transistor and C is the integrating capacitance.

This expression was included in the system level implementation for modeling the integrator response. A

good frequency response agreement between system and circuit level is observed in Fig. 4a and Fig. 4b.

For intermediate frequencies, it behaves as an ideal integrator. It can be seen that there are two poles which make the frequency response differs from the ideal integrator response.

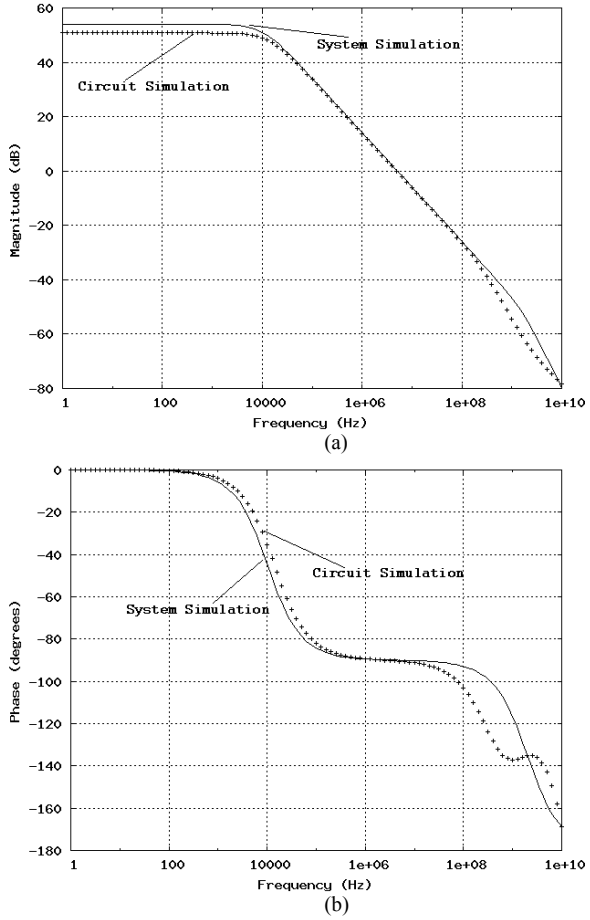

Fig. 4. Bode diagram of the integrator at system and circuit level (using Spectre).

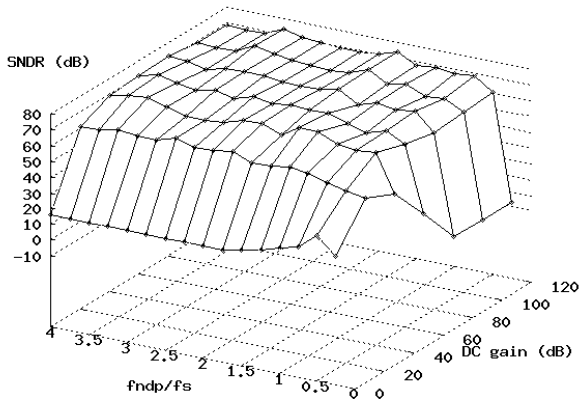

Fig. 5. Impact of integrator nonidealities on modulator SNDR, obtained from system level implementation. No noise was included. fndp is the frequency of the non-dominant-pole, fs is the sampling frequency and DC gain is the integrator DC gain.

System level simulations prove that non idealities of the integrator (finite DC gain, dominant pole and non dominant pole) do not limit significantly the signal-to-noise-distortion-ratio (SNDR) of the modulator when appropriate values are used. As is presented in Fig. 5, if the nondominant pole is above the sampling frequency and DC gain is above the OSR used, the SNDR of the modulator is not significantly affected. This is absolutely in concordance with literature, for instance, see reference [2]. DC gain and the position of the dominant pole are directly related: the smaller the DC gain, the higher the dominant pole frequency.

Integration capacitors have been implemented using the gate capacitance of NMOS transistors whose drain, source and bulk terminals have been shorted to ground. These transistors are working in the inversion region, maintaining an almost constant capacitance for a gate voltage above its threshold voltage.

B. DAC

The HRZ exponential DAC, shown in Fig. 6, is composed of two capacitors, two resistors and some switches controlled by the corresponding logic circuit.

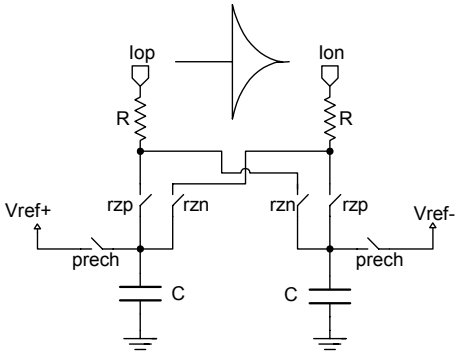

Fig. 6. HRZ exponential DAC. Differential exponential feedback waveforms have been included.

Its operation is as follows. First, the capacitor is precharged to the reference voltage. Next, the capacitor is connected to the output node, which is selected according to the logic circuit. The outputs nodes have a corresponding DC voltage value established by the integrator. The reference voltages are chosen to generate symmetric exponential waveforms in DAC output branches. Then, the capacitor discharges and generates a positive or negative current pulse whose integration corresponds to the charge accumulated during the precharge phase. The peak current of the exponential waveform has a value of

$$I_{peak} = Iref \cdot a\_scl \quad (7)$$

Where a_scl is the corresponding scaled DAC coefficient.

Capacitors are implemented in the same way as described for integration capacitors. Simple NMOS transistors are used to implement the output switches. When these output switches are conducting, they are working in the ohmic region, implementing at the same time the corresponding output resistor. Capacitors, resistors and reference voltage values have been chosen to ensure a good coupling with the integrator input.

C. Comparator

A fully differential architecture with current input and voltage output has been used. It is composed of three different stages: preamplifier, clocked regenerative latch and C^2MOS dynamic output latches (Fig. 7). Because of it has

current mode input the comparator is not sensitive to DC offset, and there is not necessity for common-mode circuit.

It has been proved at circuit level simulations that the regeneration time is short enough to avoid metastability problems.

Assuming the input to the comparator is a random variable, metastability can be quantified as the probability of its occurrence [10]. This probability is expressed as:

$$P(T_1 > T_C) = \exp(-\frac{T_C}{\tau}) \quad (8)$$

Where T1 is the time required for regeneration, T_C is half the sampling period, and τ is the time constant of the regeneration phase. The regenerative latch must achieve a stable state within half a sampling period to avoid metastability. From circuit level simulation, τ has been found to be about 110 ps, and T_C for a sampling frequency of 128 MHz is 3.9 ns. The probability to occur a metastable state within a clock cycle is about 5.7e-16. Thus, the time between two consecutive errors will be of 158 full days. Then, metastability can be considered negligible.

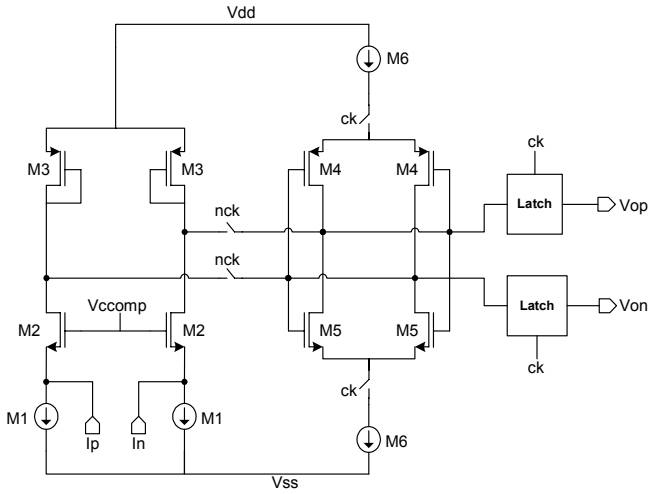

Fig. 7. Circuit implementation of the regenerative comparator.

IV. Simulation Results

The results obtained from system and circuit level simulations will be shown next. For the later, simulations from the schematic circuit have been used.

The schematic circuit has been implemented for a supply voltage of 2.5 V and a reference current of 25μA.

Integrator 1: C=7.82 pF

Integrator 2: C=3.91 pF

DAC 1: C=557 fF, R=1.4 K

DAC 2: C=222 fF, R=3.5 K

DAC reference voltages: Vref1=1.65 V, Vref2=0.95 V.

A. Spectrum analysis

Output spectra from system and circuit level simulations are shown in Fig. 8 for comparison. Each spectrum has been obtained by applying the Fast Fourier Transform algorithm to the differential output in the time domain.

Only distortion and quantization noise have been considered at circuit level, due to the inability of the software design tool to include other sources of noise in a timing analysis.

At system level, thermal, flicker, and clock jitter noise have also been included. A value of 1‰ of the clock period has been used for both, *JitterT* and *JitterW*. Thermal and *JitterW* noise increase the noise floor, whereas *JitterT* causes visible skirts of the test tone [2]. Flicker noise is hardly appreciated in the figure because of the low corner frequency selected (about 40 KHz). Transistors channel length has been increased to get this low corner frequency.

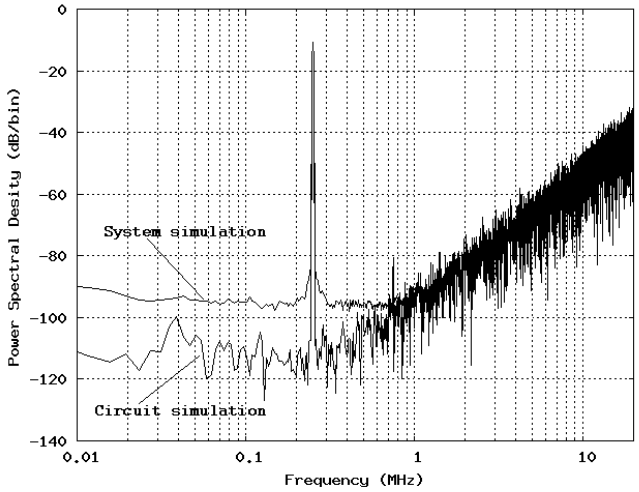

Fig. 8. Output spectra of the second order modulator for system and circuit simulation. 32768 samples have been used for the FFT in both cases.

The input used for these simulations is a tone at 250 kHz which amplitude is -6 dB referred to the reference current. As the sampling frequency is 128 MHz and an oversampling ratio of 64 was used, the bandwidth is 1 MHz.

The different noise floor and tone skirts observed in Fig. 8 in the signal band are consistent with the additional noise sources considered at system level. As a consequence, the SNDR is limited to about 62 dB.

B. Jitter sensitivity

Multiple system simulations have been carried out to draw diagrams of Fig. 9a and Fig. 9b. Neither thermal nor flicker noise were included in order to analyze the effect of clock jitter separately. Values of *JitterT* and *JitterW* are varied from 0 to about 6 ‰ of clock cycle. HRZ exponential and rectangular feedback waveforms have been used for comparison.

Fig. 9a presents the modulator SNDR as a function of *JitterW* for different values of *JitterT*. For the exponential feedback signal case, there is no SNDR drop when *JitterW* is increased within the considered range, for a given value of *JitterT*. On the contrary, there is a quick fall of SNDR for the rectangular case if *JitterW* is increased. Thus, Fig. 9a shows clearly that the modulator with rectangular feedback signals is visibly affected by *JitterW,* whereas it is almost insensitive to *JitterW* when using exponential feedback signals.

Fig. 9b shows the modulator SNDR as a function of *JitterT* for different values of *JitterW*. When exponential feedback signals are used, SNDR drops approximately in the same manner regardless the value of *JitterW*. From plots Rec(JW=0) and Exp(JW=0) it can be seen that the modulator SNDR falls with the same slope for the exponential and rectangular cases. Even though it is more

difficult to see, this is also true for the cases JW=15 ps and JW=30 ps, and the apparent difference is due to the effect of *JitterW* and not of *JitterT*. The similar modulator behavior for exponential and rectangular cases when *JitterT* is increased is completely logical, since clock phase noise (*JitterT*) affects to the instant when clock edge happens and not to the pulse-width.

From this analysis, it can be concluded that *JitterT* will affect in the same way to modulators with HRZ exponential and rectangular feedback signals. However, using HRZ exponential feedback signals makes the modulator insensitive to *JitterW* up to relatively high values. This conclusion is in concordance with other studies recently published [3], [8], [9].

Finally, from system level simulations, a reduced sensitivity of the modulator SNDR to the absolute value of the time constant is obtained. Thus, tolerance of the technological process, switch resistances, non-zero input resistance of the integrator and parasitic elements of the devices do not deteriorate significantly the modulator response.

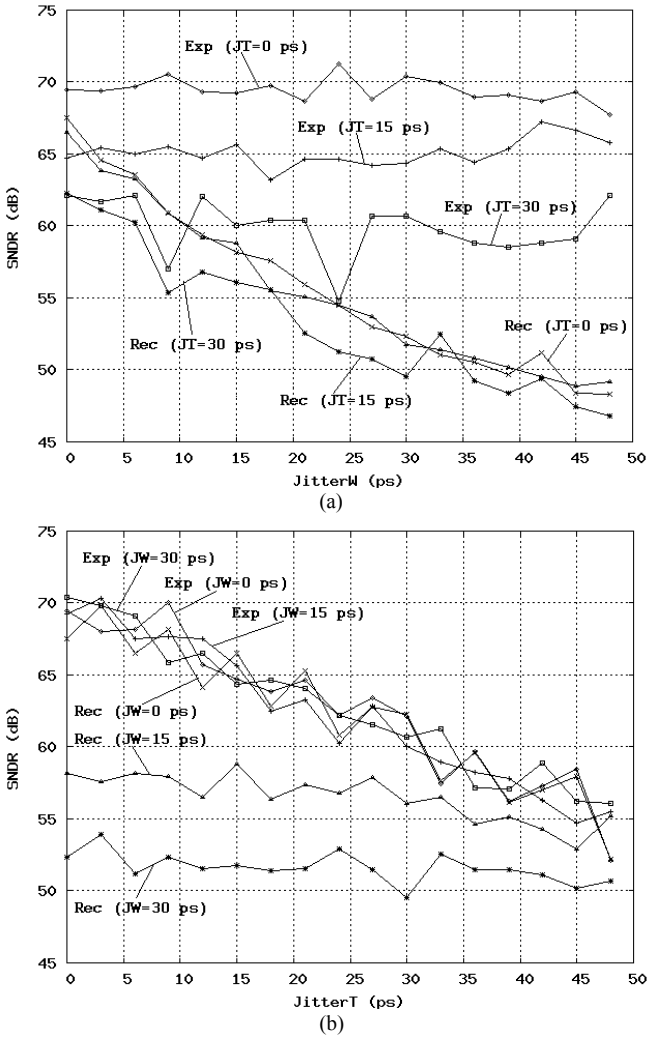

Fig. 9. SNDR diagrams for different values of JitterT and JitterW. Exp and Rec represents simulations with HRZ exponential and HRZ rectangular feedback waveforms, respectively. JT stands for JitterT and JW for JitterW. a) Shows the SNDR as a function of JitterT while keeping JitterW constant at a certain value. b) Shows the SNDR as a function of JitterW while keeping JitterT constant at a certain value. All simulations have been carried out at system level.

C. *Dynamic range*

Dynamic range, DR, has been considered as the difference between the maximum and the minimum value of the input amplitude that makes SNDR greater than 0 dB [2]. Fig. 10 shows the SNDR value for different amplitudes of sinusoidal input current in differential mode. The circuit simulation points show a greater dynamic range, because the system model includes thermal, flicker, and jitter noise, which are not present in circuit simulations. The DR measured from the system simulation graph, which includes noise, is about 67 dB, and the SDNR peak, 62 dB. The peak of SNDR occurs for an input current value of approximately half the maximum allowable input.

The power consumption of the modulator is 2.9 mW at a supply voltage of 2.5 V. Using the DR and the power consumption of the modulator, the Figure of Merit (FM), defined in [11], can be calculated as follows:

$$FM = \frac{P}{2 \cdot BW \cdot 2^{\text{resolution (bit)}}} \cdot 10^{12} \quad \text{(pJ)} \tag{9}$$

Where P is the power consumption in watts, BW is the signal bandwidth in Hz, and resolution corresponds to the number of bits calculated from the DR. For the 67 dB of DR (the effective number of bits, ENOB, is 10.8), a bandwidth of 1 MHz, and a power consumption of 2.9 mW, the resulting FM is equal to 0.81 pJ. That is an excellent figure of merit within the state-of-art of ΣΔ modulators, as can be seen, for instance, in [3] and [12].

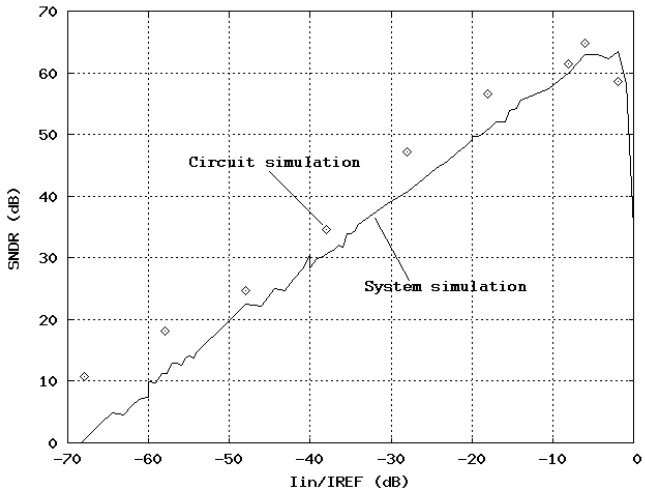

Fig. 10. Dynamic Range as a function of the input tone magnitude. Both circuit and system level results are shown.

V. CONCLUSION

A continuous-time Sigma Delta modulator working on current mode with reduced jitter sensitivity has been analysed and designed in a 0.35 μm CMOS technology. This reduction has been achieved using exponential-feedback waveforms generated by a switched capacitor-based DAC. Simulations show a substantial improvement on jitter rejection with respect to the conventional rectangular-feedback DAC. A specific circuit implementation has been proposed achieving 67 dB of dynamic range, and a resolution of 10.8 bits, for 1MHz of bandwidth with a power consumption of 2.9 mW for 2.5 V of supply voltage.

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