A 3-30 MHz Tunable Continuous-Time Bandpass Sigma-Delta A/D Converter for Direct Conversion of Radio Signals

D. Bisbal, J. San Pablo, J. Arias, L. Quintanilla, J. Vicente, and J. Barbolla

Abstract— **In this paper we present the design and simulation results of a CMOS fourth-order bandpass delta-sigma modulator, intended for the A/D conversion of RF signals directly coming from a shortwave receiver antenna. The modulator tuning range covers the 3-30 MHz frequency band. The continuous-time loop filter is based on two Gm-C resonators, with low-power transconductors and MOS capacitors. The modulator is implemented in a 0.35um triple-metal standard CMOS technology. Circuit-level simulations demonstrate that the modulator achieves SNDR higher than 60 dB for all the nominal frequency range, for a signal bandwidth of 10 kHz, and a power consumption of about 6 mW.**

Index Terms— **Delta-sigma A/D converter, continuous-time, bandpass, tunable, low-power.**

I. Introduction

DELTA Sigma Modulation is a widely applied technique for high-performance analog-to-digital conversion of narrow band signals. In addition, this technique is well suited to perform the so-called *bandpass* A/D conversion, that is, direct conversion of narrow-band signals modulated on a carrier, (as occurs in many communication systems) [1]. This bandpass A/D conversion capability has opened a door towards the realization of fully-monolithic, low-cost, low-power communication devices, since it allows several transceiver stages to be moved to the digital domain. This way, better noise inmunity, more robustness and flexibility may be achieved, leading to potential improvements in performance and power consumption, and cost reduction.

Several work has been done in digitalizing bandpass signals in the IF range, using both Discrete-Time (DT) [2], [3] and Continuous-Time (CT) [4]–[6] bandpass delta-sigma A/D converters. DT converters, which are mostly implemented as switched-capacitor circuits, are more accurate and achieve higher dynamic range than their CT counterparts. However, the speed of these modulators is limited to several megahertzs. On the other hand, CT converters allow high-speed operation while keeping power consumption and chip area low. Though clocking rates in the gigahertz range have been reported [7], [8] using GaAs or InP bipolar technology, attempts in CMOS bandpass $\Delta\Sigma$ modulators are still limited to IFs of several tens of megahertzs [6], [9]. The disadvantages of the CT approach are less accuracy and lower dynamic range.

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All these proposals allow the IF signal-processing stage of the receivers to be moved to the digital domain. However, in these receivers, RF signals are still first downconverted to IF by means of an analog mixer, so mixer circuit non-idealities (such as non-linearity or mismatch of components) can still degrade sensibly the expected (theoretical) performance.

In our work, following this trend of moving to the digital domain as many blocks as possible, we aim to digitalize the RF signal coming from the antenna before any mixing. This way, by moving the mixing to the digital domain, a perfect matching between mixers is achieved and, therefore, no high performance channel-selection filters are required.

In Fig. 1 a system block diagram of such a *digital-RF* receiver is shown. Analog components are minimized: just a low noise amplifier (LNA), a bandpass filter (BPF) and a bandpass ADC are needed. The function of the BPF is to reduce the amplitude of out-of-band signals, thus avoiding overloading the ADC. This filter also acts as an anti-alias filter, improving further the implicit anti-alias rejection of CT delta-sigma ADC [4].

In this paper we focus on the bandpass delta-sigma A/D converter, suitable to be integrated in a Single-Chip, digital-RF Short-Wave Radio Receiver, implemented in 0.35μm CMOS technology. Based on short-wave radio receiver specifications —3-30 MHz tuning range, maximum signal bandwidth of 6 kHz (AM and SSB signals), sensitivity of 0.5 μV (for 10 dB SNR) , and high dynamic range [10]— we have set the following requirements for our ADC:

- Tuning capability: 3-30 MHz
- SNDR > 60 dB
- ADC input signal amplitude range: 10 μV – 10 mV.

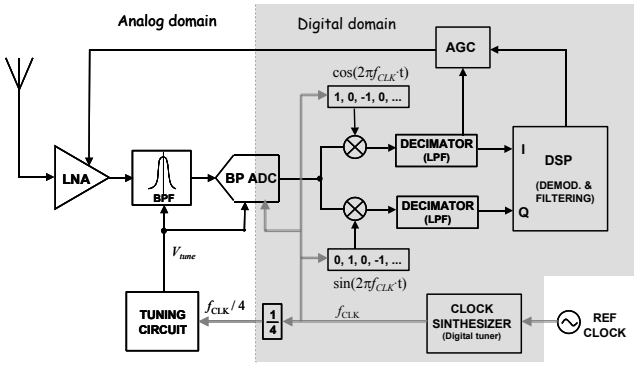


Fig. 1. Proposed receiver architecture

The input range of the ADC has been selected in order to reduce the required gain of the preceding blocks —the LNA and the BPF— to practical values.

II. Modulator Architecture

In order to meet the specifications we have chosen a 4th order CT bandpass ΔΣ ADC with an NTF having a frequency notch at $f_o = f_s/4$. Though, intuitively, a 2nd order BP modulator may appear to meet the SNDR specifications (in fact, theoretically, it achieves SNDR higher than 60 dB, since OSR is at least 500), system level simulations have shown that order two is insufficient, due to the so-called *idle-tones problem* [1]. Moreover, using a 4th order modulator can alleviate both tuning and linearity requirements, since it can potentially perform widely over the specifications.

As it is commonly done, we have designed our CT delta-sigma modulator by transforming a DT prototype into the CT system, following the exact DT-CT transformation method presented in [4]. The DT noise and signal transfer functions of a fourth order $f_s/4$ bandpass modulator with a full sample of delay in the feedback path [4], [5] are

$$NTF(z) = z^{-1}\frac{z^{-1}(2+z^{-2})}{(1+z^{-2})^2} \quad (1)$$

$$STF(z) = 0.5\frac{z^{-1}(1-z^{-2})}{(1+z^{-2})^2} \quad (2)$$

which, for the particular case of half-delayed return-to-zero (HRZ) DAC pulses, transform into

$$NTF(s) = \frac{\frac{\pi}{2T}\cdot\left(1+\sqrt{2}-\frac{1}{2\pi}\right)\cdot s^3+\left(\frac{\pi}{2T}\right)^2\cdot\left(\frac{7-\sqrt{2}}{8}+\frac{\sqrt{2}}{2\pi}\right)\cdot s^2+\left(\frac{\pi}{2T}\right)^3\cdot\left(1+\sqrt{2}+\frac{1}{2\pi}\right)\cdot s+\left(\frac{\pi}{2T}\right)^4\cdot\left(\frac{7-\sqrt{2}}{8}\right)}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \quad (3)$$

and

$$STF(s) = \frac{\frac{\pi}{2T}\cdot\left(\frac{1+\sqrt{2}}{4}-\frac{1}{2\pi}\right)\cdot s^3+\left(\frac{\pi}{2T}\right)^2\cdot\left(\frac{1-\sqrt{2}}{8}+\frac{\sqrt{2}}{2\pi}\right)\cdot s^2+\left(\frac{\pi}{2T}\right)^3\cdot\left(\frac{1+\sqrt{2}}{4}+\frac{1}{2\pi}\right)\cdot s+\left(\frac{\pi}{2T}\right)^4\cdot\left(\frac{1-\sqrt{2}}{8}\right)}{\left(s^2+\left(\frac{\pi}{2T}\right)^2\right)^2} \quad (4)$$

In Fig. 2 we show the architecture chosen to implement the desired NTF and STF. This architecture, which was suggested in [4], but not implemented, consists of the cascade of two Gm-C resonators. Gm-C technique is a well known approach for implementing high-speed CT filters. The main disadvantage of these circuits is the non-linearity of transconductors. However, in our particular case, it is not a serious problem since the modulator handles small signals, of about tens of milivolts.

The loop transfer function of this modulator is given by

$$H(s) = \frac{\frac{g_{mb3}}{C}\cdot s^3 + \frac{g_m g_{mb2}}{C^2}\cdot s^2 + \frac{g_m^2(g_{mb3}+g_{mb1})}{C^3}\cdot s + \frac{g_m^3(g_{mb2}+g_{mb0})}{C^4}}{\left(s^2+\left(\frac{g_m}{C}\right)^2\right)^2} \quad (5)$$

The signal transfer function G(s) is equal to H(s) just by changing the subscript *b* by *a*. Matching H(s) with NTF(s) and G(s) with STF(s) leads to the following relationships.

$$\frac{g_m}{C} = \frac{\pi}{2T} \quad (6)$$

$$g_{mb0} = -\frac{\sqrt{2}}{2\pi}g_m \quad (7.1) \qquad g_{ma0} = -\frac{\sqrt{2}}{2\pi}g_m \quad (7.5)$$

$$g_{mb1} = \frac{1}{\pi}g_m \quad (7.2) \qquad g_{ma1} = \frac{1}{\pi}g_m \quad (7.6)$$

$$g_{mb2} = \left(\frac{7-\sqrt{2}}{8}+\frac{\sqrt{2}}{2\pi}\right)g_m \quad (7.3) \qquad g_{ma2} = \left(\frac{7-\sqrt{2}}{8}+\frac{\sqrt{2}}{2\pi}\right)g_m \quad (7.7)$$

$$g_{mb3} = \left(1+\sqrt{2}-\frac{1}{2\pi}\right)g_m \quad (7.4) \qquad g_{ma3} = \left(\frac{1+\sqrt{2}}{4}-\frac{1}{2\pi}\right)g_m \quad (7.8)$$

The notch frequency is given by $f_o = \frac{g_m}{2\pi C}$ (8)

III. Tuning

The bandpass modulator is designed to have a notch at $f_o=f_s/4$. Thanks to the significant tolerance of delta-sigma modulators to component parameters, the modulator is expected to work properly even if the notch frequency (f_o) is shifted up or down (by changing either transconductance g_m or capacitance C) without changing the sampling clock frequency f_s, thus breaking the equality $f_o = f_s/4$. However, system level simulations indicate a maximum relative frequency shift limited to 18%, due to, out of this range, the Q of the bandpass loop filter is too low for the modulator to be stable. Hence, in order to fully cover the 3-30 MHz range, tuning must be carried out by changing the sampling clock frequency f_s accordingly. Of course, the change in f_s must be followed by either a proportional change in g_m or an inversely proportional change in capacitance C (remind that $f_o = g_m/2\pi C$). Since neither the transconductance of a transconductor nor the capacitance of a capacitor can be changed in a continuous way for so vast a range, either transconductor arrays or capacitor arrays must be used.

Therefore, tuning is performed in two steps: a first step of discrete *coarse tuning*, and a second step of continuous *fine tuning*. This concept is illustrated in Fig. 3. In coarse tuning, a notch frequency $f_{o,i}$ is selected from a finite set of discrete notch frequencies $[f_{o,0}, f_{o,1}, \ldots, f_{o,N}]$. This is done by digitally synthesizing a clock frequency $f_{s,i} = f_{o,i}/4$, and selecting the cells of either the *g_m-array* or the *C-array* accordingly. Once the notch frequency is coarsely tuned, fine tuning is performed by changing the transconductance of g_m by means of adjusting its biasing current.

Tuning is performed automatically by means of the master-slave tuning circuit shown in Fig. 4. The resonance frequency of the master resonator is locked to an external accurate frequency by a PLL system. The frequency control

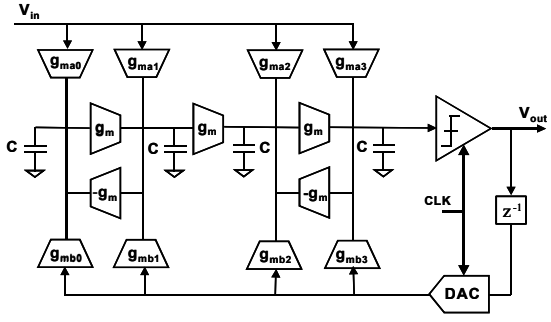


Fig. 2. Single-ended block diagram of the 4th-order bandpass ΔΣ modulator, with loop filter based on the cascade of two Gm-C resonators.

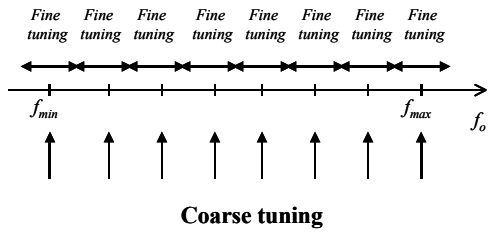


Fig. 3. Two-step tuning concept.

voltage (V_{tune}) of the master resonator is then used to tune the loop filter resonators (slave resonators). In the PLL, the output amplitude of the VCO is kept small (tens of mV) thanks to an amplitude control circuit. This is needed due to the non-linear characteristics of the Gm-C master resonator, that can result in detuning. Automatic tuning also makes the system robust to fabrication tolerances, temperature variations and parasitic effects.

A. Coarse Tuning: Constant-C versus Constant-Gm

Now, we will compare the two approaches for coarse tuning (Fig. 5) —*constant-C* (using transconductor arrays) and *constant-G_m* (using capacitor arrays) — in terms of performance, power consumption and area.

As we will discuss later, the most limiting factor of the modulator SNDR is thermal noise. At each of the four integrating nodes of the loop filter, we can consider the superposition of a signal current and a noise current. These currents are the sum of the signal and noise currents, respectively, delivered by all transconductors connected to that node. At a node *j*, the squared noise current is given by

$$I_{n,j}^2 = I_n^2 + I_{naj}^2 + I_{nbj}^2 = 4kT\gamma\Delta f\left(g_m + g_{maj} + g_{mbj}\right)\cdot 4 \quad (9)$$

Since g_m, g_{maj} and g_{mbj} are proportionally related (i.e., $g_{maj}=\alpha_{aj}\,g_m$, $g_{mbj}=\alpha_{bj}\,g_m$), we can write

$$I_{n,j}^2 = 4kT\gamma\Delta f\left(1+\alpha_{aj}+\alpha_{bj}\right)g_m\cdot 4 = \Delta f\cdot\kappa_n\cdot g_m \quad (10)$$

where κ_n is a proportionality constant we define for convenience. On the other hand, the signal current is given by

$$I_{s,j} = g_m v_j + g_{maj} v_{in} + g_{mbj} v_{DAC} \quad (11)$$

where v_j is voltage at node *j*. Since v_j, v_{in} and v_{DAC} are also related, we can write

$$I_{s,j} = \kappa_s g_m \quad (12)$$

where, again, a proportionality constant κ_s has been defined for convenience.

As a consequence, the signal to thermal noise ratio ($SNR_{TH} = I_{s,j}^2 / I_{n,j}^2$) is proportional to g_m. Note that signal bandwidth Δf is constant in all the frequency range. In Fig. 6*a*, SNR_{TH} is plotted as a function of the notch frequency for both *constant-C* and *constant-G_m* approaches. Note that SNR_{TH} specification settles the minimum transconductance $g_{m,min}$.

Most of circuit power is dissipated in the loop filter transconductors. Power consumption of a transconductor is proportional to its transconductance when a constant V_{EG} is maintained during circuit design. Also, all transconductances are proportionally related to g_m. Then, the loop filter power consumption is proportional to g_m. In Fig. 6*b* power consumption as a function of notch frequency is plotted for both approaches.

Finally, we compare both approaches in terms of chip area. Remind that SNR_{TH} specification defines $g_{m,min}$. According to that, we can state that, for the constant-C approach, $f_{o,min} = g_{m,min}/2\pi C_{max}$ and $f_{o,max} = g_{m,max}/2\pi C_{max}$, and, for the constant-Gm approach, $f_{o,min} = g_{m,min}/2\pi C_{max}$ and $f_{o,max} = g_{m,min}/2\pi C_{min}$. From these equations we can conclude than the area required by constant-C solution is the largest, since in both cases, a total capacitance of C_{max} is needed, while constant-C solution demands for a larger transconductance.

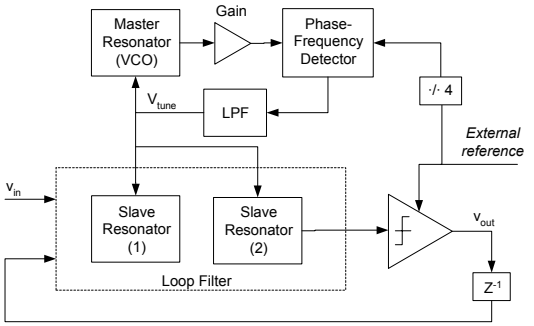


Fig. 4. Diagram of the bandpass ΔΣ modulator with the master-slave tuning circuit.

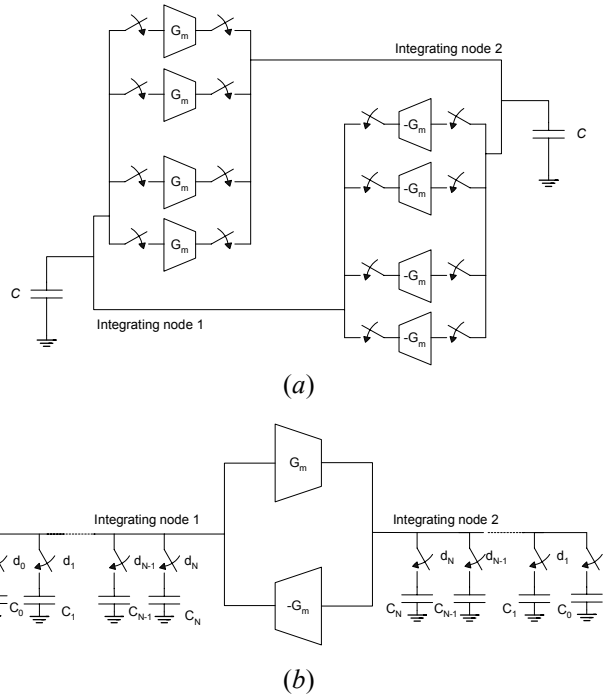


Fig. 5. Circuit schematic of the modulator's resonator, using (*a*) transconductors arrays (*Constant-C* approach) and (*b*) capacitor arrays (*Constant-Gm* approach) for coarse tuning.

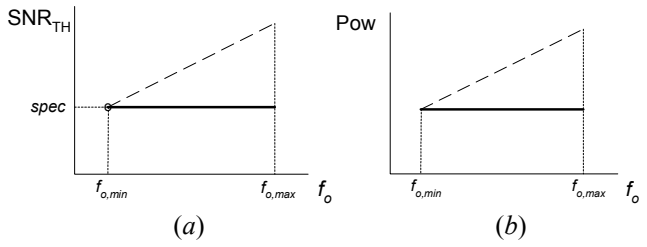


Fig. 6. Variation of signal to (*a*) thermal noise ratio and (*b*) power consumption versus notch frequency of the tunable bandpass ΔΣ modulator, using the Constant-Gm approach (solid line) and the Constant-C approach (dashed line).

Therefore, we can conclude that the *constant-G_m* approach is preferable since, for a given SNR specification, it consumes less power and less area than the *constant-C* approach for *all* notch frequencies larger than $f_{o,min}$.

IV. Effect of Circuit Non-idealities on System Performance

Before designing the circuits, we have analysed, by means of system-level simulations, how system non-idealities affect the modulator performance. In order to perform system level simulations, we have developed a *C*-language model of our continuous-time modulator where thermal noise, output resistance, non-linearity, and non-dominant pole of transconductors, as well as the series resistance of capacitors, have been considered. Thermal noise has been considered for all transconductors, which are assumed to be implemented as cascode differential pairs. Modelling the transistor noise by a noise current source between its drain and source terminals —with value $I_n^2 = 4kT\gamma g_m$—, and assuming that the main noise contributors (i.e. the input transistors and the PMOS current sources) have equal transconductance, the transconductor output noise current results $I_{o,n}^2 = 16kT\gamma g_m$. Clock imperfections have been also modelled, namely, timing jitter (the deviation of a clock's output transitions from their ideal positions) and phase noise (modelled as accumulated jitter) [11]. We have been driven to the following conclusions:

Thermal noise introduces a flat noise floor. It has shown to be the main source of SNDR degradation. The thermal noise level will mask all the other sources of noise, while those be maintained under reasonable limits. Similar to thermal noise, non-linearity of transconductances also pushes up the quantization noise level, consequently degrading SNDR. It is well known that non-linearity of transconductors decreases by increasing the overdrive voltage (V_{OV}) of the input transistors. In this case, setting V_{OV} above 200 mV guarantees that noise caused by non-linearity will be masked by the thermal noise floor.

Output resistance of transconductors and non-dominant pole of transconductors affect the Q of the resonators. If the resulting Q is too low (i.e., Q<20), the system becomes unstable. Our simulations prove that stability is guaranteed if integrator voltage gain is maintained above 500, and non-dominant pole frequency is kept above 1 GHz. When the system is stable, the SNDR degradation is quite below that produced by thermal noise, so it will be masked.

When the integrating capacitors are implemented as MOSFET capacitors, their series resistance introduces an additional zero at high frequency, thus degrading the resonator's Q. It may cause system instability if the resulting Q is too low (Q<20).

Clock jitter causes uncertainty not only in the clock sampling instants, but also in the clock pulse width. Its effect on modulator performance appears as a flat noise floor in the modulator output spectrum, that will be masked by thermal noise if clock jitter is kept below 2.5% of the clock period. That means the system tolerates a jitter of more than 200 ps in the worst case. Clock phase noise effect on the modulator output spectrum is the introduction of skirts surrounding the output signal, which may degrade SNDR when a narrow band is considered. However, this degradation will be negligible while clock phase noise is kept below –90 dBc/Hz@10kHz.

V. Circuit Implementation

The modulator shown in Fig. 2 is implemented with fully-differential circuitry. Transconductors are implemented as cascode differential pairs (Fig. 7*a*) in order to introduce minimum thermal noise, while providing high output resistance. Since cascode transistors introduce an additional high-frequency pole (f_{nd}), they must have reduced area in order to keep f_{nd} above 1 GHz. Input transistors have an V_{OV} of about 300 mV to guarantee that the distortion introduced by non-linearity is kept below thermal noise level. The common mode output voltage is kept constant thanks to the high-gain common-mode feedback circuit (CMFC) shown in Fig. 7*b*.

The feedback loop shown in Fig. 2 (formed by the cascade of a voltage-output DAC and four feedback transconductors g_{mbj}) is substituted by four current-output DACs, with $I_{DAC,j} = g_{mbj}v_{DAC}$. Fig. 8 shows one of these current DACs, where cascode current sources are used in order to guarantee a high output impedance. Note that this is mandatory, since it is attached to the resonator nodes in parallel with transconductors output resistances. Transistors M_{p0}, M_{p1}, M_{n0}, M_{n1}, M_{pi} and M_{ni} work as switches, and *p0*, *p1*, *n0* and *n1* are control signals which are active only in the second half of clock cycle. During the first half of each clock cycle switches M_{pi} and M_{ni} are closed, thus draining the current provided by the current sources, so the DAC current output is 0. During the second half of clock cycle, either switches M_{p1} and M_{n1} (if the modulator output is a

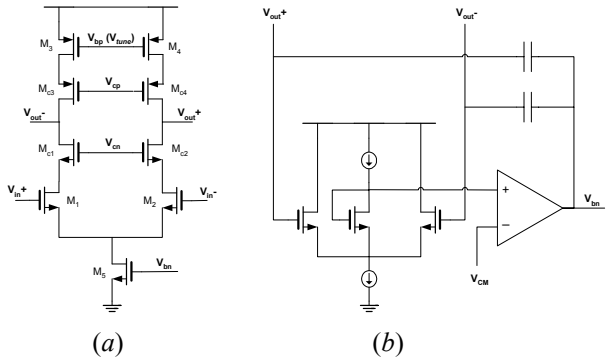


Fig. 7. Circuit implementation of (*a*) transconductors and (*b*) the common-mode feedback circuit.

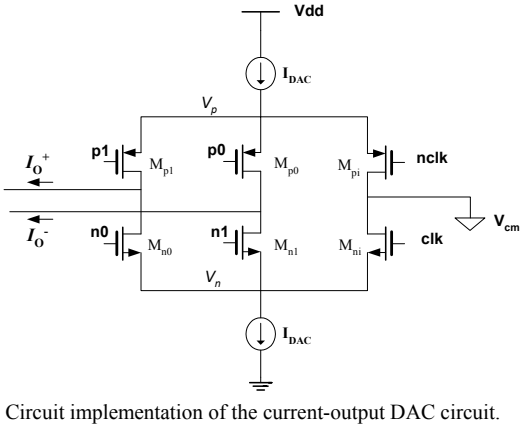


Fig. 8. Circuit implementation of the current-output DAC circuit.

logic "1") or switches M_{p0} and M_{n0} (if the modulator output is a logic "0") are closed, thus providing a differential current equal to $2I_{DAC}$ or $-2I_{DAC}$, respectively.

In order to save area, the capacitors are implemented as NMOS transistors with their source, drain and substrate tied to ground acting as the capacitor bottom plate, and their gate acting as the top plate. The main drawback of employing MOS capacitors is that the channel-resistance of the transistors remain in series with the capacitor, thus degrading its Q. The equivalent series resistance can be reduced by slicing the capacitors into small wide portions, placed in parallel, so their capacitances add while their series resistances are divided.

Implementation of capacitor arrays as it is shown in Fig. 5 entails design difficulties, due the position of the switches. The switch on-resistance causes an additional zero which degrades the resonators' Q significantly. Therefore, we propose a more practical solution, which is illustrated in Fig. 9. In this scheme, the integrating node is the top plate of the capacitor C_0, instead of the transconductor output. So, now, from the integrating node, the switch on-resistance is seen in series with the large transconductor output resistance, instead of in series with the integrating capacitor. As a consequence, the switch on-resistance introduces no additional zero, and does not degrade the Q of the resonator. For this circuit to work properly, switches have to be scaled proportionally to capacitors, thus creating a "virtual short-circuit" of the top plates of all capacitors that are switched to the integrating node. This way, the integrating capacitance (namely, the capacitance seen from the integrating node) is the sum of the capacitances connected to the integrating node. The word $d_N d_{N-1} \cdots d_2 d_1$, in thermometric code, is used to control the switching of the capacitors. The switches controlled by d_0 are always closed.

Fig. 10 shows the comparator implementation. It consists of the cascade of six stages: an input buffer, a regenerative comparator, three C^2MOS dynamic latches, and an output inverter. The purpose of the buffer is to isolate the loop filter output from the large voltage pulses of the latch. The comparator is implemented as a clocked regenerative full-swing latch. The cascade of three dynamic latches hold (and regenerate) the data for three half cycles, so the output is delayed one whole extra clock cycle.

VI. Simulation Results

The bandpass delta-sigma modulator is implemented in a 0.35μm triple-metal standard CMOS technology. The component values used in the simulations are C_{max} = 10 pF, $G_m = G_{m,min}$ = 188 uA/V, v_{DAC} = ±30 mV, and an input sinusoidal signal v_{in} with an amplitude of 10 mV. The capacitor array has dimension N = 12, where the capacitors values have been selected to obtain consecutive notch frequencies separated 20% (i. e. $f_{o,i} = 1.2 \cdot f_{o,i-1}$). Circuit-level simulation results presented in this section are based on schematics and have been carried out using Spectre. Layout-extracted simulation results will be presented at the conference.

Fig. 11*a* shows the modulator output spectrum obtained from a circuit level simulation with an input signal frequency

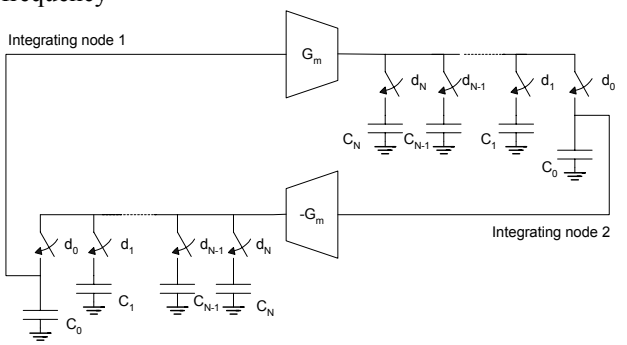


Fig. 9. Practical solution for the circuit implementation of the modulator resonators using capacitor arrays.

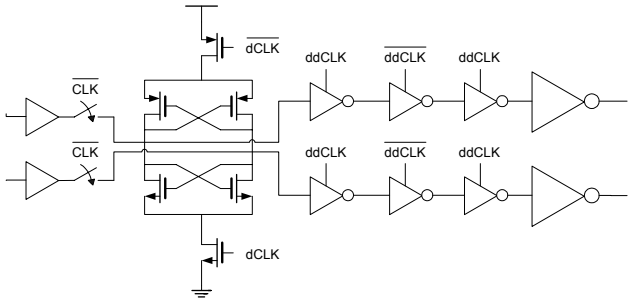
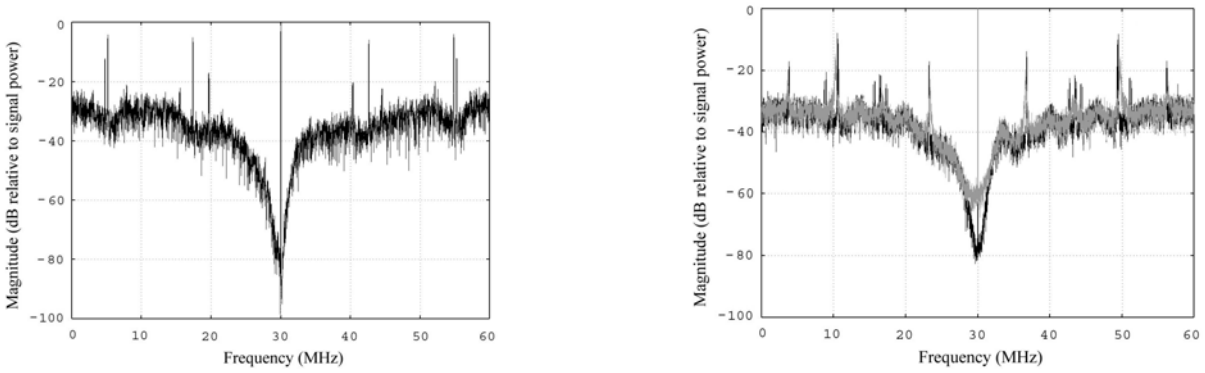


Fig. 10. Circuit implementation of the comparator and the one cycle digital delay.

of 30 MHz and a clock frequency of 120 MHz. The calculated SNDR is 95 dB, for a bandwidth of 10 kHz. At circuit level, thermal noise is not considered, due to the inability of the software design tool to include sources of thermal noise in a time-domain analysis. In order to complement this result, the presence of thermal noise and clock jitter have been simulated at system level. Fig. 11*b* shows the modulator output spectra including the effect of jitter (black curve) and including the effect of jitter and thermal noise together (light gray curve). The simulated jitter corresponds to that of a cheap commercial clock generator —e.g. timing jitter of 50 ps, phase noise of –100 dBc/Hz@10kHz—. We have assumed that jitter in pulse width is of the same order that jitter in sampling instants. If only jitter is considered, the SNDR obtained is 69 dB, which is quite above the required SNDR. If thermal noise is included then SNDR falls to 61.8 dB. It is clear that thermal noise is the most limiting factor of modulator performance, thus masking the effect of any other source of noise.

Fig. 12 plots the modulator output spectra (obtained from Spectre circuit-level simulations) for two different notch frequencies separated approximately 33% one from the other, obtained by changing the transconductance of all transconductors while maintaining a fixed f_s = 120 MHz (fine tuning). SNDR obtained is above 60 dB for both cases, for a notch-centered bandwidth of 100 kHz. Fig. 13 plots SNDR obtained by coarsely tuning the modulator in a number of frequencies within the 3-30 MHz range, by adequately switching the capacitors from the array. Again, we consider a notch-centered bandwidth of 100 kHz. This data has been also obtained from circuit-level simulations using Spectre. By examining Figs. 12 and 13, we can see that the proposed modulator covers the entire 3-30 MHz range with proper performance.



(*a*) (*b*)

Fig. 11. Modulator output spectra obtained via (*a*) circuit-level simulation and (*b*) system-level simulation, by taking a 2^{14}-point Hanning windowed FFT of the modulator output bit stream.

As expected, SNDR grows for high carrier frequencies because the bandwidth relative to sampling frequency decreases as the sampling frequency increases. Note that this does not contradict Fig. 6*a*, since there only thermal noise was considered.

Furthermore, note that the SNDR requirements are fulfilled for a bandwidth (100 kHz) much wider than the AM-SSB signal bandwidth specification (6 kHz). It can be seen as our proposed system provides certain tolerance to tuning inaccuracies. That is, even though, due to some detuning of the resonators, the notch of the NTF is deviated from the desired location (i. e., the signal carrier frequency), an SNDR higher than 60 dB can be obtained after filtering the modulator output signal.

Finally, via time-domain circuit-level simulation, we have estimated the modulator power consumption is 6 mW.

VII. Conclusion

We have presented a continuous-time fourth-order bandpass delta-sigma modulator implemented in a 0.35 μm triple-metal standard CMOS technology. The modulator achieves an SNDR higher than 60 dB for 10 kHz-bandwidth signals modulated on a carrier in the 3-30 MHz frequency range, while consuming only 6 mW. The modulator wide-band tuning capability makes it suitable to work as an RF receiver front-end, realizing A/D conversion of signals directly coming from the receiver antenna. In this paper, we suggest its use as a shortwave radio receiver front-end. System-level and circuit-level simulation results have been given.

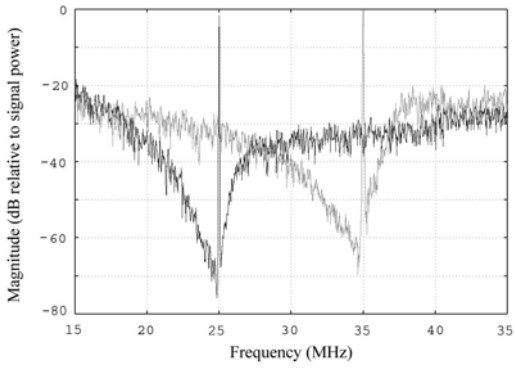


Fig. 12. Modulator output spectra for two distinct notch frequencies, obtained by means of fine tuning of the modulator. An average of four 2^{14}-point Hanning windowed FFTs of the modulator output bit stream was used. Circuit-level simulations using Spectre.

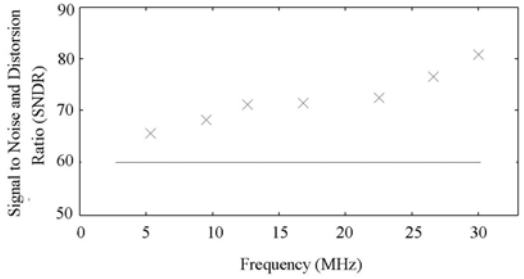


Fig. 13. SNDR obtained for different notch frequencies set by means of coarse tuning. Circuit-level simulations using Spectre.

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