Delta-Sigma ADCs for High Speed Data Communications

17th May 2006

SRC Contract: 2004-HJ-1198
Task Title: Delta-Sigma ADCs for High Speed Data Communications
Task Leader: Jesús Arias
Principal investigator: Jesús Arias
ITRS Grand Challenge: 12
Deliverable Report:

- Overall ADC simulation.
- Design of a test chip including the ADC and test-related logic. (Preliminary)

Abstract

This report describes the complete ΔΣ modulator, including the layout of a test chip and the simulation results obtained from the extracted circuit from the layout. This extracted circuit includes the expected parasitic capacitances related to routing, and, therefore, the results describe better the expected performance of the real circuit. These simulations include results for different technology corners, temperatures and the effect of mismatches. In all cases the specifications are meet. Finally, an schematic circuit for chip testing is proposed.

Technical results and data

In Figure 1 an schematic of the test chip is shown. This chip includes the ΔΣ modulator along with the required blocks for testing, namely, a clock buffer, a serial input register and three serial-to-parallel data converters. The purpose of these last converters is to lower the data rate from 1GHz to 125MHz, allowing the connection of moderate-speed equipment to the output. The layout of the test chip is shown in Figure 2 along with the location of its most significant blocks.

A circuit netlist has been extracted from the layout using Assura in its "coupled" capacitance mode that includes parasitic capacitors between nodes, not only to ground. A set of simulations were carried out using this netlist. In Figure 3 the three most significant technology corners were simulated and the corresponding results shown along with the obtained performance. In all cases, the resolution is higher than 7 effective bits (43.9 dB of SNR). Although two harmonics are observed, their amplitudes remain well below the resolution of the converter. The second harmonic is not present in schematic simulations (due to the differential structure of the circuit) and, therefore, it has to be related to some imbalance in the layout. The typical estimate for power consumption is 8.8mW.

The circuit performs well under a wide range of temperature. The simulated results are shown in Figure 4. The specifications are meet from -30^{o}C to +125^{o}C.

The effect of device mismatches is also investigated. In the simulations of Figure 5 mismatch variations are included in all MOSFET devices and capacitors. Mismatches in DAC's elements will result in nonlinearity and an increased noise floor, but these effects can be overcome using the DWA scrambler. As can be seen in Figure 5, the results obtained with the scrambler enabled are close to those of a modulator without mismatches in their devices, while, if the scrambler is held in a reset state, the distortion increases, mainly that of the second harmonic, and the noise floor raises, filling in the NTF notch.

Finally, the test chip will be included in a prototype board along with some other components for its characterization. A proposed schematic for this board is shown in Figure 6. The differential input signal is obtained using a single-ended to differential converter. The differential 1GHz clock signal is generated from a single-ended sine-wave source using transmission lines with different lengths. The output data is recorded in a FIFO memory running at 125 MHz. In this way, we can record the output data at full speed and then recover the data from the FIFO memory at a much lower speed using a general-purpose digital interface to a computer for its further processing.

This chip prototype will be sent for fabrication at the beginning of June 2006.

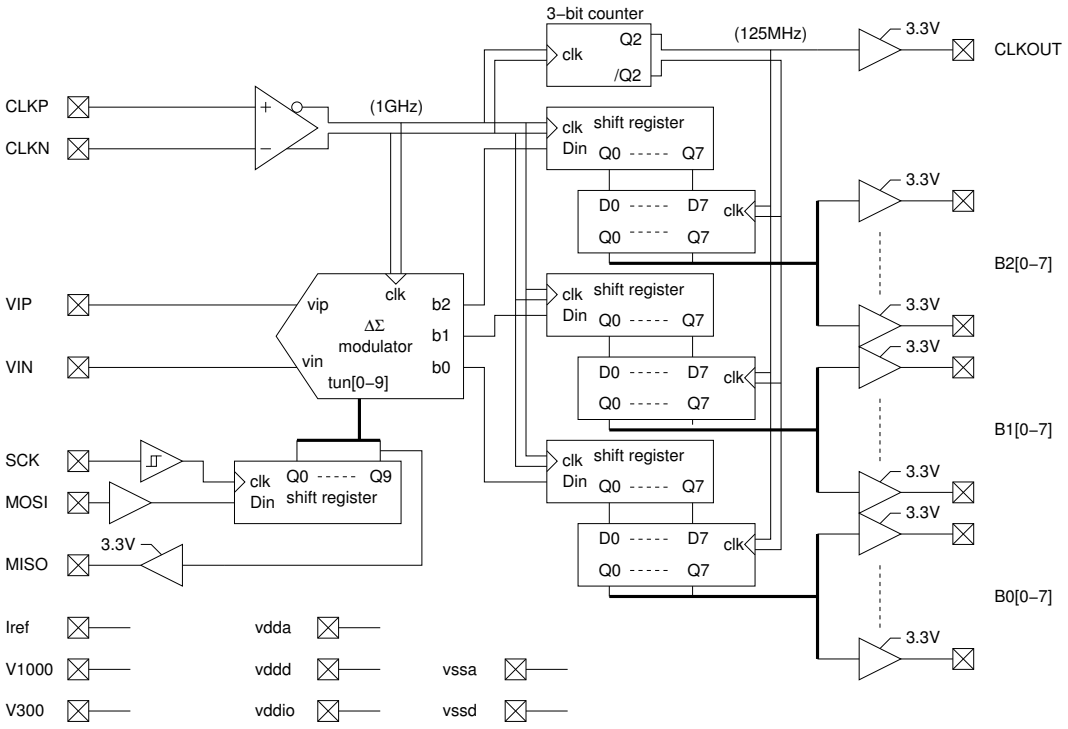


Figure 1: Block diagram of the complete test chip for the ΔΣ ADC.

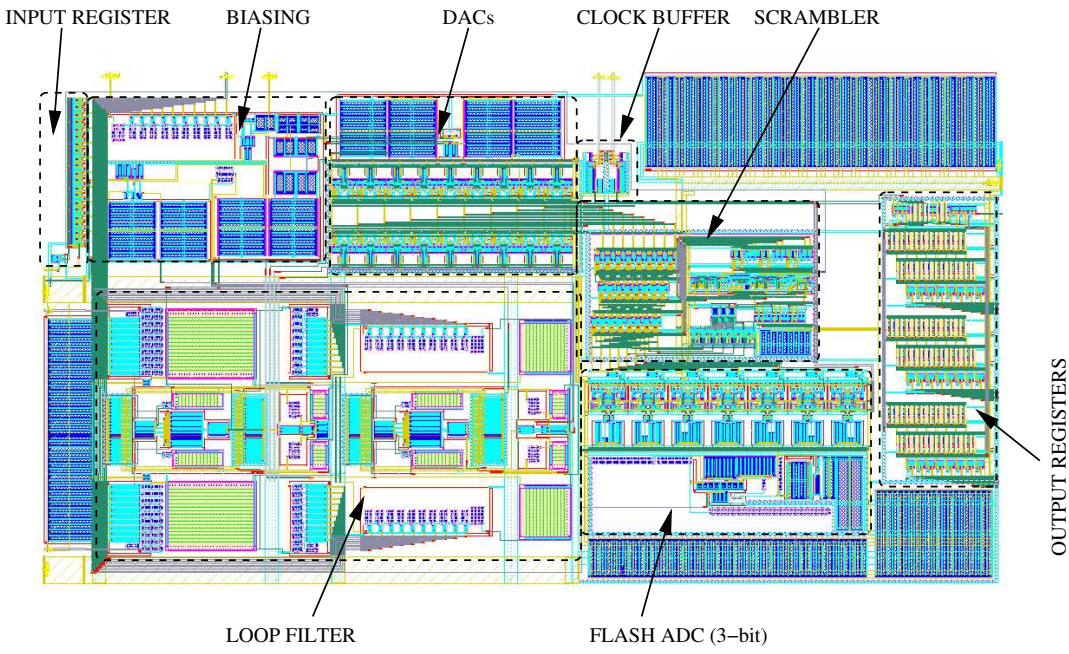
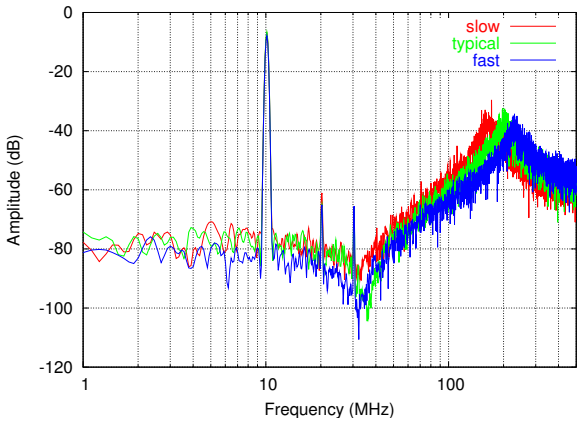


Figure 2: Layout of the test chip showing the placement of main blocks.



Corner	slow	typical	fast
SNR (dB)	44.3	47.7	49.3
2^{nd} Harm (dBc)	–53.5	–57.6	–56.9
3^{rd} Harm (dBc)	–64.4	–59.3	–57.5
Power (mW)	7.9	8.8	9.9

Figure 3: Simulated output spectra for three technology corners and resulting performance.

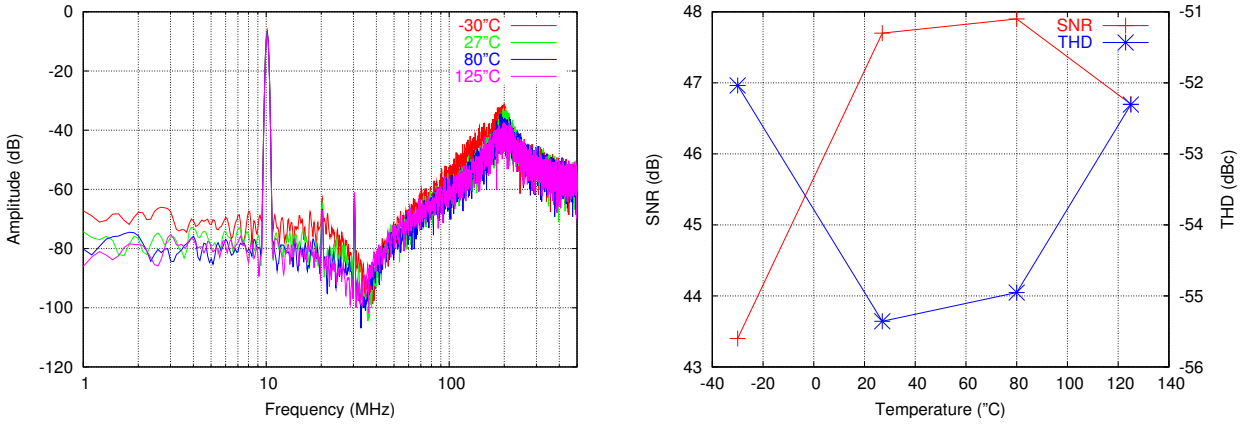
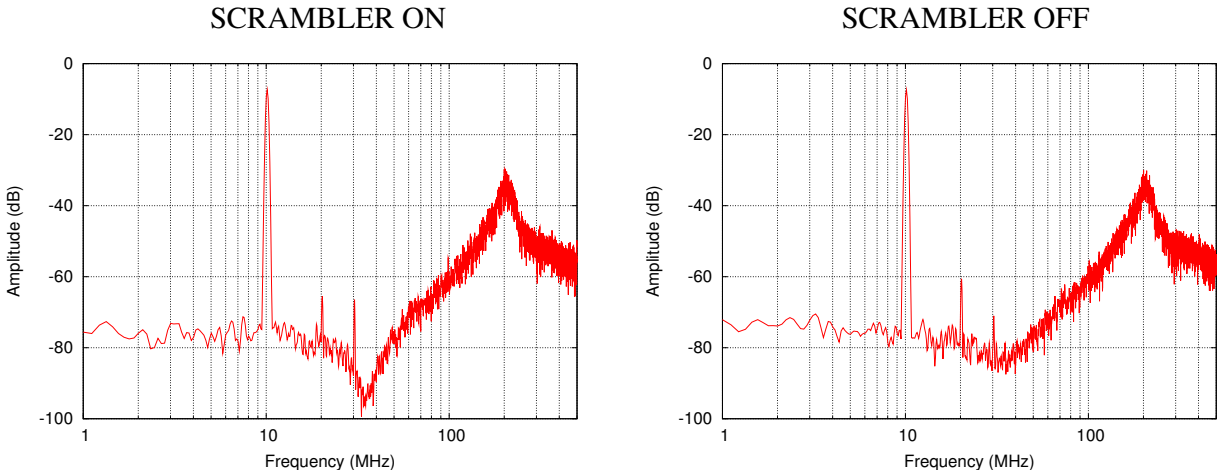


Figure 4: Simulated output spectra for different temperatures.

Mismatch on all extracted MOSFETS (N & P) and CID capacitors



SNR: 46.2 dB
2nd harm. distortion: −57.1 dBc
3 rd harm. distortion: −58.8 dBc

SNR: 45.6 dB
2nd harm. distortion: −52.8 dBc
3 rd harm. distortion: −62.4 dBc

Figure 5: Simulated output spectra including device mismatches with the scrambler on and off.

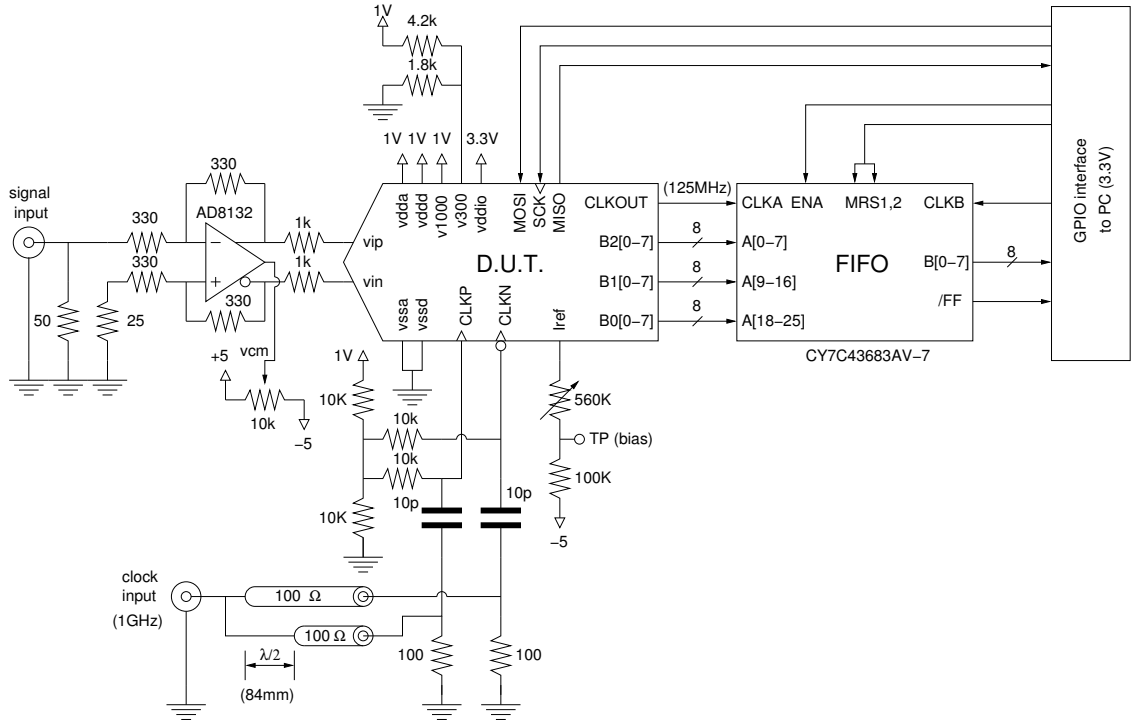


Figure 6: Proposed schematic of the PCB board for chip testing.