Semiconductor Research Corporation

Delta-Sigma ADCs for High Speed Data Communications

Task ID# 1198.001

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SRC Students

⇨ David Bisbal, UVA, PhD in progress.

⇨ Jacinto San Pablo, UVA, PhD in progress.

Industrial Liaisons

Customized SRC project:

Primary Anticipated Result

A delta-sigma ADC for High speed data communications (Gigabit Ethernet) will be designed and its performance will be tested to meet the required specifications.

Summary of Task's Deliverables

- ⇨ Architectural analysis of the propossed converter, development of the software for system-level simulations and system-level simulations. (Nov. 2004)

- ⇨ Circuit-level design and simulation of the different functional blocks composing the modulator: integrators, embedded flash ADC and DAC, and digital logic. (May. 2005)

Publications & Software

⇨ Conference Presentation:

“Noise Simulation of Continuous-Time Sigma-Delta Modulators”
J. Arias, L. Quintanilla, D. Bisbal, J. San Pablo, L. Enriquez, J. Vicente and J. Barbolla.
ICNF 2005. Salamanca (Spain) Sep. 19th-23rd.

⇨ Software description:

system-level simulator for continuous-time sigma-delta modulators

✔ Version 1 (Nov. 2004): Gm-C based modulators

✔ Version 2 (May. 2005): Opamp based modulators are also included.

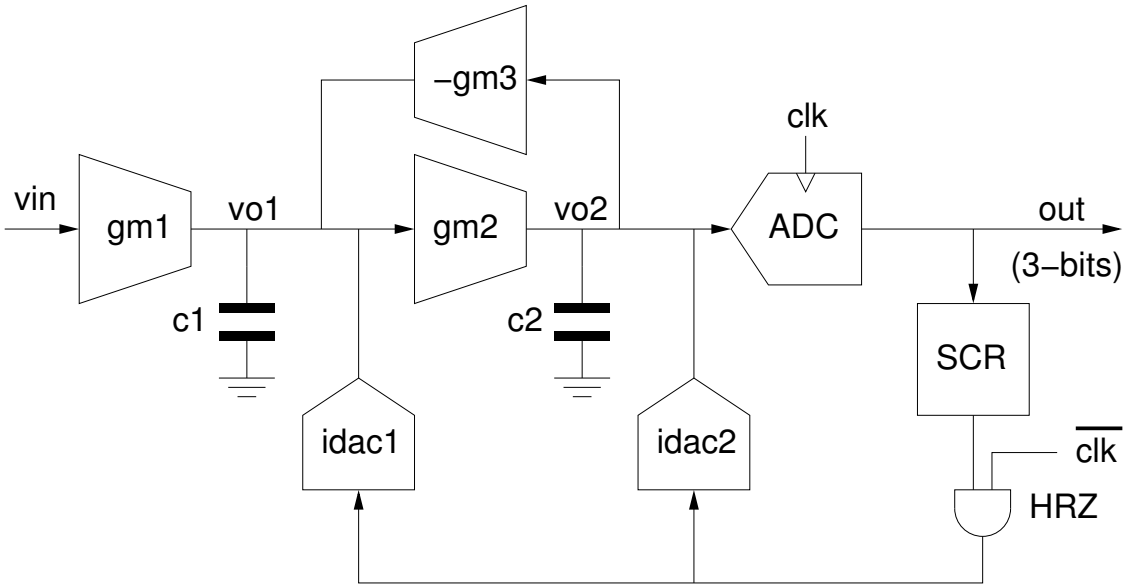
Delta-Sigma ADCs for High Speed Data Communications

1^{st} *deliverable*

Due Date: November 2004

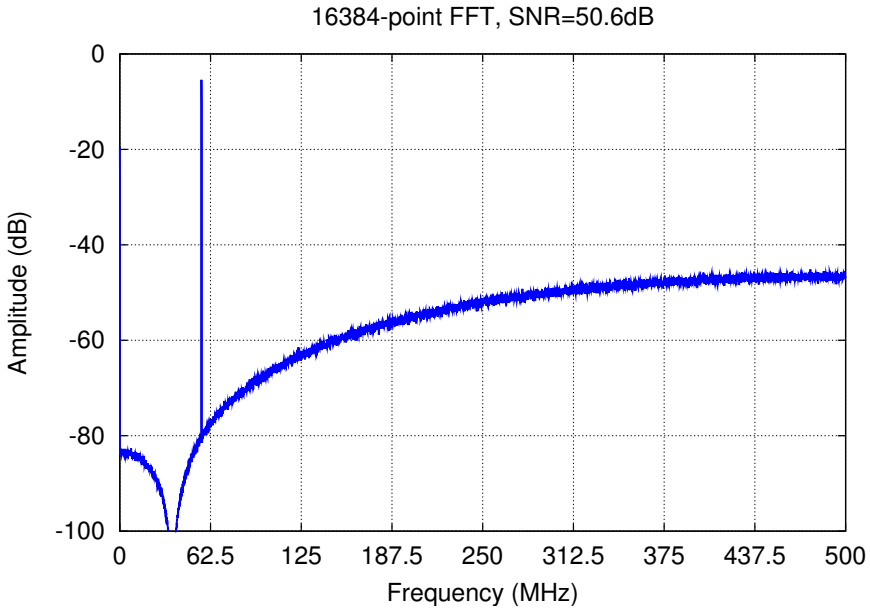
Architectural analysis of the proposed converter, development of the software for system-level simulations and system-level simulations.

Gm-C based, Continuous-Time, multibit ΔΣ modulator



- Second–Order loop filter
- 3–bit quantizer
- Oversampling ratio of 8
- Optimal zero placement
- Gm–C based integrators

- 90nm CMOS technology
- 1 GHz clock frequency
- 62.5 MHz signal bandwidth
- ~50 dB of SNR
- 8 effective bits of resolution



System level simulator for CT $\Delta\Sigma$ modulators

Main features:

- Quick simulations (seconds).

- Performance analysis: SNR and distortion extraction.

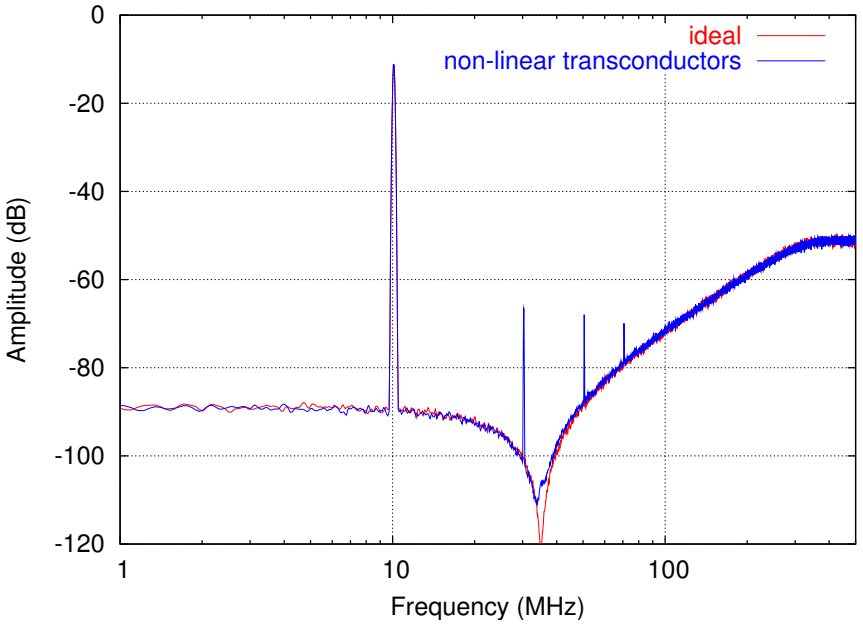
- Parameter sweep and Monte Carlo simulations.

- Many real effects included.

Nonlinear Gm	Clock jitter
Finite integrator gain	Nonlinear ADC
Nondominant pole	Metastability in ADC
Variable output resistance of DACs	Hysteresis in ADC
Dynamic range scaling	Nonlinear DACs
Thermal noise	DWA scrambler
1/f noise	Loop delay

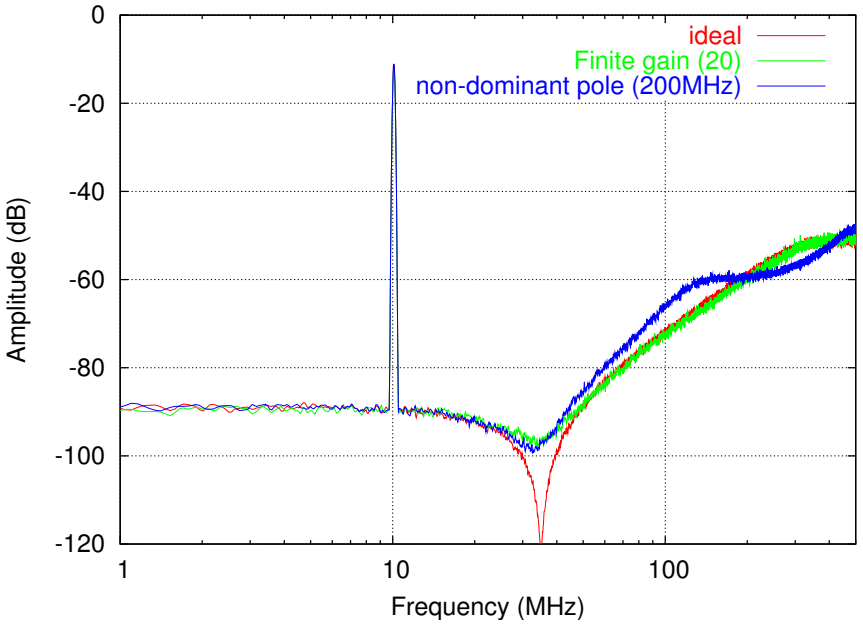
Nonidealities in Transconductors

Nonlinearity



THD = –53dBc

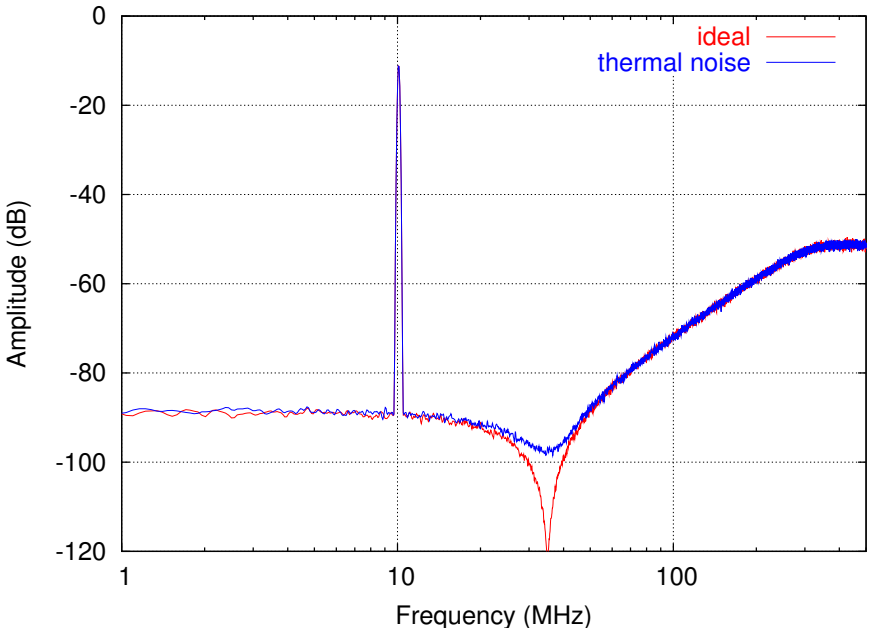
Finite Gain and nondominant pole



SNR=51.7 dB SNR=50.1dB

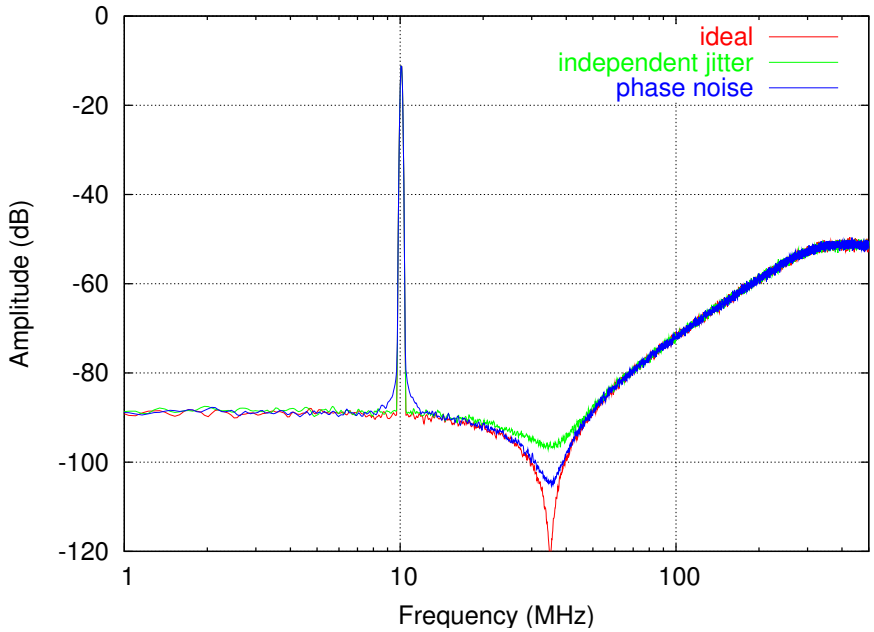
Noise & Jitter

Thermal Noise



SNR=52dB
(C1=0.5pF, C2=0.1pF)

Clock Jitter

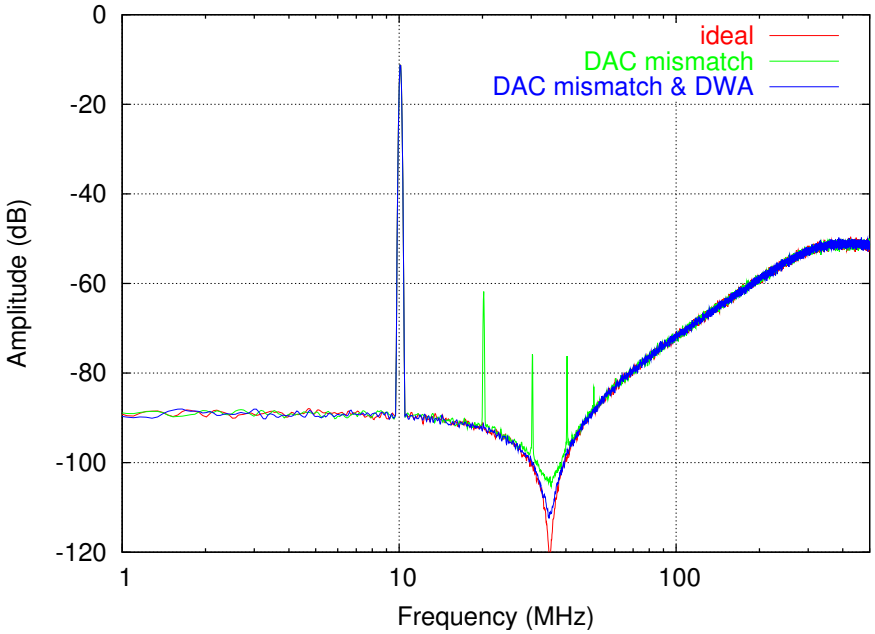


SNR=51.8dB
(Jitter=1ps)

SNR=52.2dB
(phase noise=
–90dBc/Hz @ 1MHz)

Nonidealities in the Quantizer

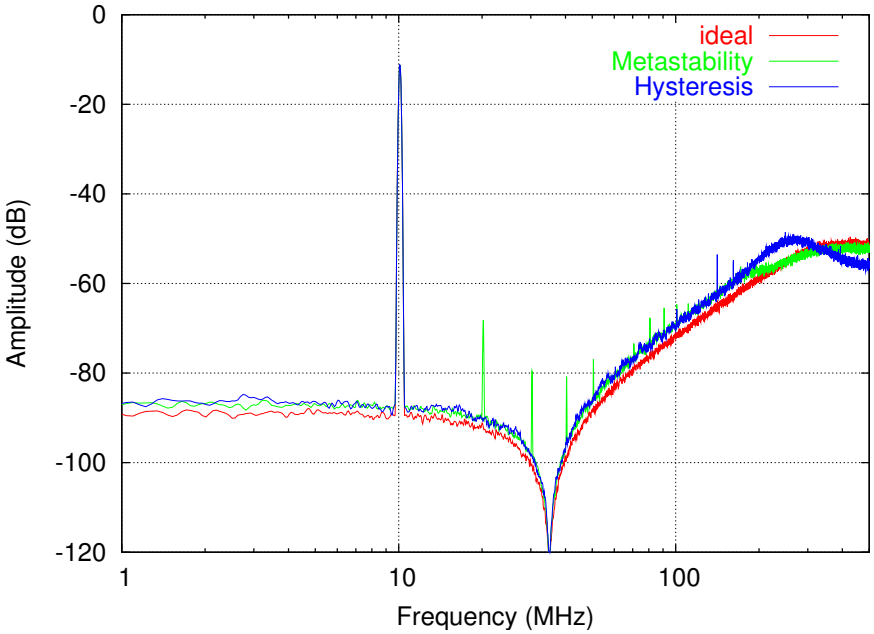
Mismatches in DACs



THD=–50.5dBc THD negligible

(1% element mismatch)

Flash ADC Effects

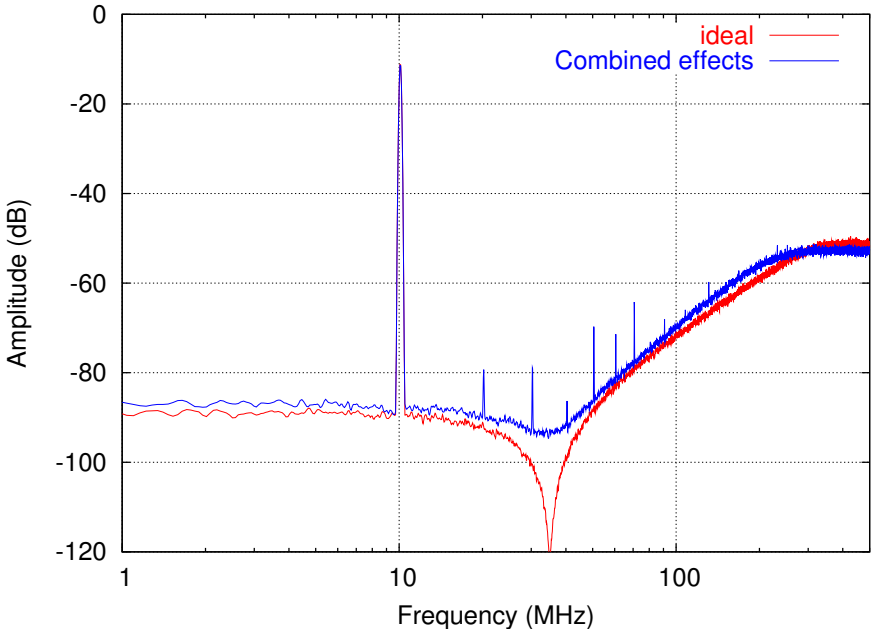


THD=–56dBc, SNR=50.3dB (τ=500ps)

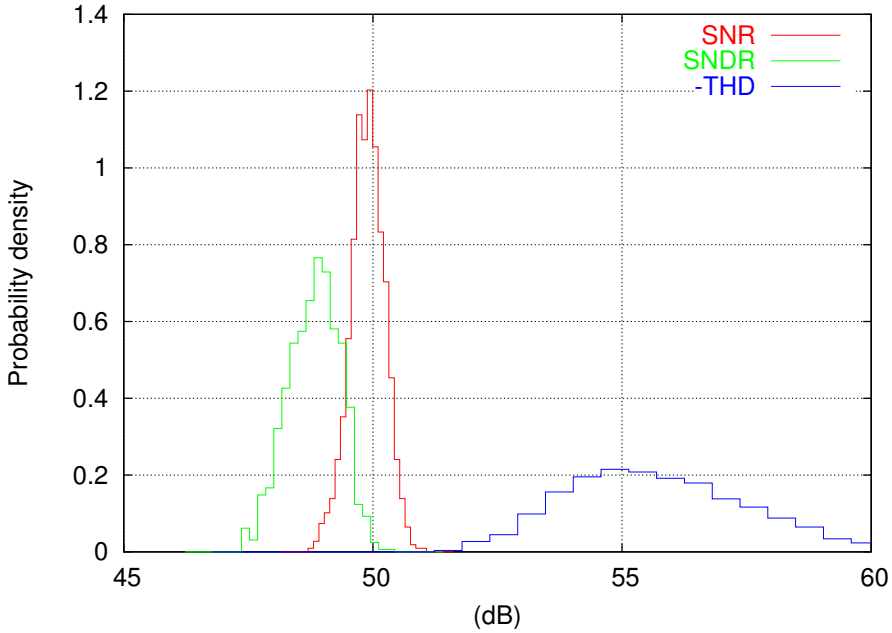
SNR=49.8dB (Vhyst=30mV)

Combination of effects and Monte Carlo

Combined effects

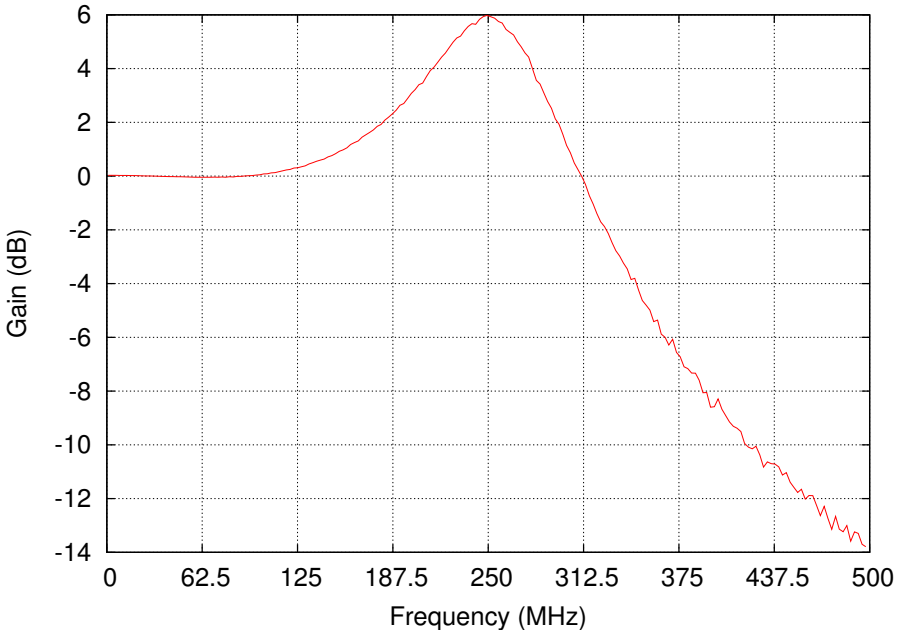


Monte Carlo simulation

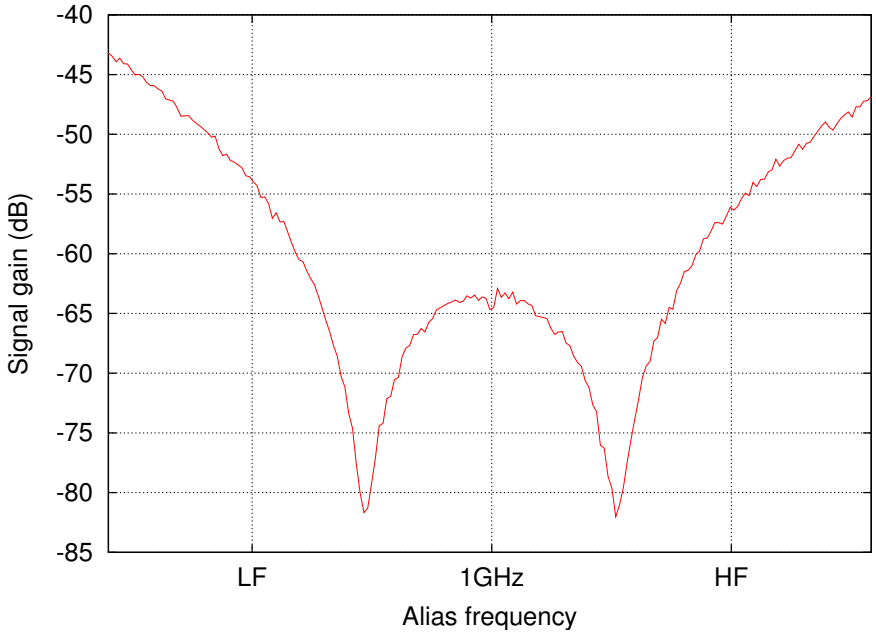


Signal-related performance

Signal Transfer Function (STF)



Alias freq. rejection



Delta-Sigma ADCs for High Speed Data Communications

2^{nd} deliverable

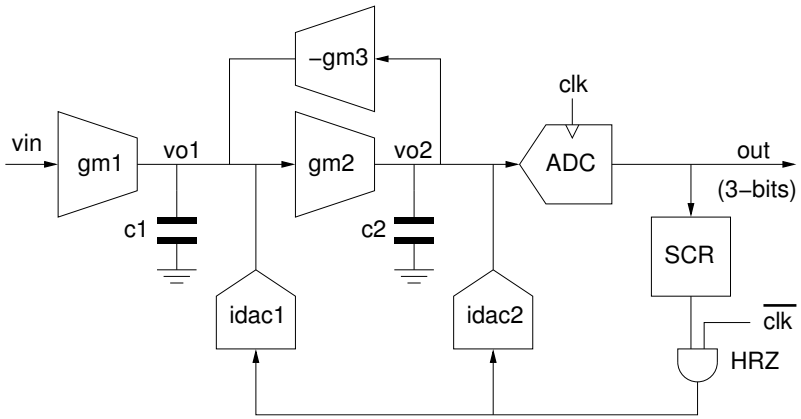
Due Date: May 2005

Circuit-level design and simulation of the different functional blocks composing the modulator: integrators, embedded flash ADC and DAC, and digital logic.

Significant change in research direction

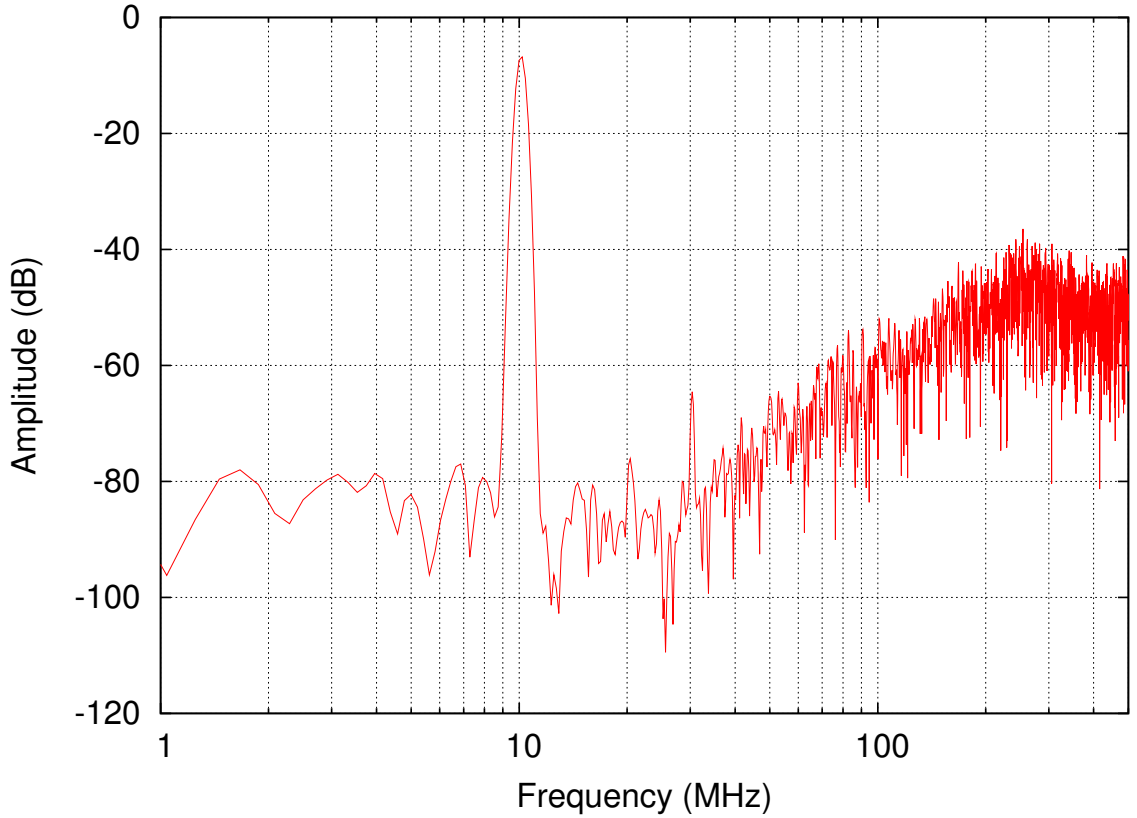
⇨ Gm-C based modulators have several drawbacks

- ✔ Transconductor nonlinearity⇒ Distortion.
- ✔ Low output impedance in transconductors ⇒ Low DC gain⇒High in-band quantization Noise.
- ✔ Low output impedance in DACs ⇒ Distortion, higher quantization Noise
- ✔ Parasitics ⇒ Detuning, Distortion



Gm-C modulator. Simulation

Ideal transconductors and biasing sources.



- Too high noise floor (SNR=48dB)

- Some distortion still present (3^{rd} har. = -58dBc)

Gm-C modulator. Design issues

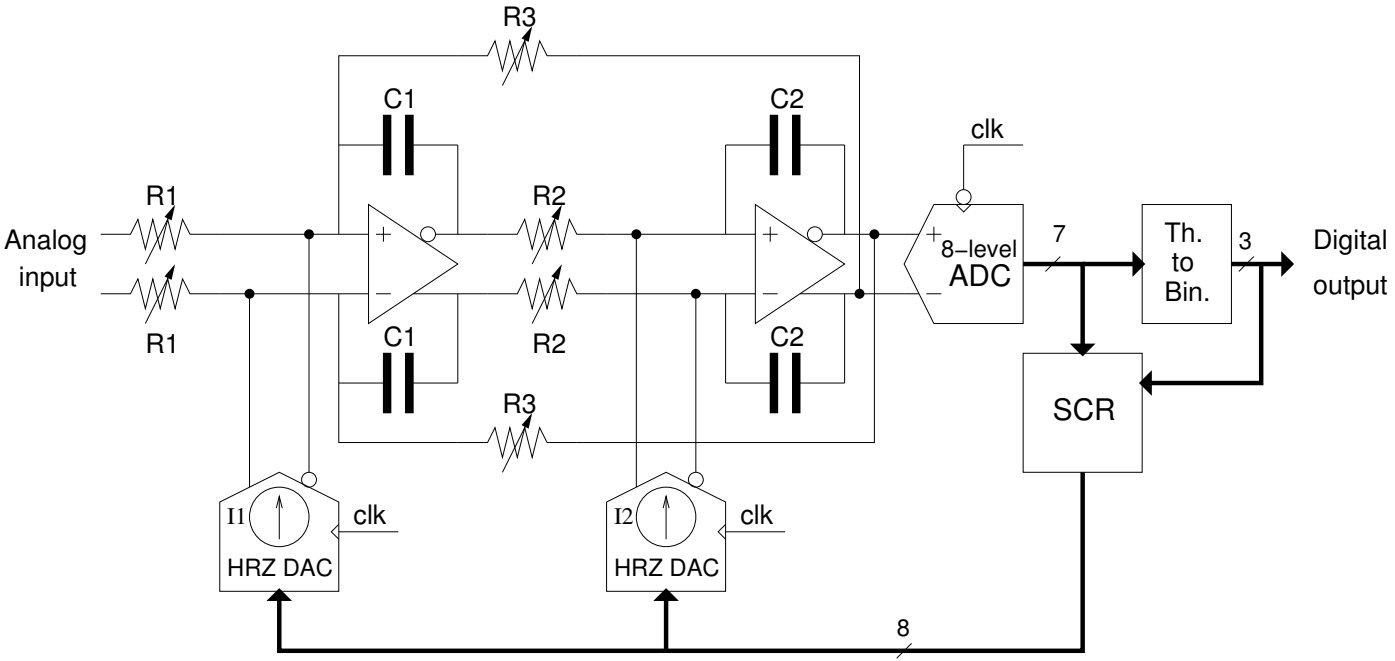
⇨ It is difficult to design current-mode DACs with the required specs with only 1 volt supply.

⇨ Not enough voltage room for cascode structures.

⇨ Transconductors and biasing sources will further degrade the performance. (Low output resistance)

⇨ Parasitic capacitances are a substantial fraction of the total integration capacitance and they are highly nonlinear.

New modulator architecture



- DACs are connected to low impedance nodes.

- Voltage swing at DAC outputs is small.

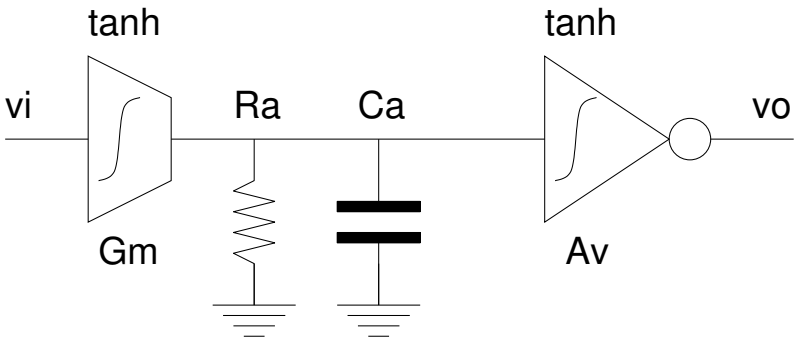
- Parasitics are not included as integration capacitances.

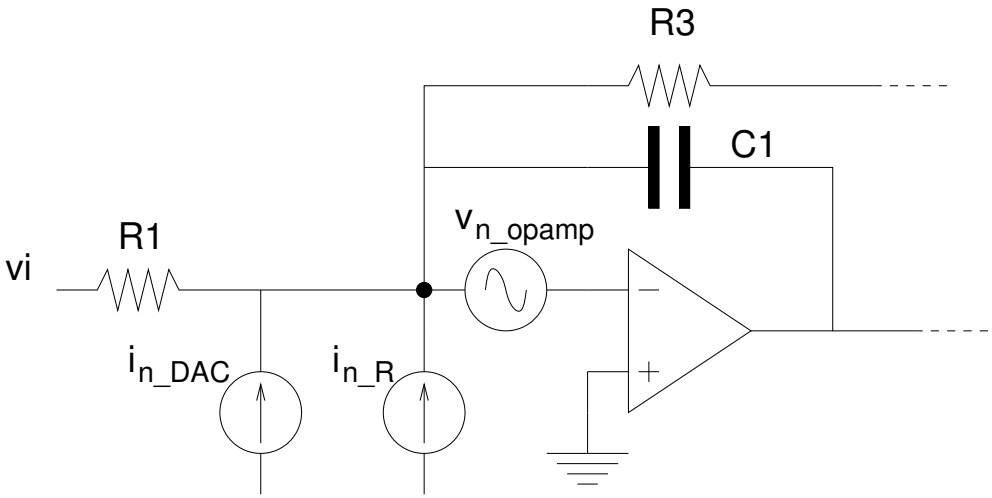
- Feedback improves linearity.

- Penalty: higher power consumption.

System-level simulations

Opamp modeling (single-ended):





- Nonlinear transfer function.

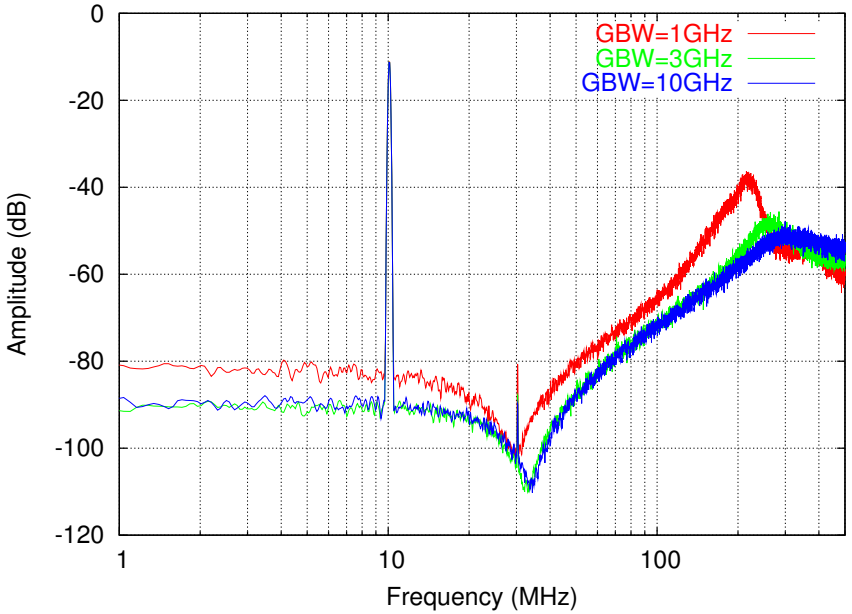
- Finite DC gain.

- Finite Gain-Bandwidth product.

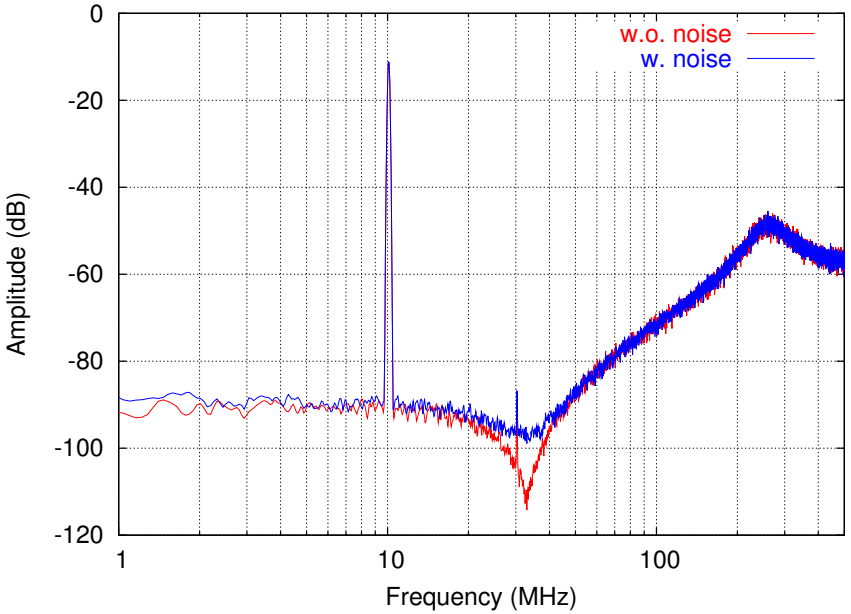
- Thermal and 1/f noise

System-level simulations

Opamp's GBW effect



Thermal & 1/f noise effect

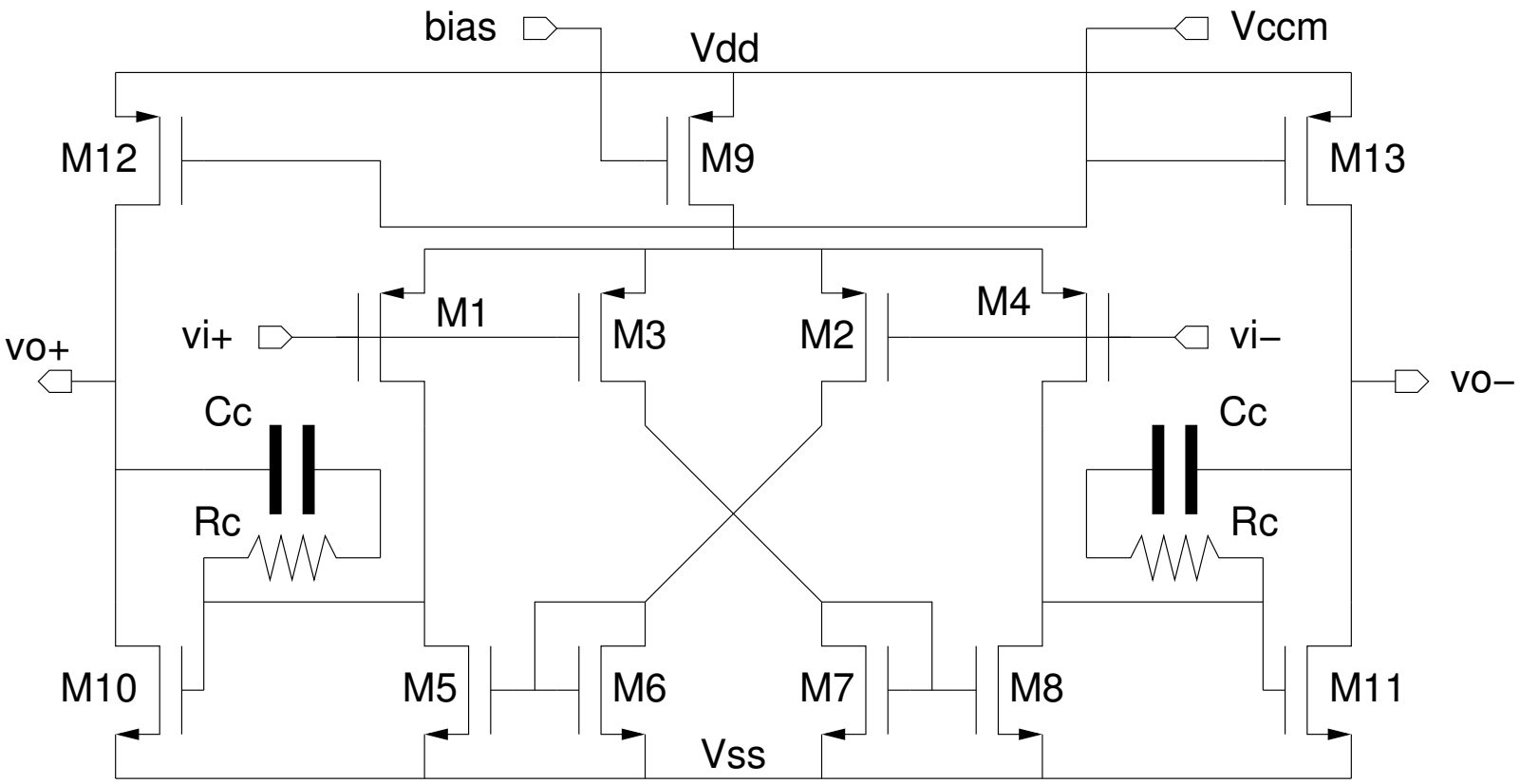


Requirements:

- Opamps with GBW $\approx$ 3GHz

- Integrating capacitors: C1=0.5pF, C2=0.2pF (1dB loss of SNR)

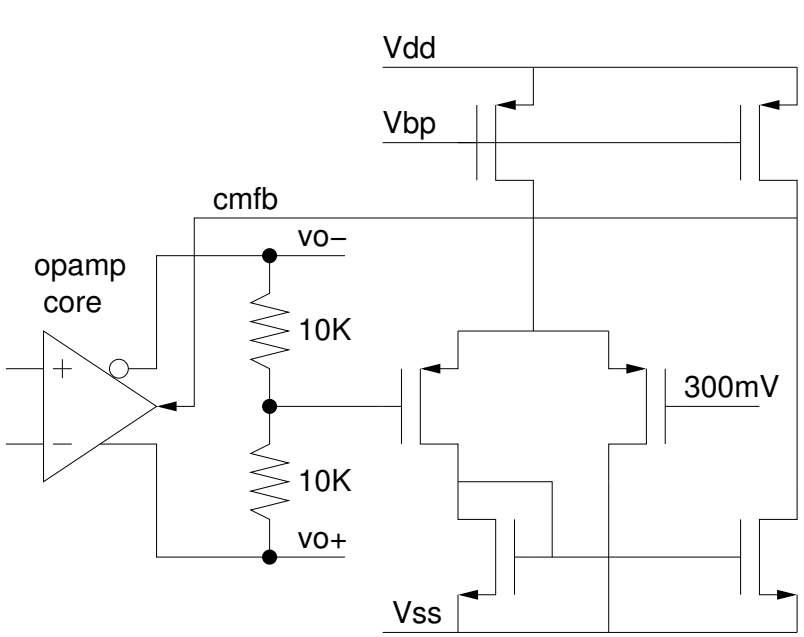
Opamp-based modulator. Opamps

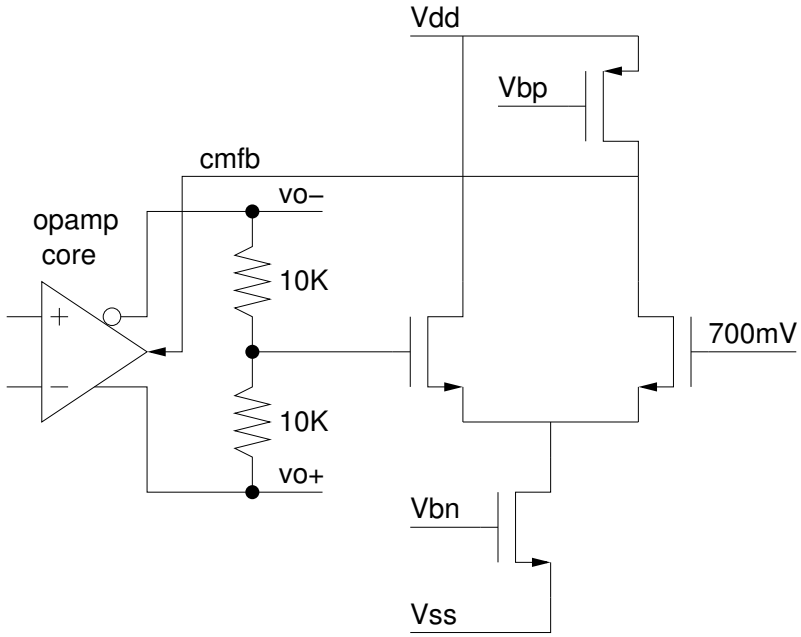


- Main spec: GBW > 2GHz. Load capacitance: 0.5pF.

- Current consumption ≈3mA

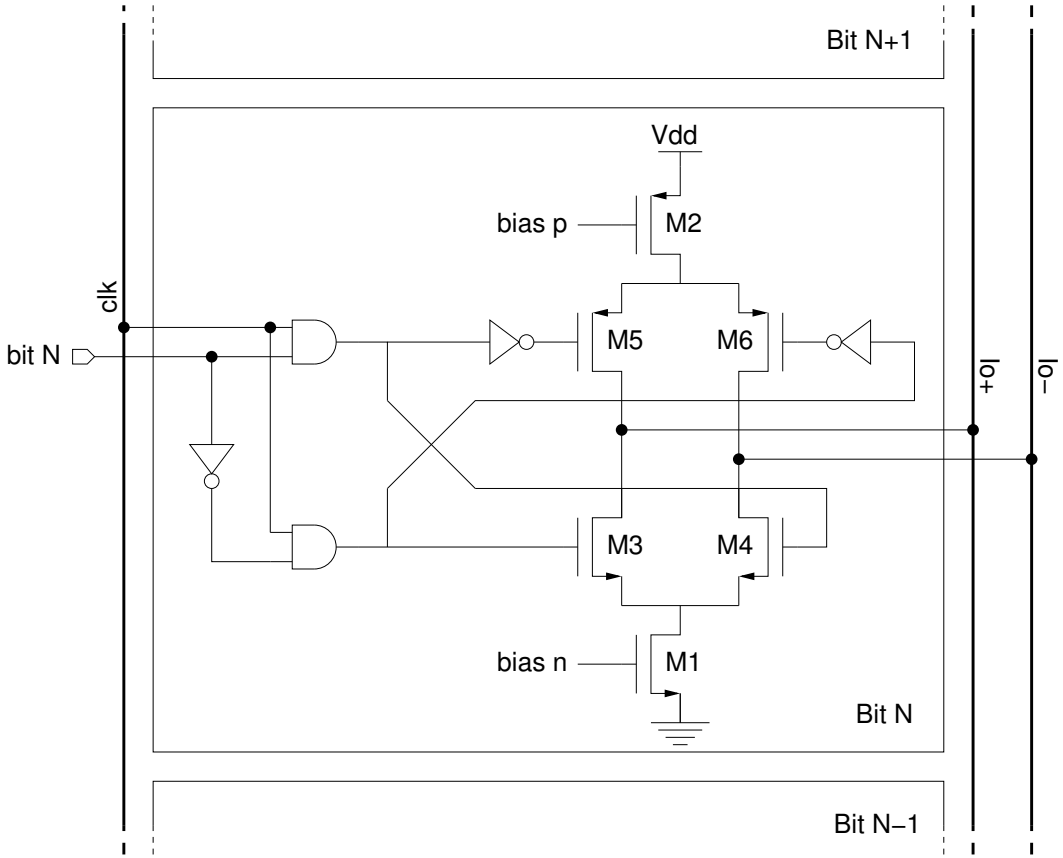
Opamp-based modulator. CMFB circuits





- Different CM voltages through the modulator. (efficient use of N-channel devices in opamps)

Opamp-based modulator. DACs

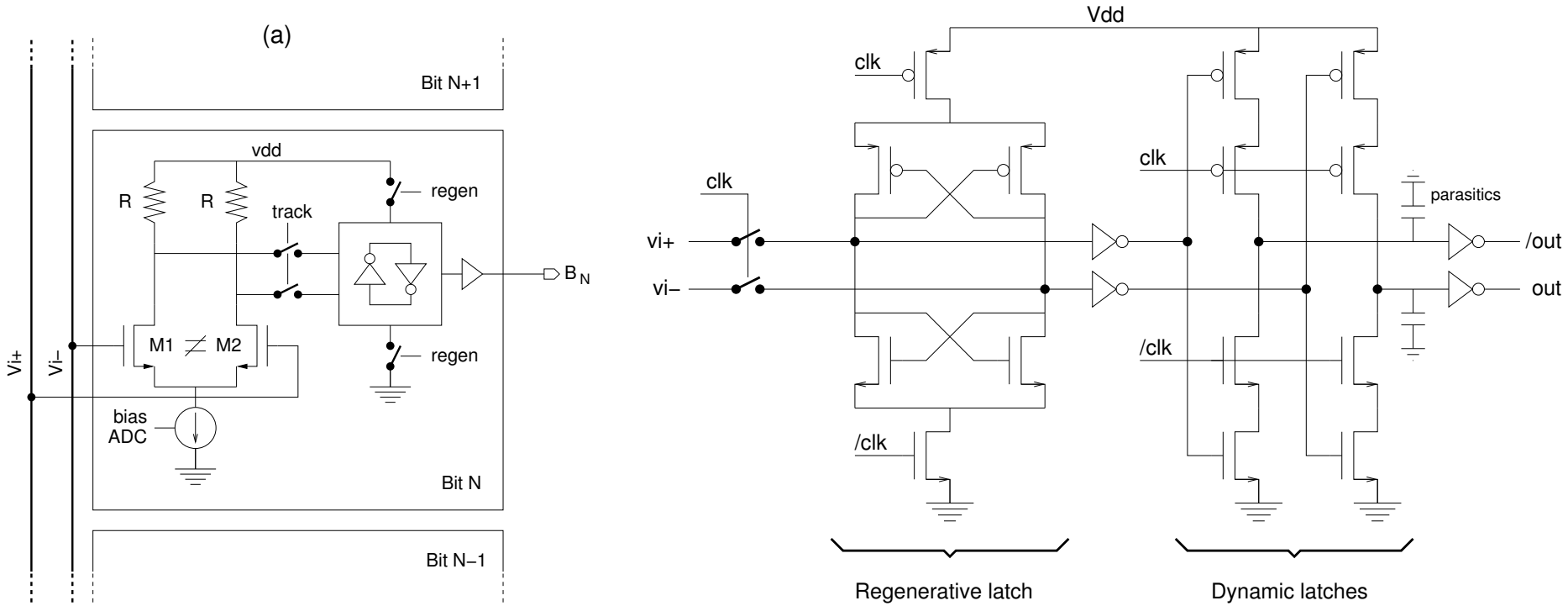


- Simple, bipolar output, DAC.

- High enough output impedance without cascodes.

- Small devices $\Rightarrow$ mismatch. Corrected via DWA scrambler.

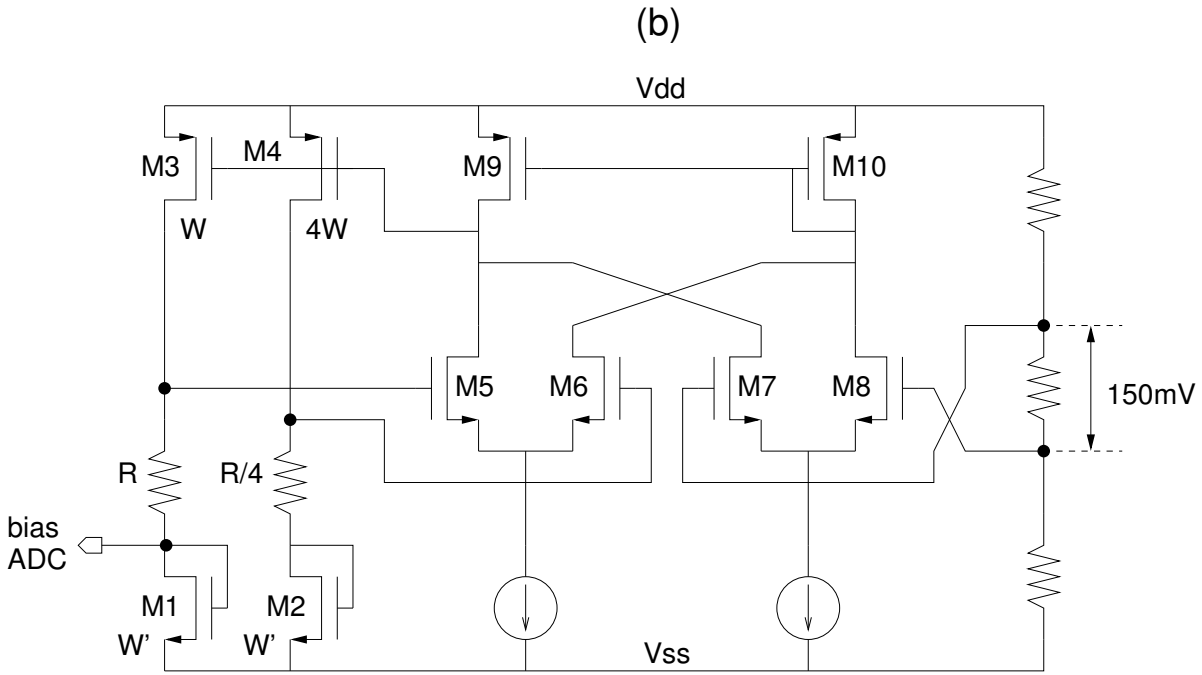
Flash ADC



- Preamp: variable threshold voltage obtained by using different input transistors.

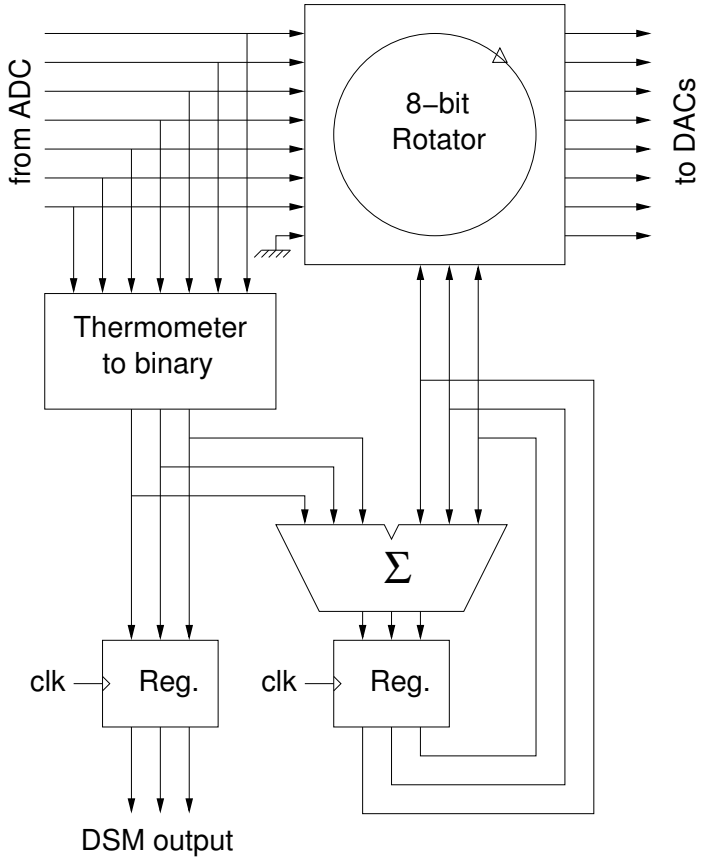
- Fast regenerative latch ($\tau = 30ps$).

Flash ADC. Biasing



- $(V_{GS} - V_{TH})$ independent of process variations and temperature $\Rightarrow$ Constant LSB voltage.

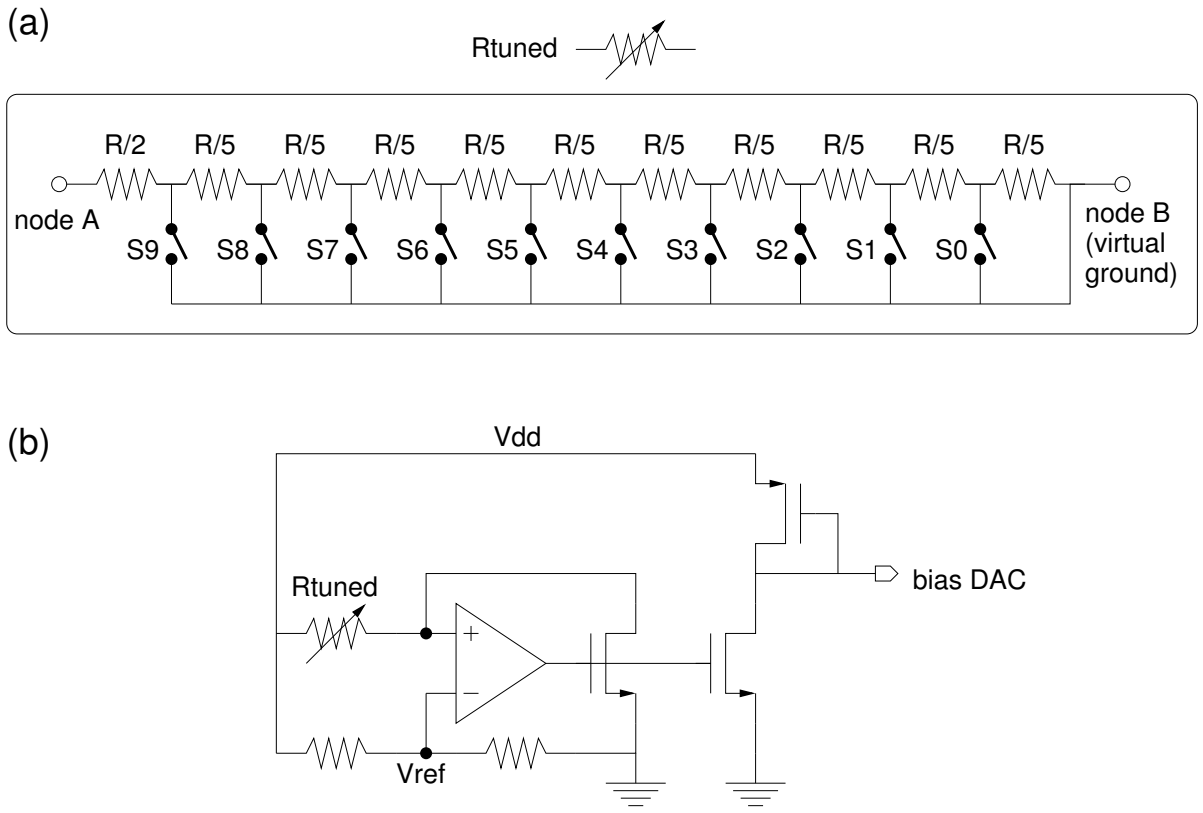
Mismatch correction. DWA scrambler



- Dynamic element matching for DACs.

- Mismatch errors are translated to a shaped noise floor.

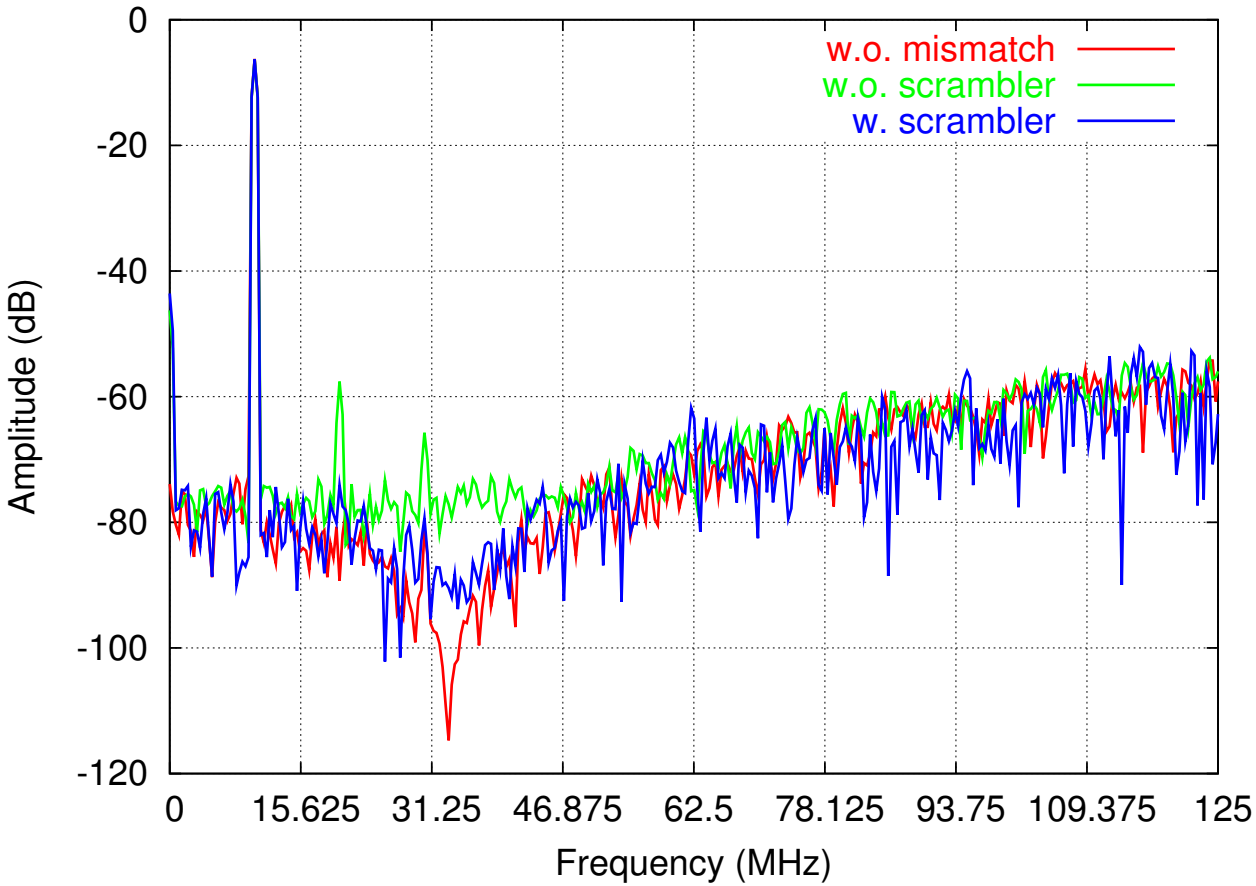
Tuning against process variations



(a) Resistors with switchable portions allow for the digital tuning of the modulator.

(b) DAC's currents are kept proportional to 1/R

Transistor-level simulations (full circuit)



Results for simulation including mismatch and scrambler:

SNR = 50.8dB SNDR = 50.3dB

Total power = 7mW

Summary

- A $\Delta\Sigma$ modulator for Gigabit Ethernet has been designed.

- System-level and transistor-level simulations show that the modulator meets the design specs.

Next deliverables

- Layout of functional blocks.

- Simulations including parasitics from extracted circuits.