A Dual-Mode, Complex, $\Delta\Sigma$ ADC in CMOS for Wireless-LAN Receivers

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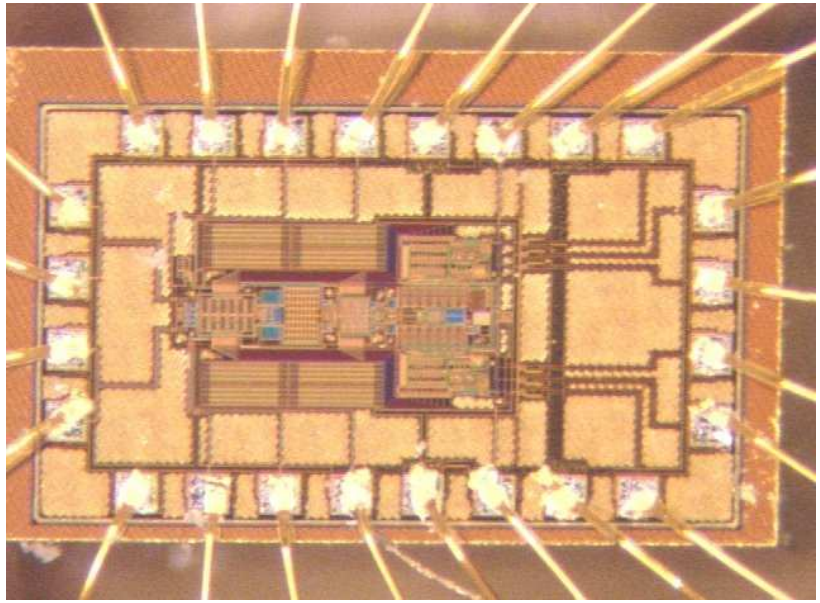

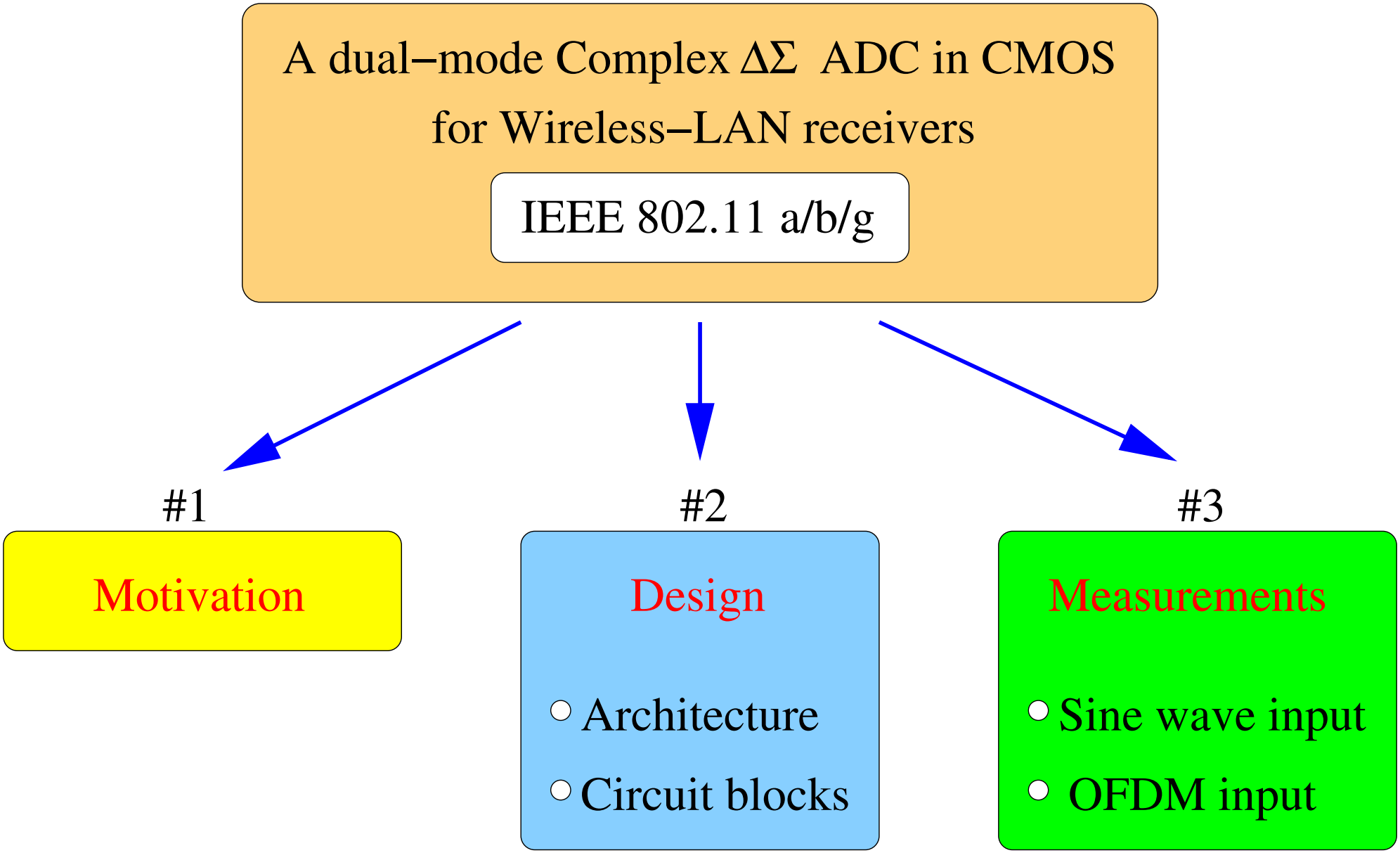
A dual–mode Complex ΔΣ ADC in CMOS
for Wireless–LAN receivers
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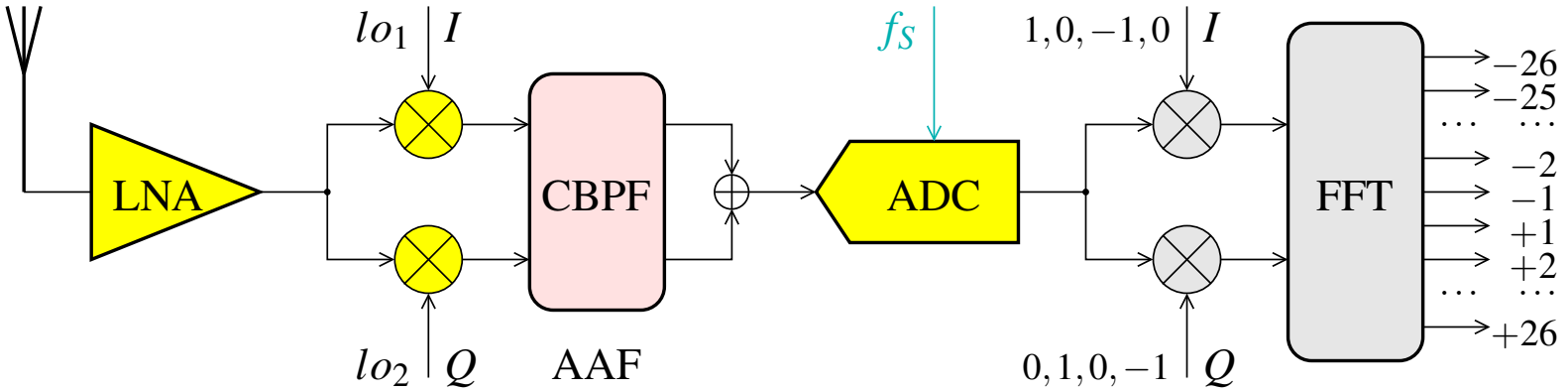
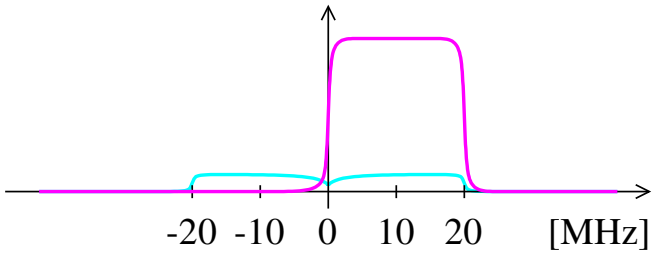
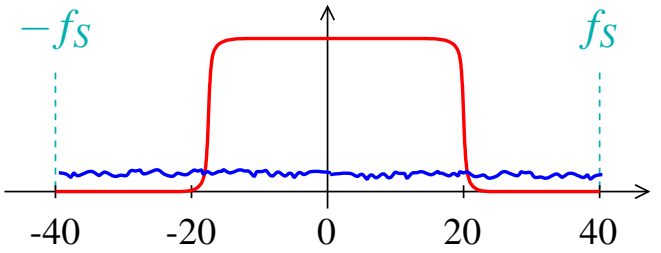
OFDM input

IEEE 802.11a/g, low-IF, receiver with Nyquist-rate ADC







Complex BPF ($1\times$):

$BW = 20$ MHz, $f_{IF} = 10$ MHz

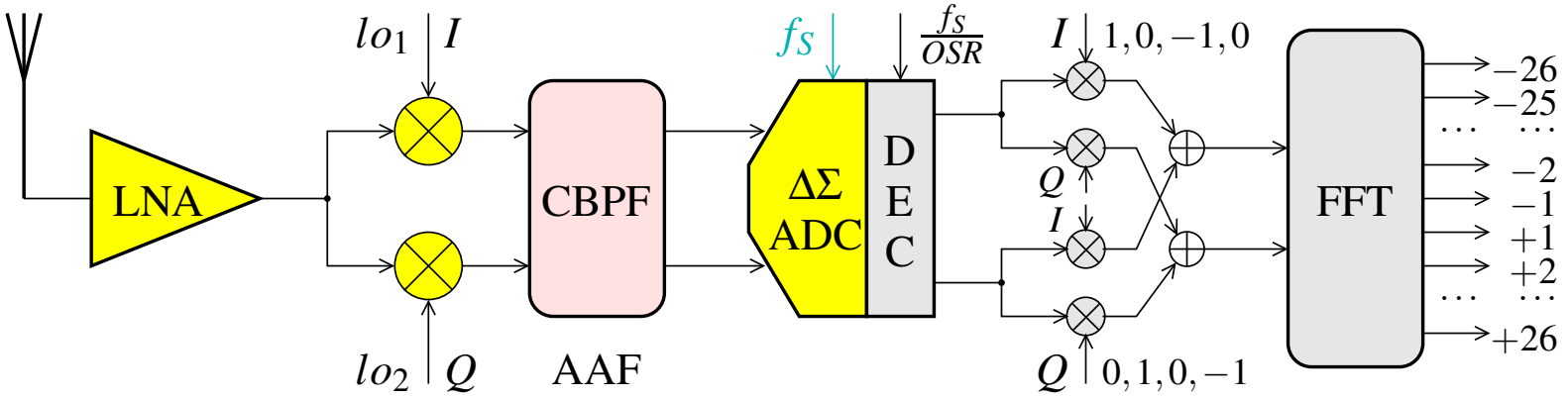
7-pole Chebyshev filter

Nyquist ADC ($1\times$):

$BW = 20$ MHz, $SNDR = 55$ dB

10-bit pipelined ADC

IEEE 802.11a/g, low-IF, receiver with ΔΣ ADC



Complex BPF:

$BW = 20$ MHz, $f_{IF} = 10$ MHz

3-pole Butterworth filter

Complex CT ΔΣ ADC:

$BW = 20$ MHz, $SNDR = 55$ dB

2nd-order 3-bit 16× oversampled

Proposed architecture

$\Delta\Sigma$ Architecture selection

⇨ Continuous-time (CT):

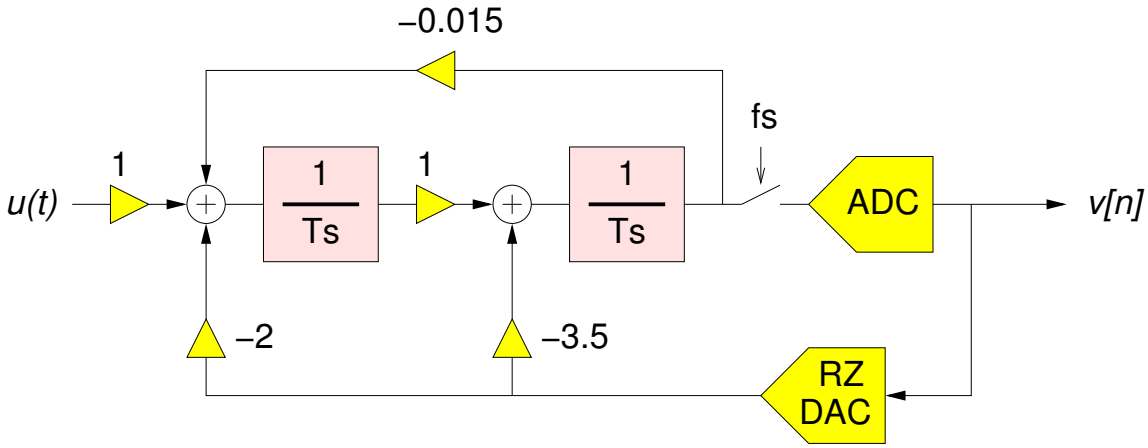
- ✔ Capable of operation at high sampling frequencies.
- ✔ Low power consumption.
- ✔ Implicit anti-aliasing property.

⇨ Multibit:

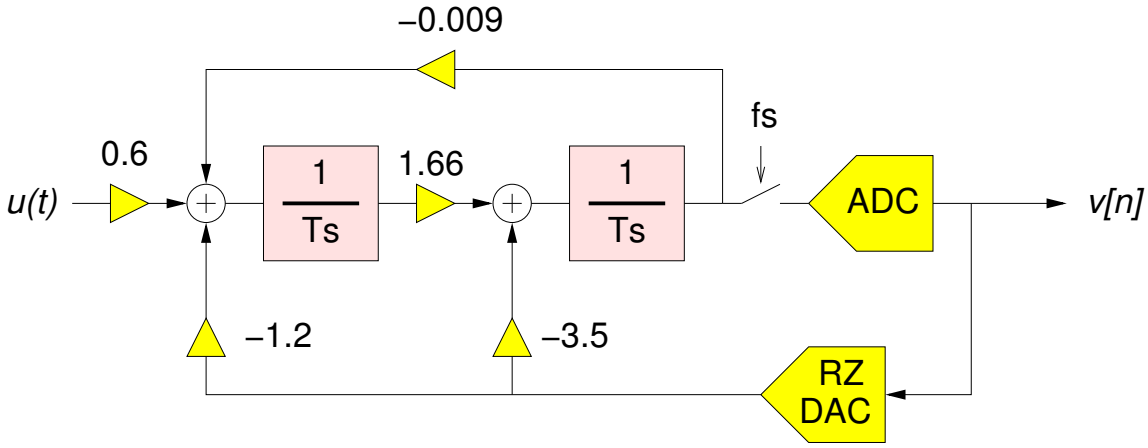
- ✔ Good SNR for low oversampling ratios. (16)
- ✔ Good stability.
- ✔ DAC mismatches can be overcome using the Data Weighting Algorithm.

Modulator architecture (Real $\Delta\Sigma$)

Starting modulator



After amplitude equalization



– Oversampling ratio of 16

– Second–order NTF

– Optimized zero: +3dB SNR

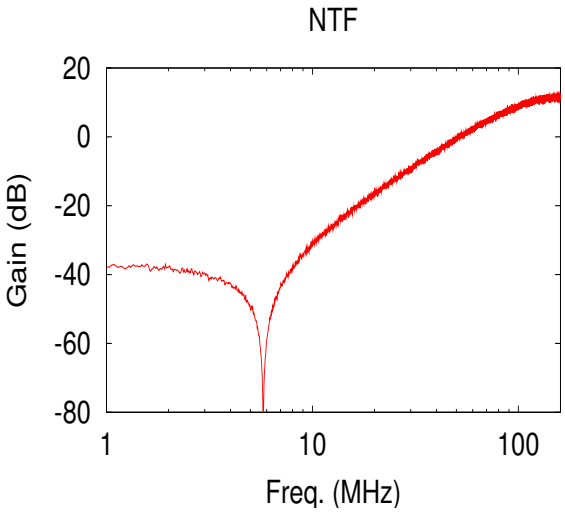
– 3–bit ADC and DAC

– 60 dB of SNR

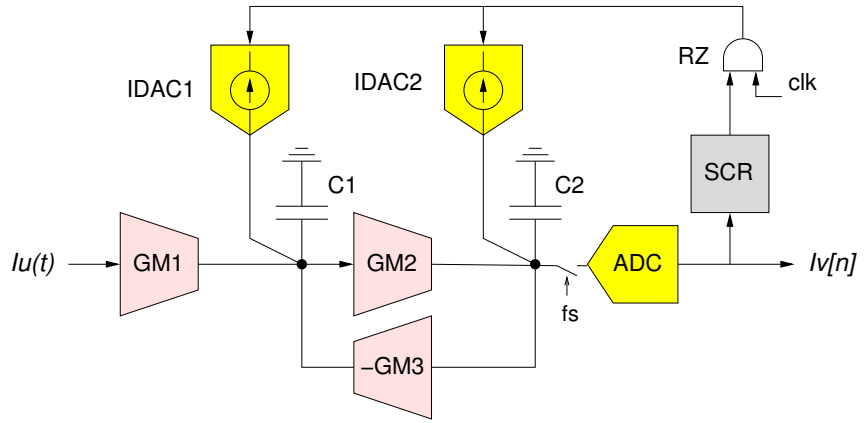
– RZ DAC: less sensitive to:

ADC metastability

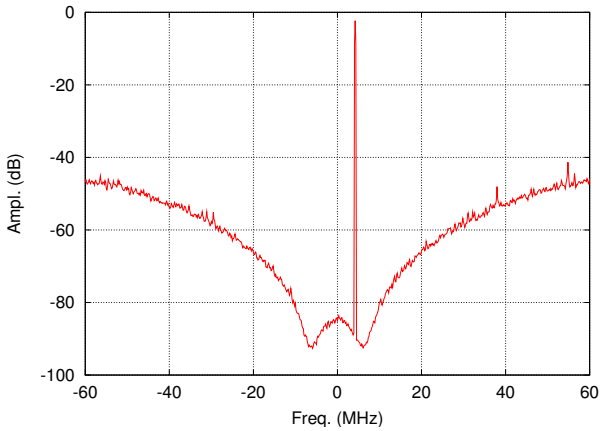
Logic delays

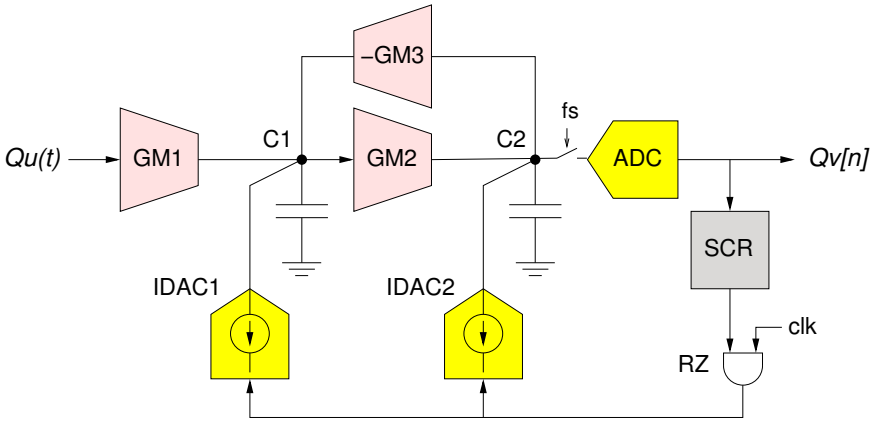


Complex ΔΣ modulator schematic

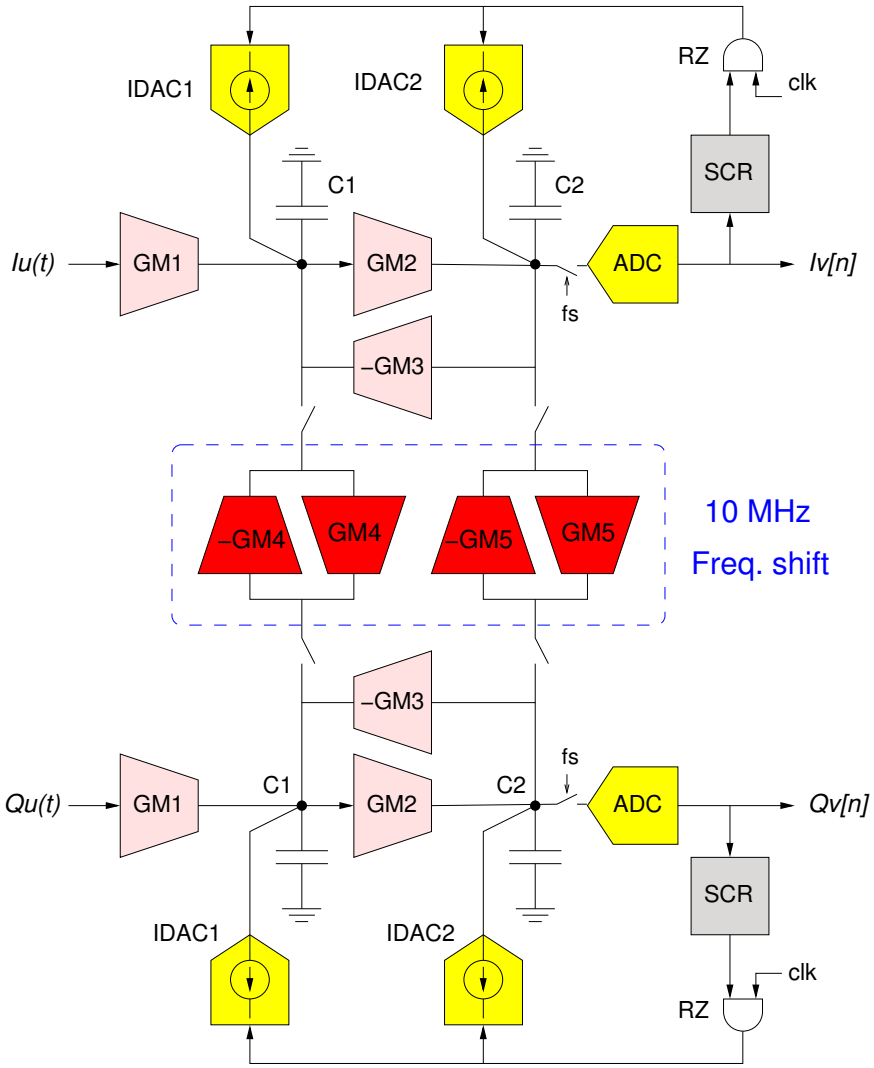


Zero–IF mode

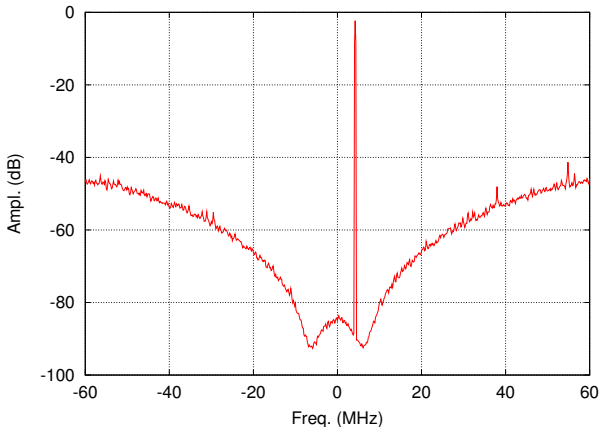




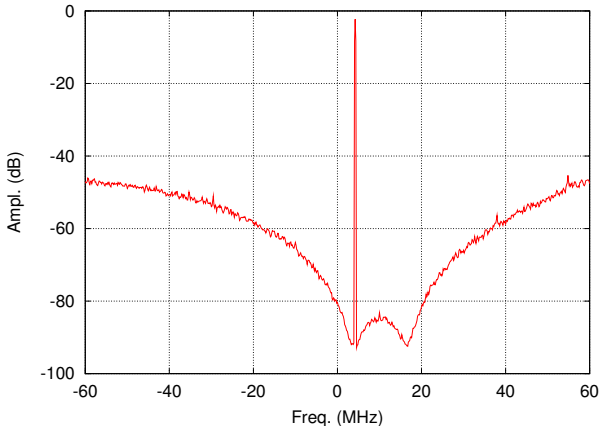
Complex ΔΣ modulator schematic



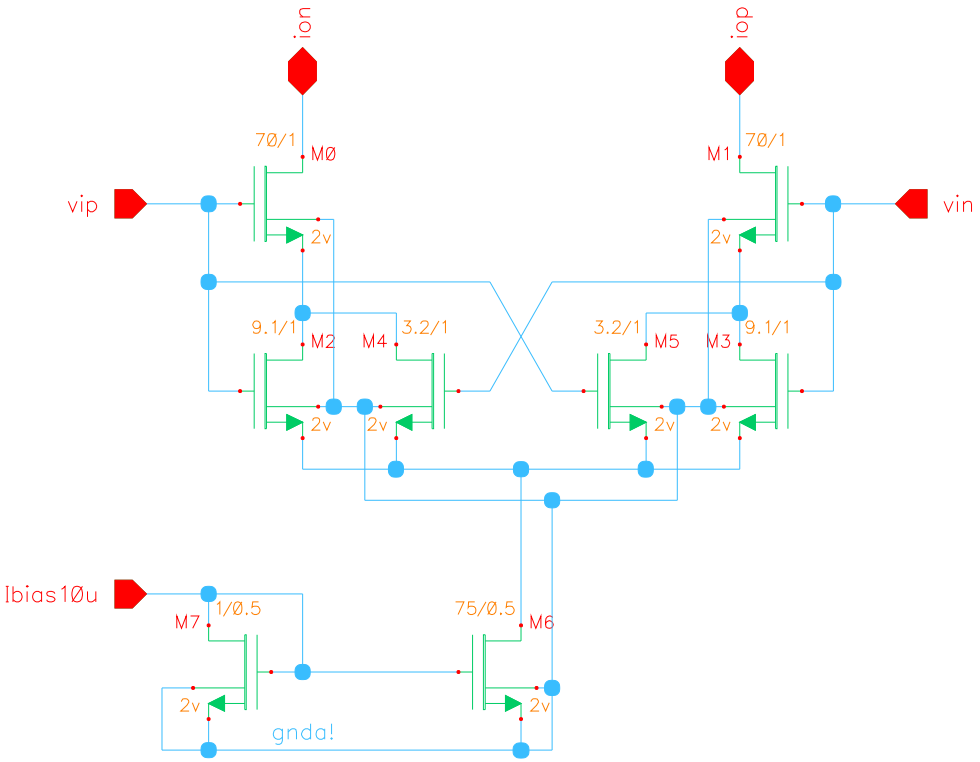
Zero–IF mode

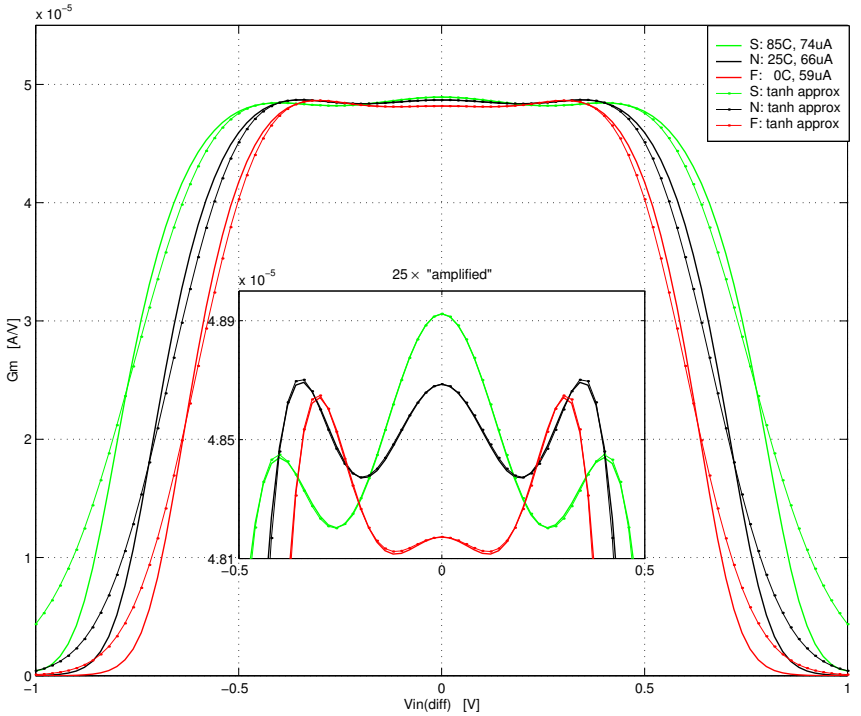


Low–IF mode



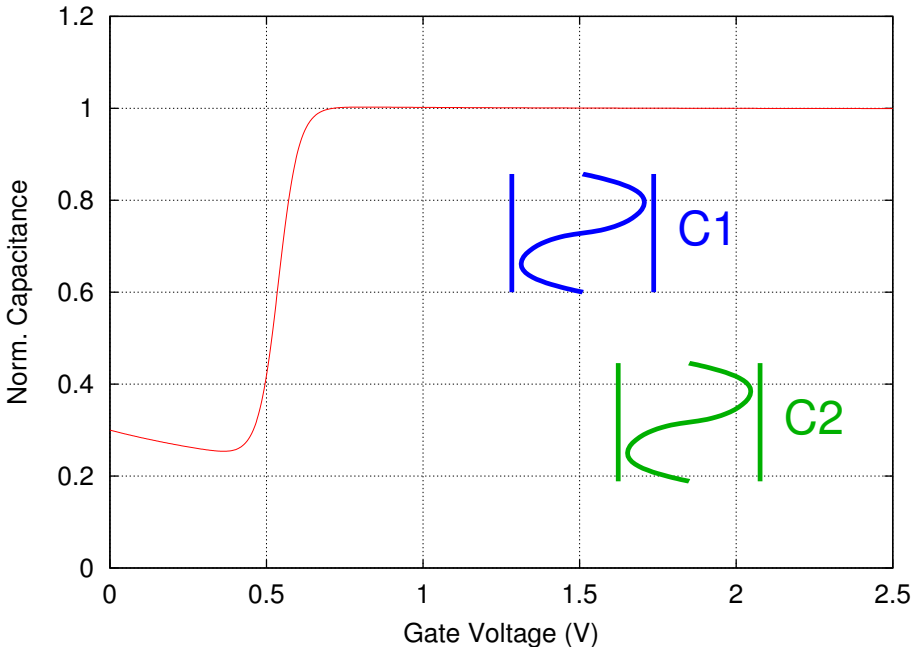
Circuit blocks: Transconductors

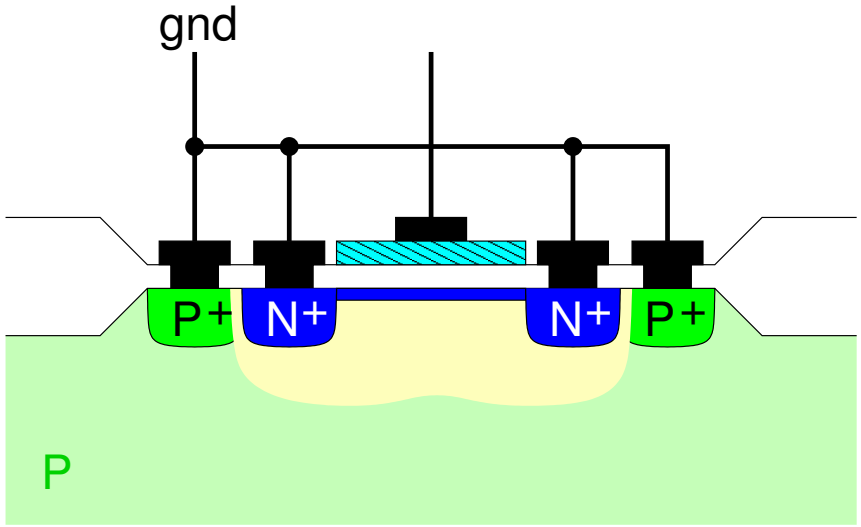




$$G_m(x) = G_m(0)\frac{\partial}{\partial x}\left\{\tanh\left(x + \frac{0.82}{3}x^3 + \frac{2.14}{5}x^5 - \frac{0.60}{7}x^7\right)\right\}$$

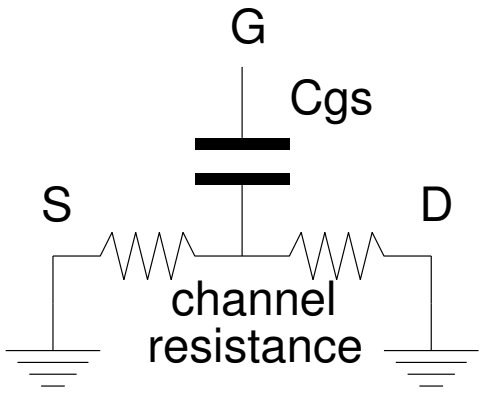
Circuit blocks: Capacitors: Inversion MOSFETs



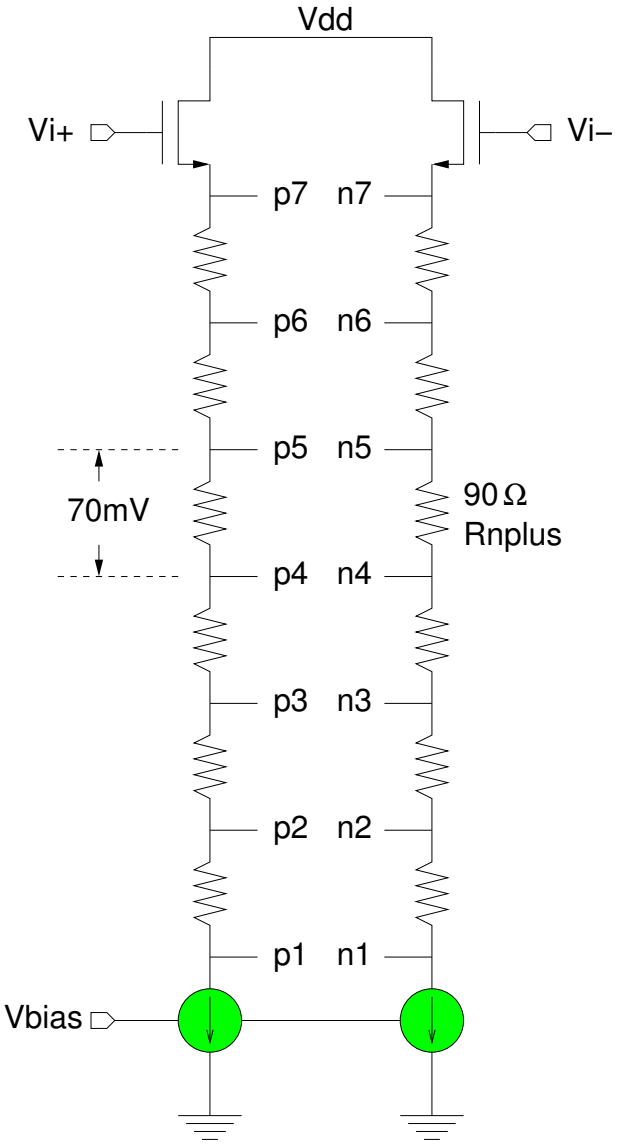


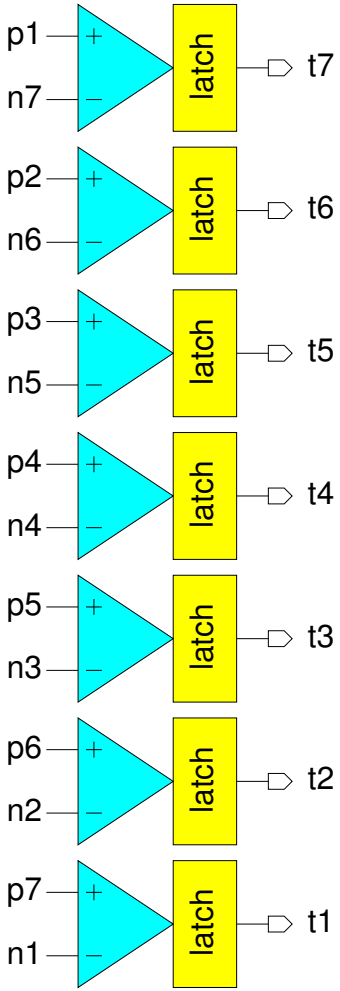
- Smallest chip area
- No technology options required
- Channel resistance can alter the NTF:

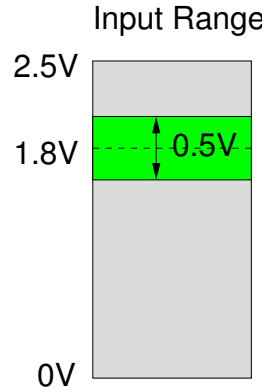
  Big capacitors must be split into parallel, smaller, capacitors to improve their Q



Circuit blocks: flash ADC

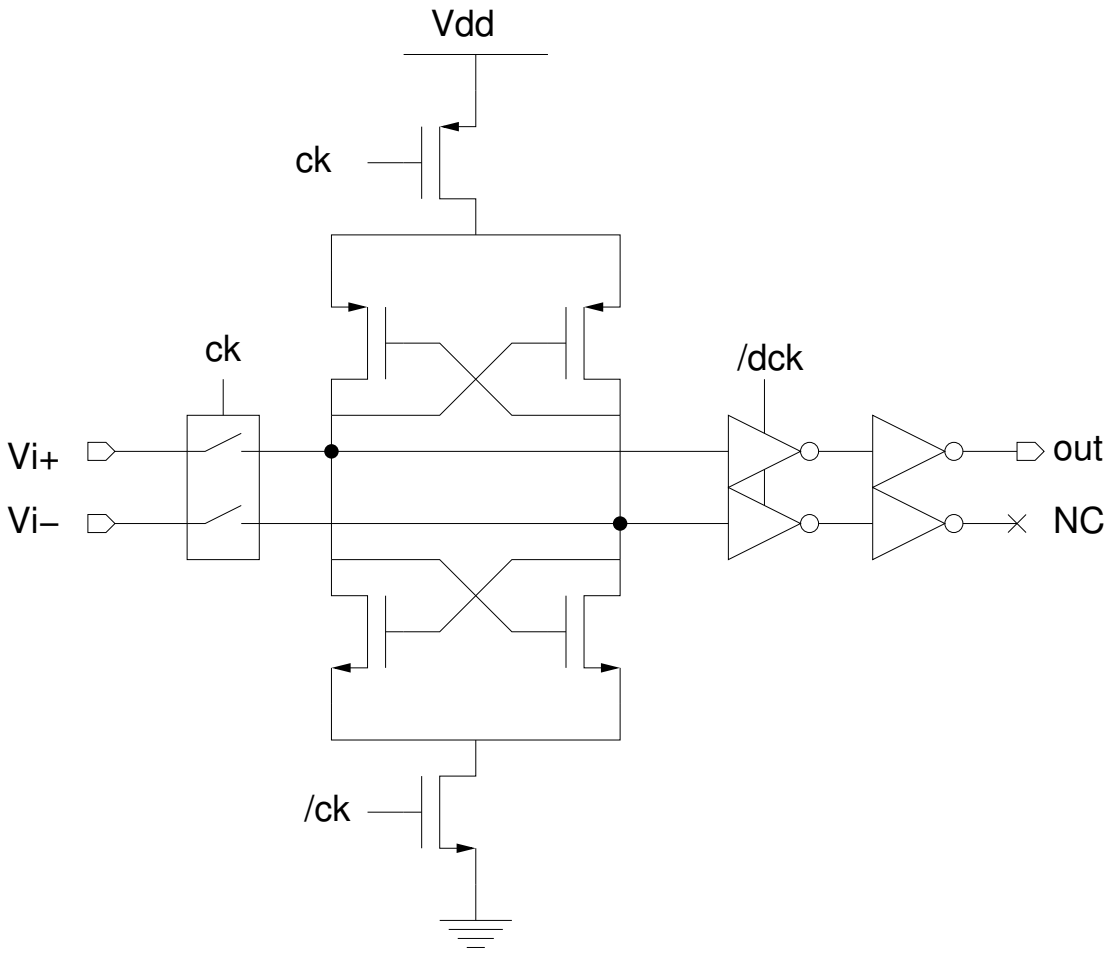




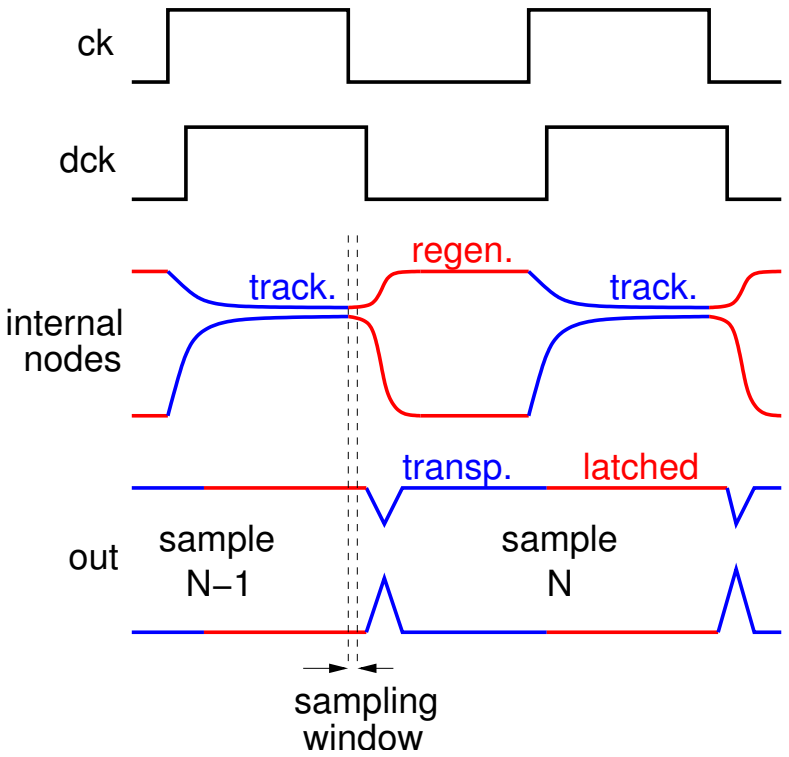


Circuit blocks: ADC's comparators

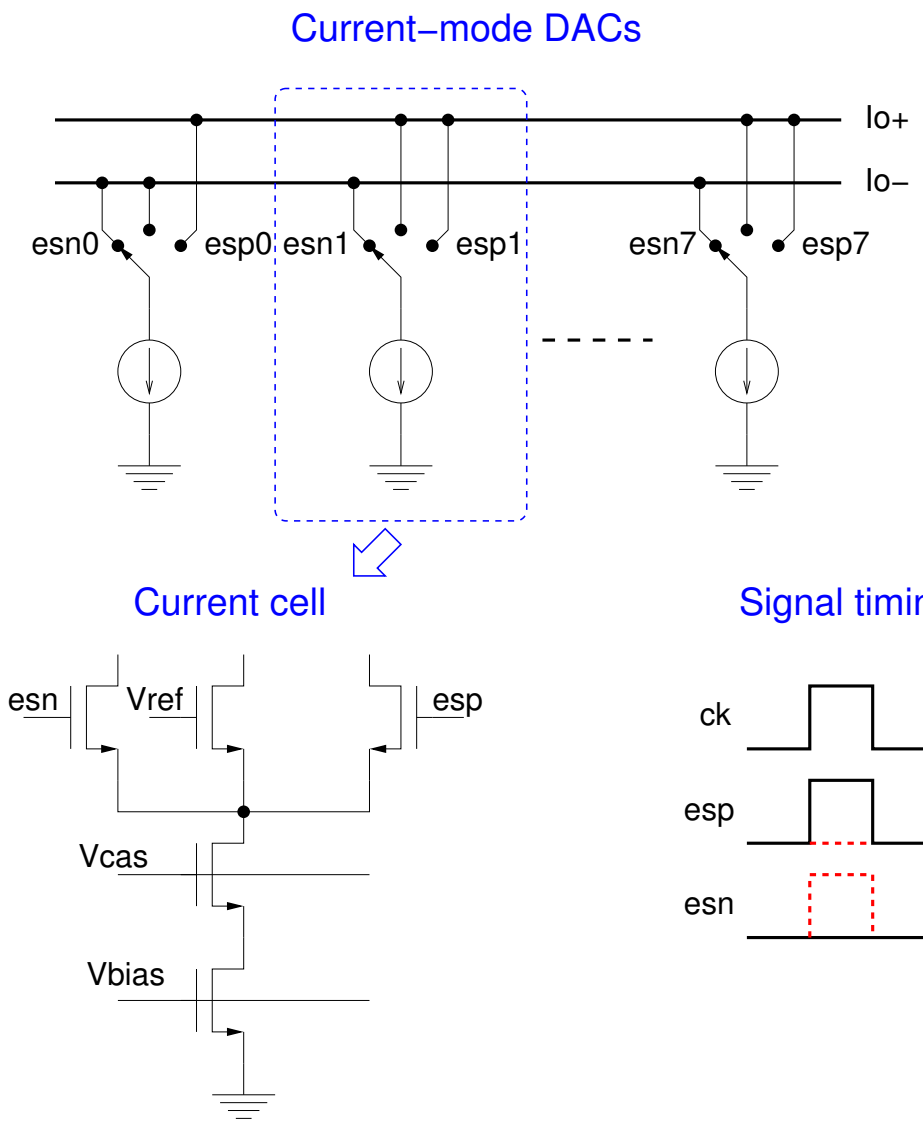
Comparator & Latch



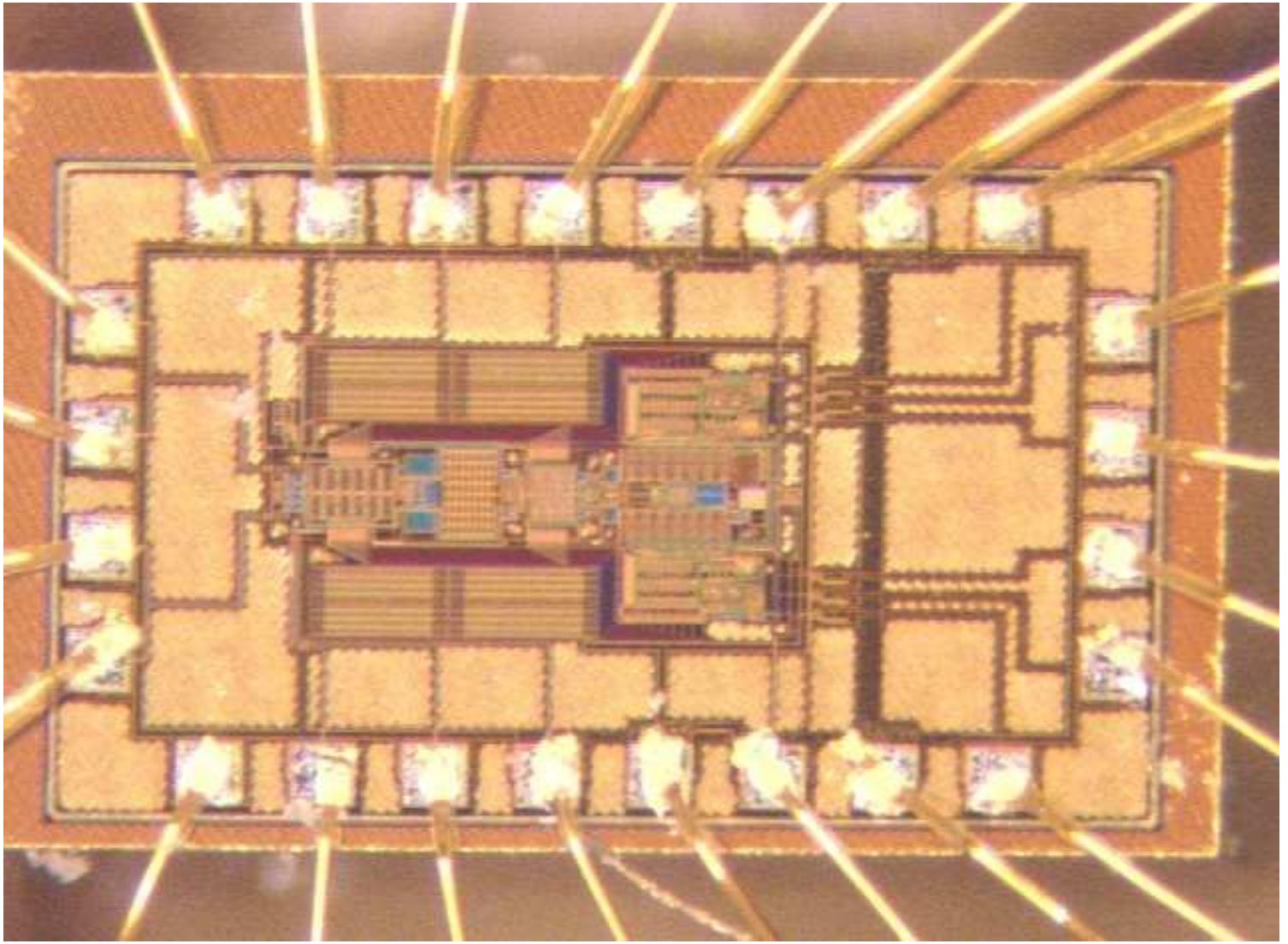
Signal Timing



Circuit blocks: Current-mode DACs

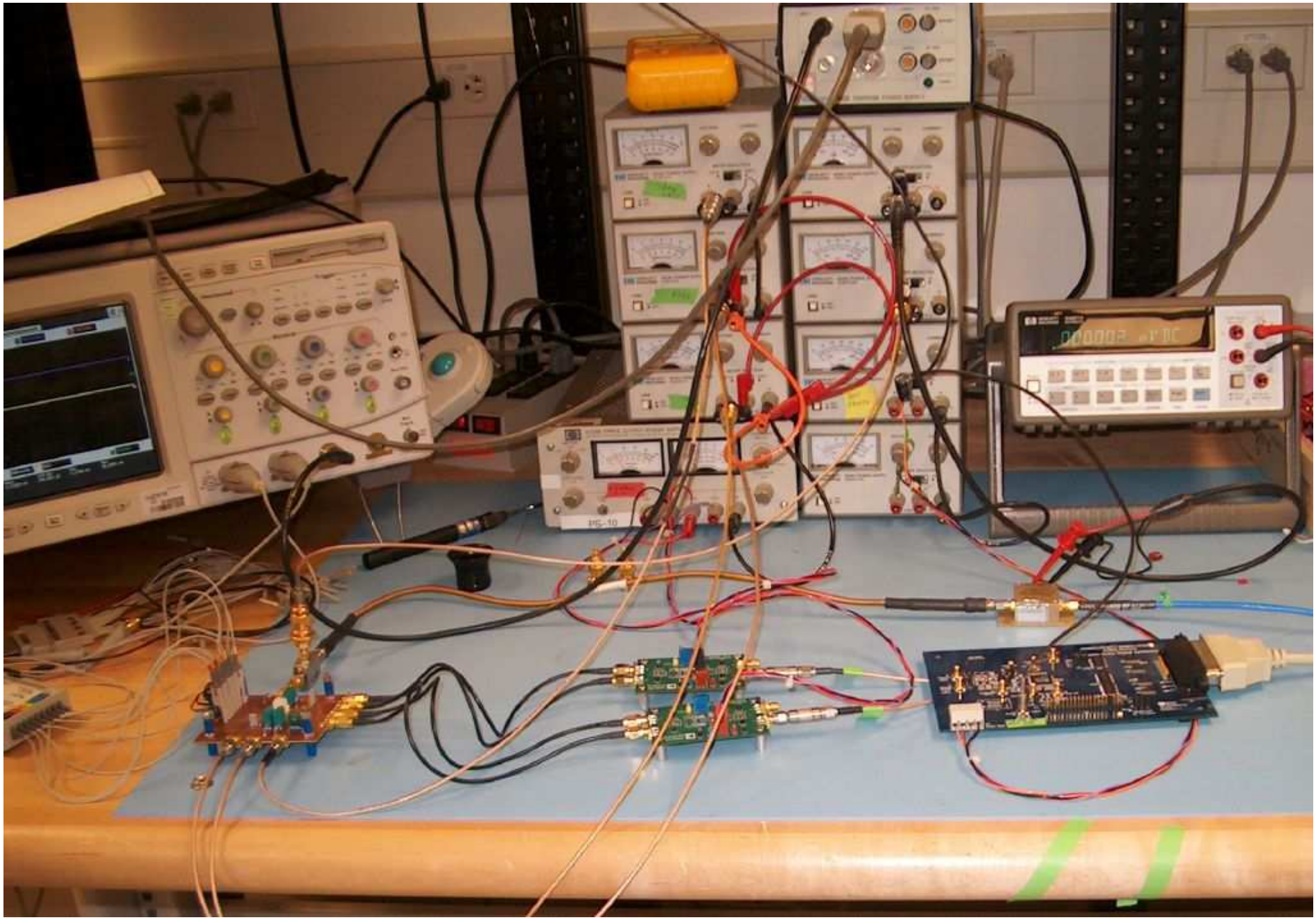


Photograph of the test chip



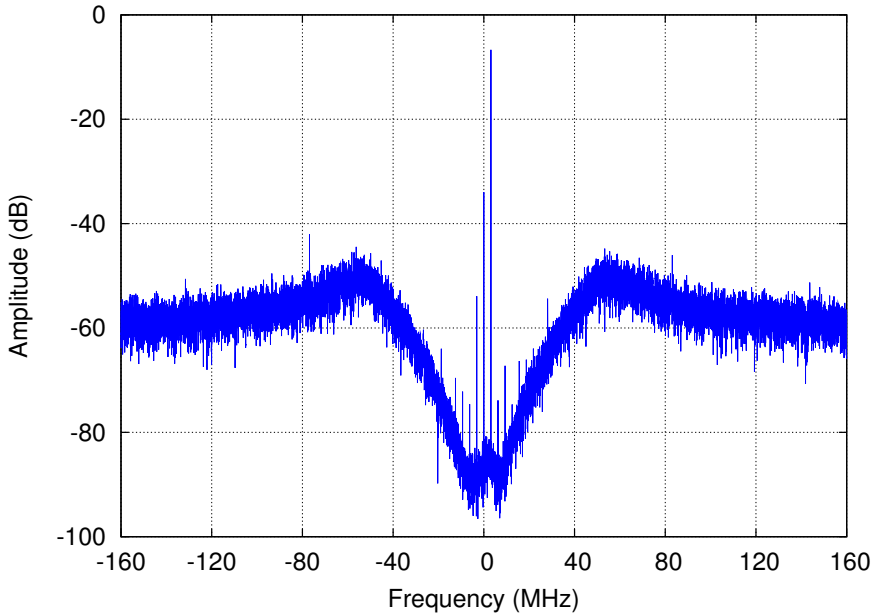
0.25μm CMOS. Area: 0.44 mm^2 without pads. (1.3 mm^2 with pads)

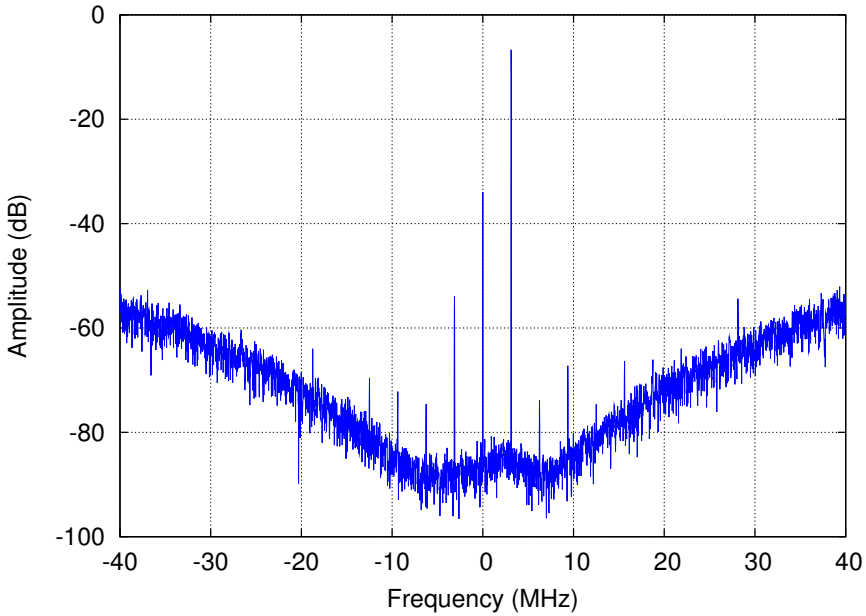
Measurements. Experimental setup



Measurements. Sine Wave.

Zero-IF mode

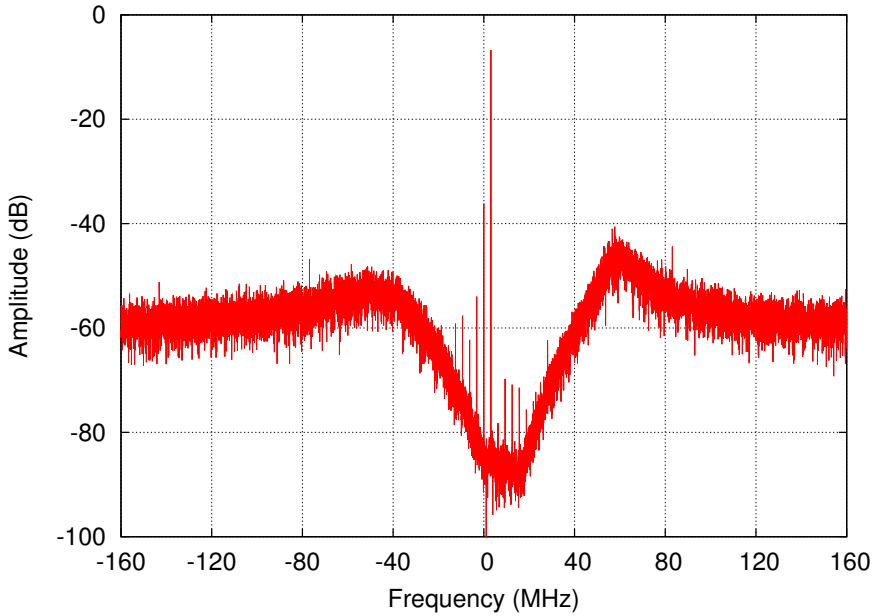


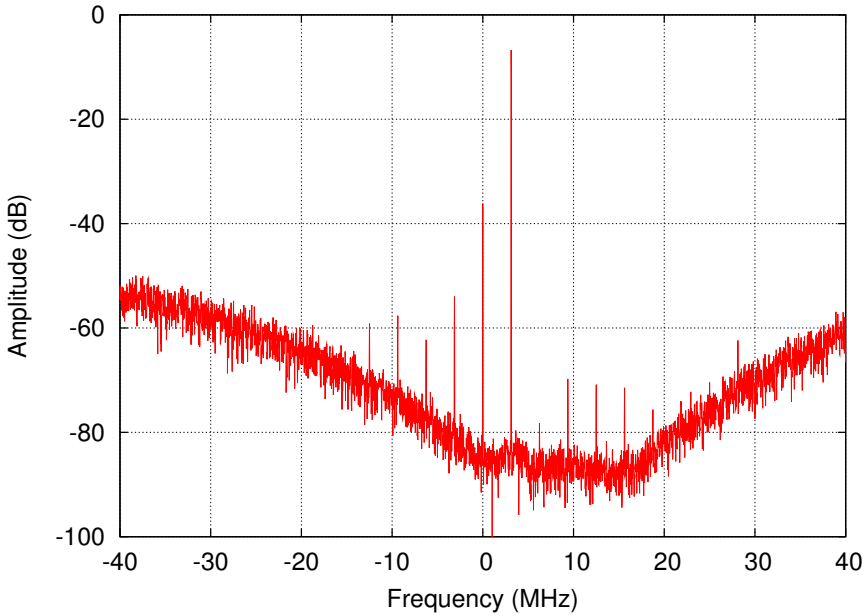


Input Ampl. = -6 dBm	SNR = 51.8 dB	IMR = 47.2 dB
Output Ampl. = -5.6 dB	THD = -58 dB	DC Ampl. = -32.9 dB

Measurements. Sine Wave.

Low-IF mode

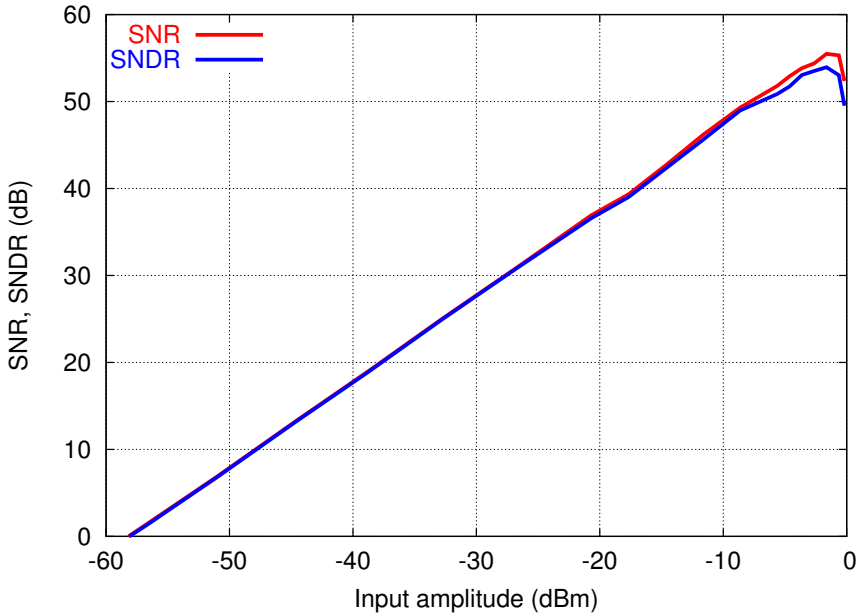




Input Ampl. = -6 dBm	SNR = 51.1 dB	IMR = 47.2 dB
Output Ampl. = -5.67 dB	THD = -58.3 dB	DC Ampl. = -35.1 dB

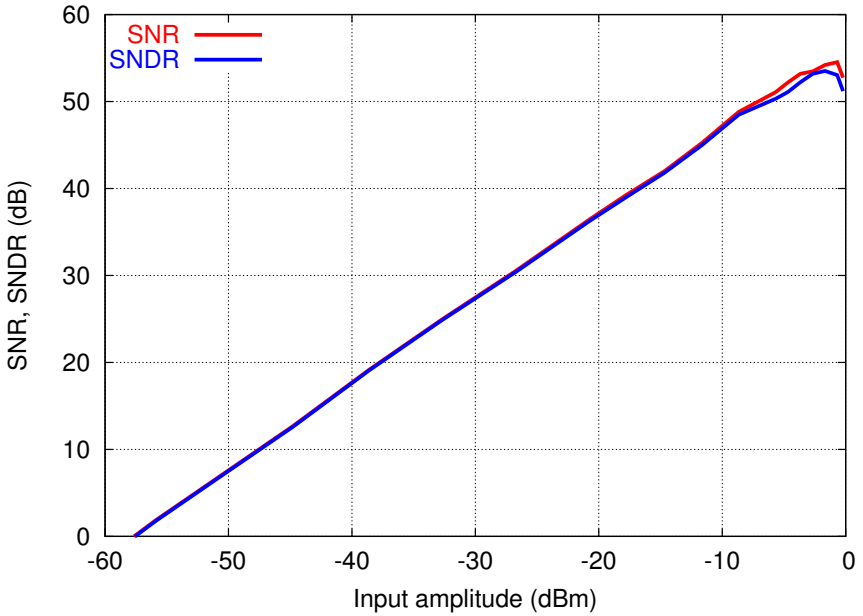
Measurements. SNR and SNDR

Zero-IF mode



max SNR = 55.5 dB
max SNDR = 53.9 dB

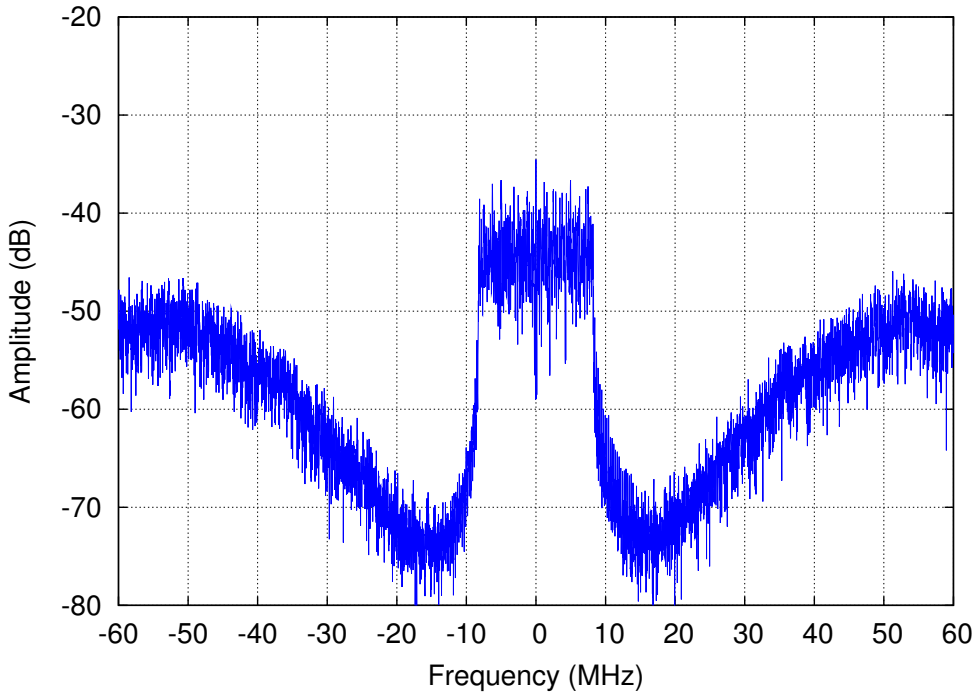
Low-IF mode

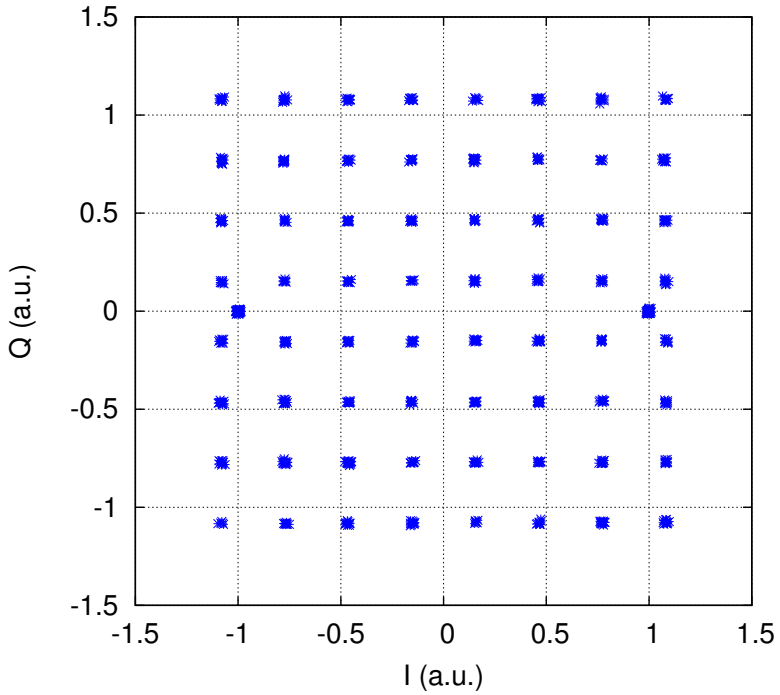


max SNR = 54.5 dB
max SNDR = 53.5 dB

Measurements. OFDM.

Zero-IF mode



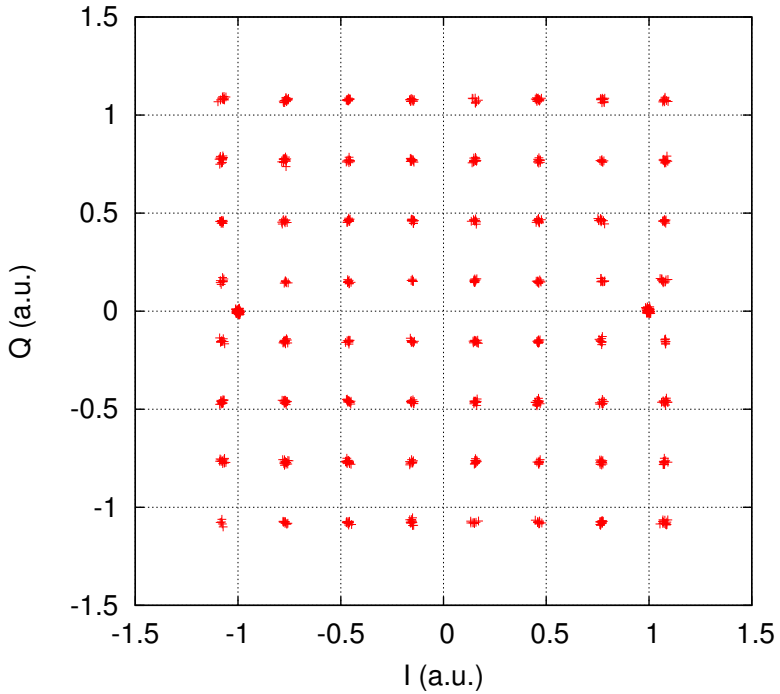


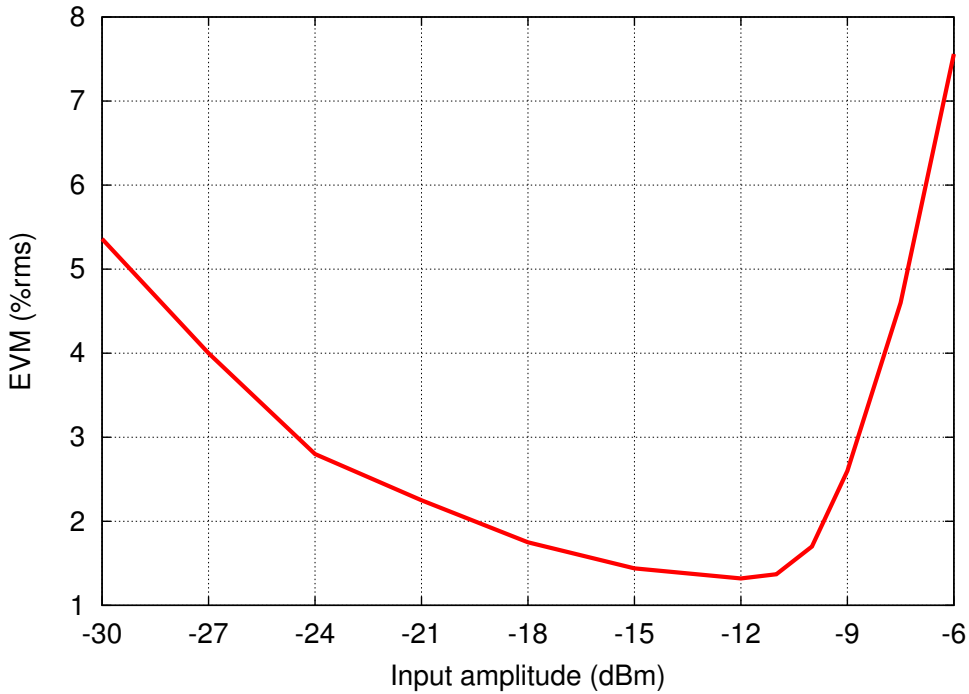
Input Amplitude = -12 dBm	EVM = 0.95 % rms

Measurement. OFDM.

Low-IF mode

(single OFDM input modulated at 10 MHz)





Summary

⇨ A dual-mode, complex $\Delta\Sigma$ modulator for wireless-LANs is demostrated.

⇨ This ADC greatly relaxes the prefiltering specs.

Key parameters

Signal Bandwidth	20 MHz
SNDR	54 dB
ENOB	8.7 bits
Image Rejection	47 dB
Power	32 mW
Technology	0.25μm CMOS

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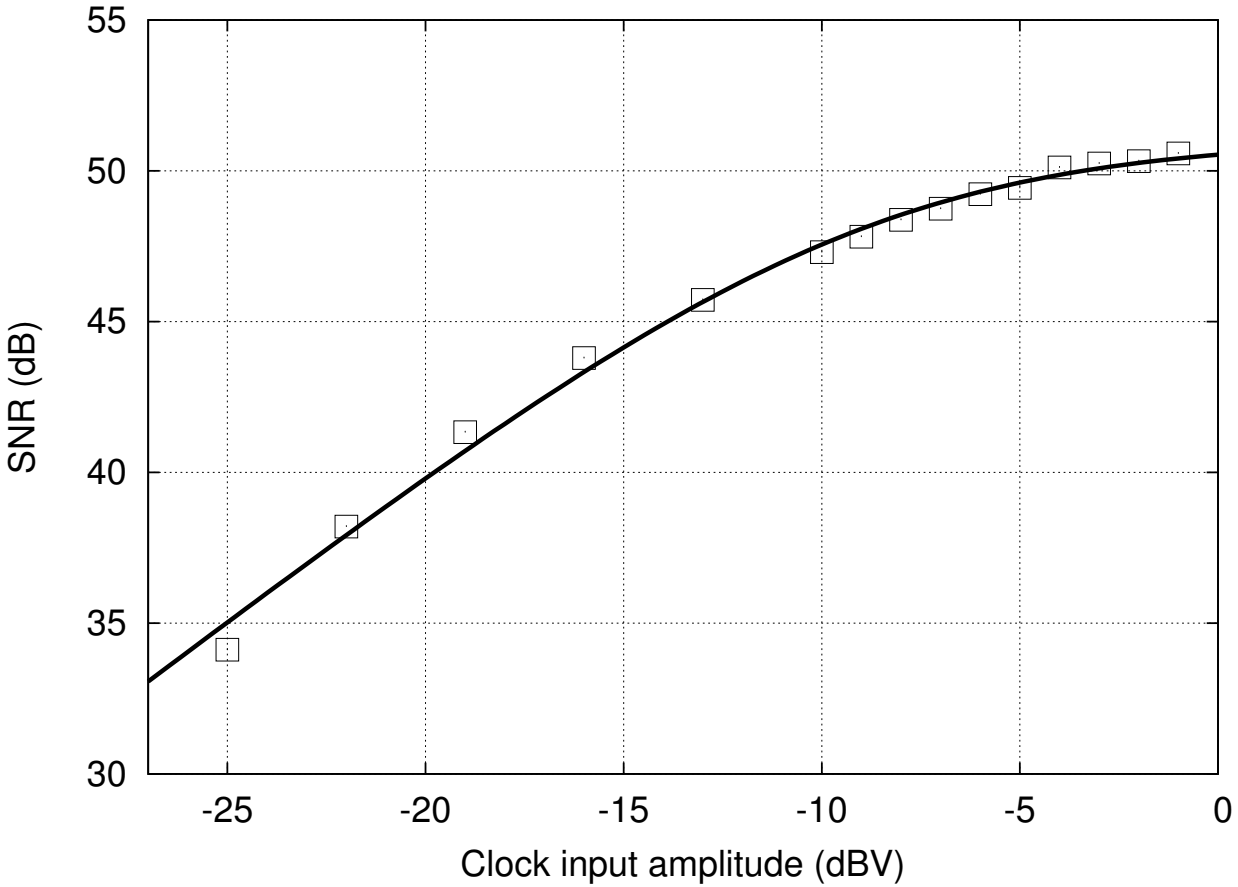
THANKS

Sensitivity to clock jitter

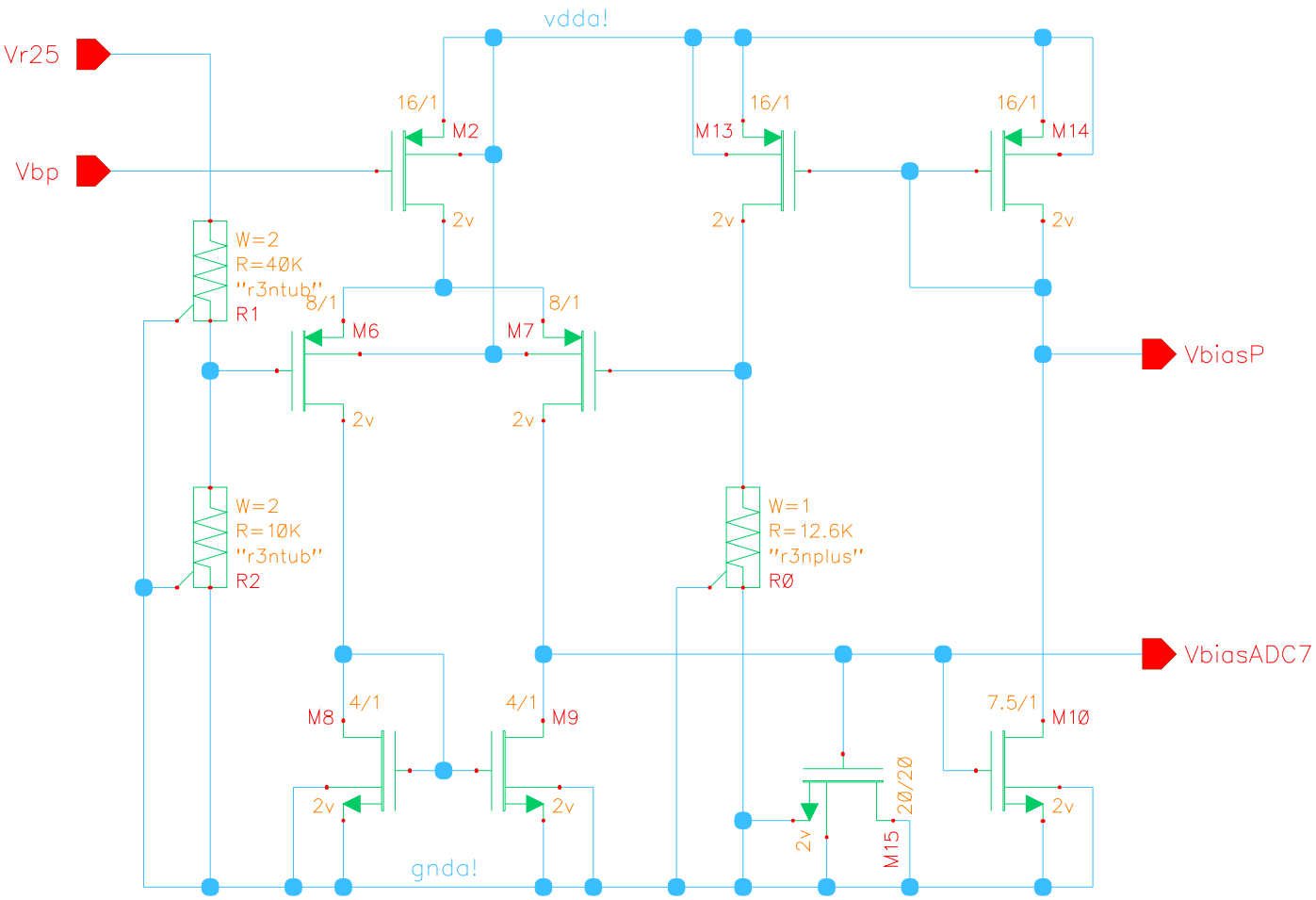
- Clock input: sine-wave with variable amplitude



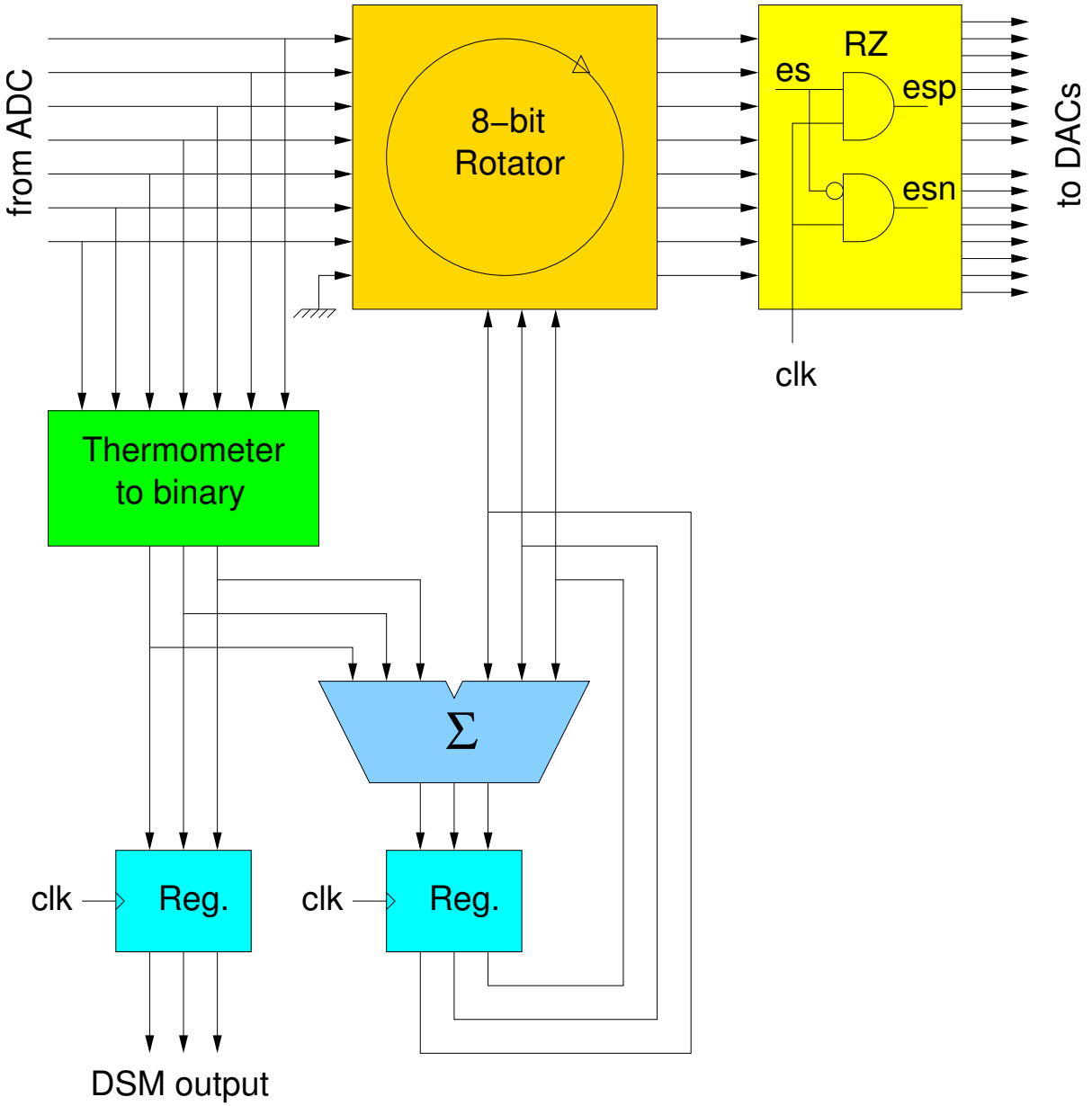
$$SNR\,(dB) = -10 \cdot \log_{10}\left[2\left(\frac{\sigma_v^2}{4\pi^2 A^2} + N^2\right)\right] \; ; \sigma_{jitter} = \frac{T\sigma_v}{2\pi A}$$

$$\sigma_v \simeq 6mV \; ; \sigma_{jitter} \simeq 0.75ps$$

Biasing circuit for ADC



DWA scrambler



Measurement. OFDM.

Low-IF mode

(single OFDM input modulated at 10 MHz)