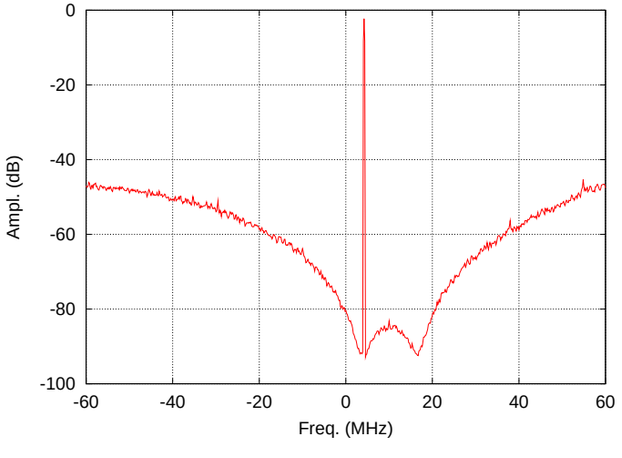
agere systems

Continuous-time, multibit, complex $\Delta\Sigma$ ADC

320 Ms/s, 16x oversampling, 3-bit quantizer, 10-bit ENOB.

J. Arias, P. Kiss, V. Prodanov



Motivation

⇨ Why complex $\Delta\Sigma$:

- ✔ Channel selection and image rejection are done in the digital domain by the decimation filter.
- ✔ Easy analog filtering. (good IQ imbalance, low power)

⇨ Why continuous-time (CT):

- ✔ Capable of operation at high sampling frequencies.
- ✔ Low power consumption.
- ✔ Implicit anti-aliasing property.

⇨ Why multibit:

- ✔ Good SNR for low oversampling ratios. (16)
- ✔ Good stability.

Drawbacks

⇨ $\Delta\Sigma$ ADCs:

- × $\Delta\Sigma$ ADCs requires high sampling rates (oversampling $\geq$ 16, typical)
- × A digital filter/decimator is needed (several Kgates).
- × $\Delta\Sigma$ ADCs consume more power than Nyquist-rate ADCs. (But the total power bill can be lower)

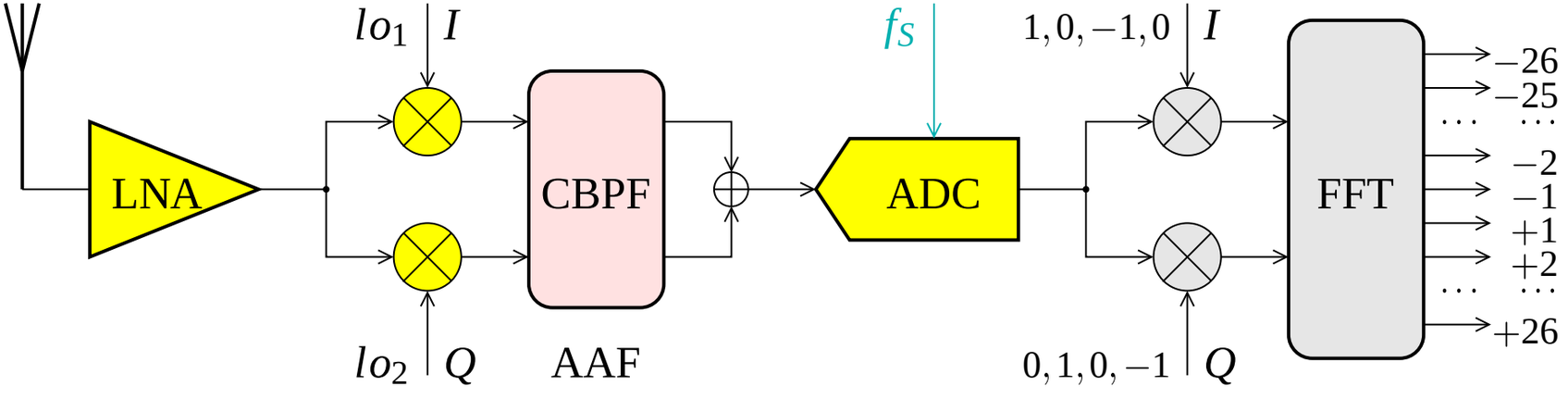
⇨ CT $\Delta\Sigma$ modulators:

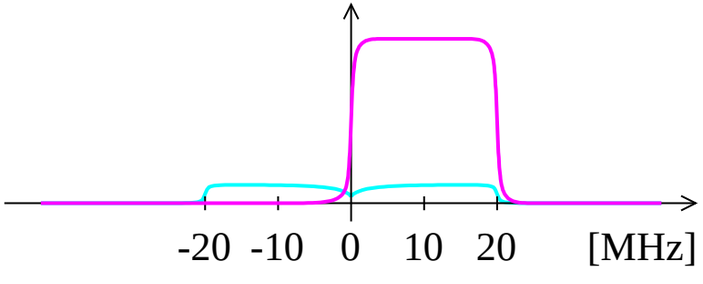
- × Involves DT to CT transformations (NTF) $\Rightarrow$ Tedious mathematics & controllability issues.
- × CT modulators are more sensitive to clock jitter.

⇨ Multibit $\Delta\Sigma$ modulators:

- × Sensitive to DAC nonlinearity. Dynamic element matching (scrambler) needed.

IEEE 802.11a/g, low-IF, receiver with Nyquist-rate ADC



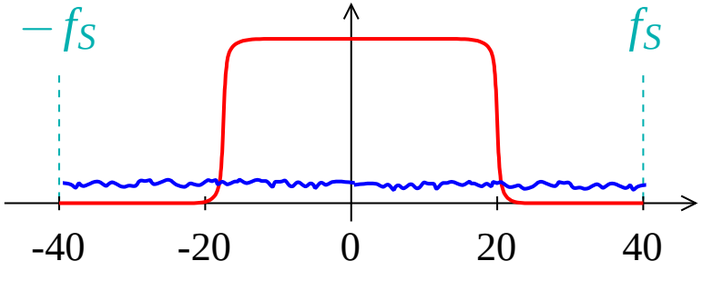


Complex BPF ($1\times$):

$BW = 20$ MHz, $f_{IF} = 10$ MHz

7-pole Chebyshev filter

(Vladimir)



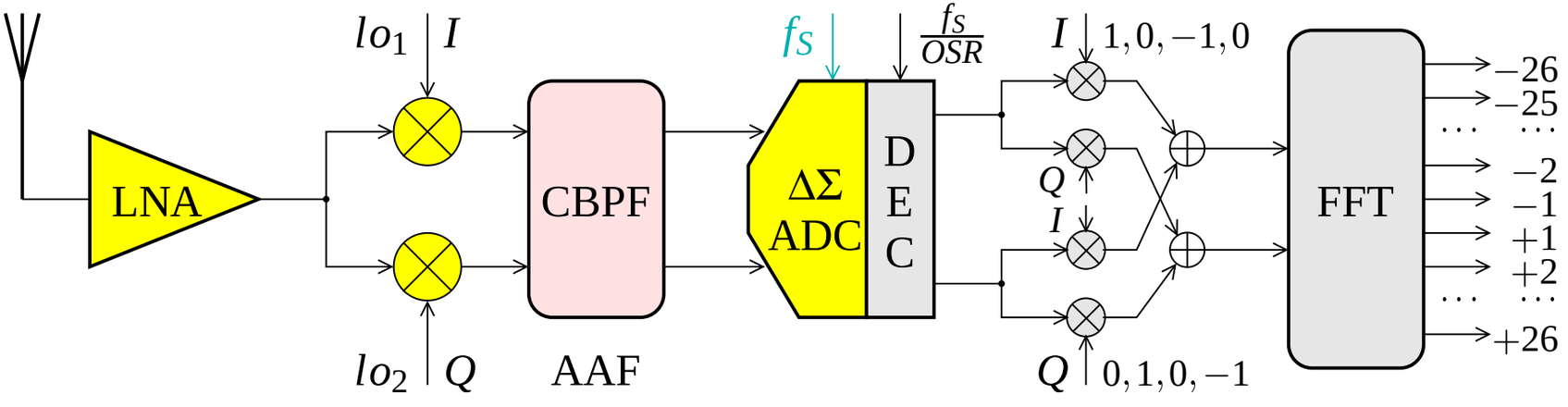
Nyquist ADC ($1\times$):

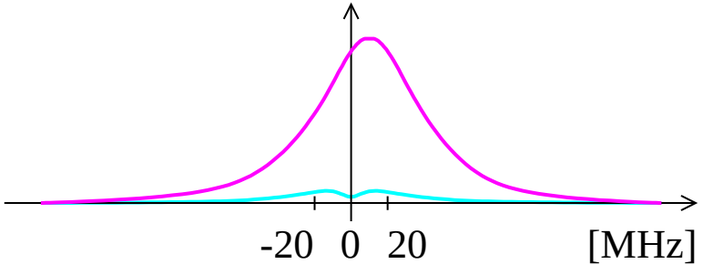
$BW = 20$ MHz, $SNDR = 55$ dB

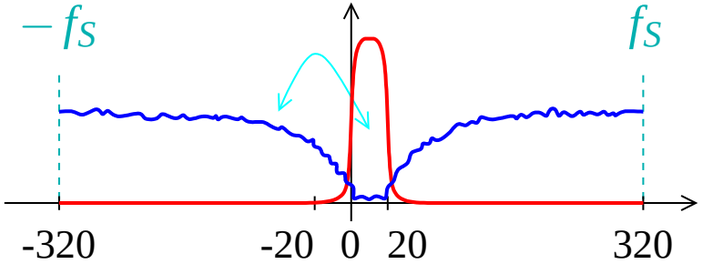
10-bit pipelined ADC

(Jesús)

IEEE 802.11a/g, low-IF, receiver with $\Delta\Sigma$ ADC







Complex BPF:

$BW = 20$ MHz, $f_{IF} = 10$ MHz

3-pole Butterworth filter

Complex CT $\Delta\Sigma$ ADC:

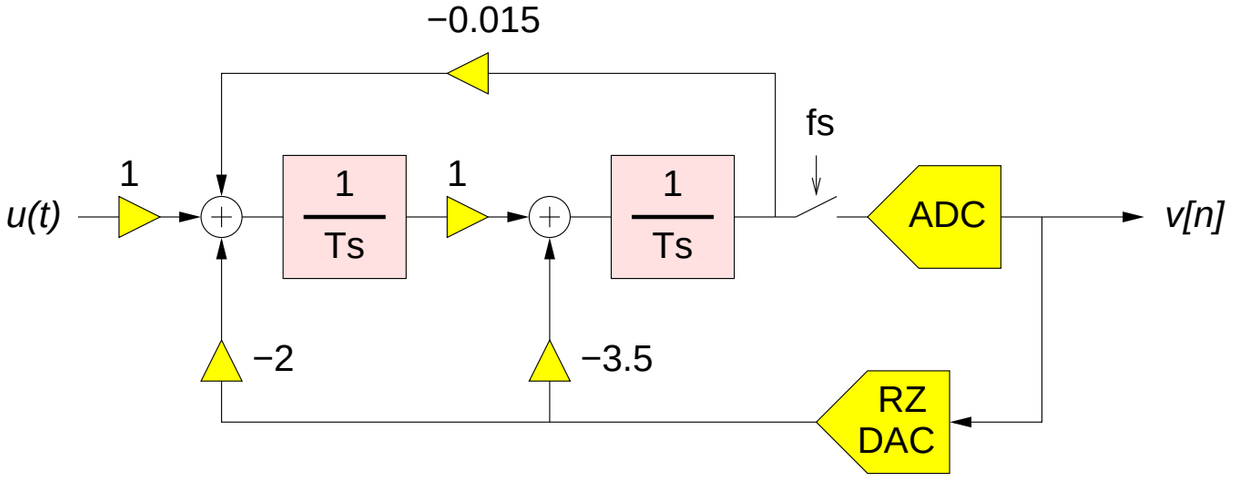
$BW = 20$ MHz, $SNDR = 55$ dB

2nd-order 3-bit 16$\times$ oversampled

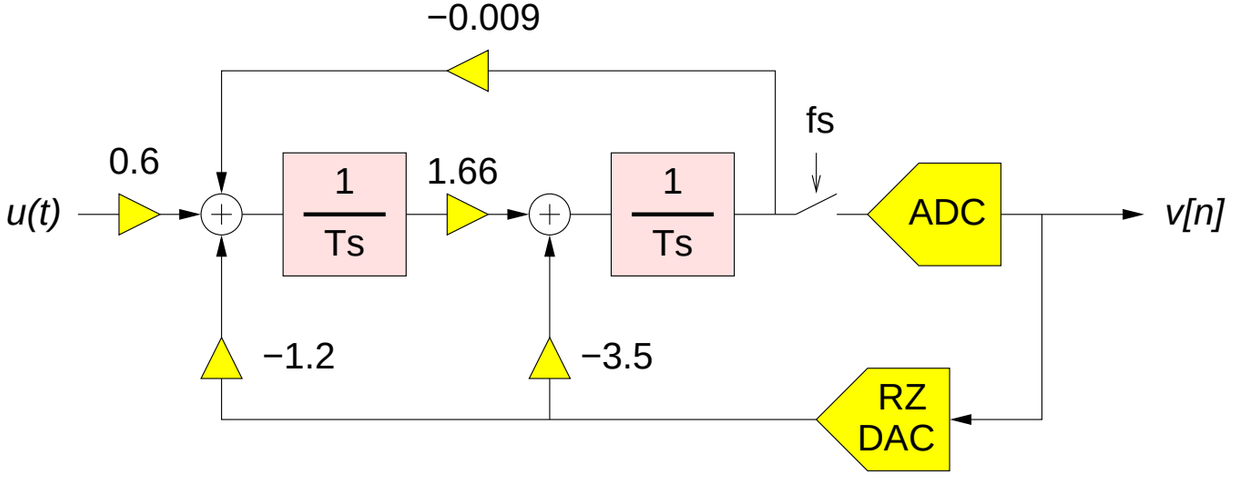
(Vladimir) Proposed architecture *(Peter/Vladimir/Jesús)*

Modulator architecture (Real DSM)

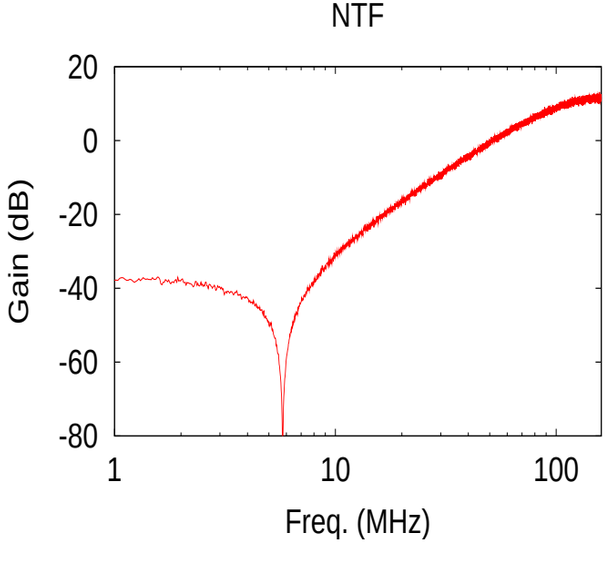
Starting modulator



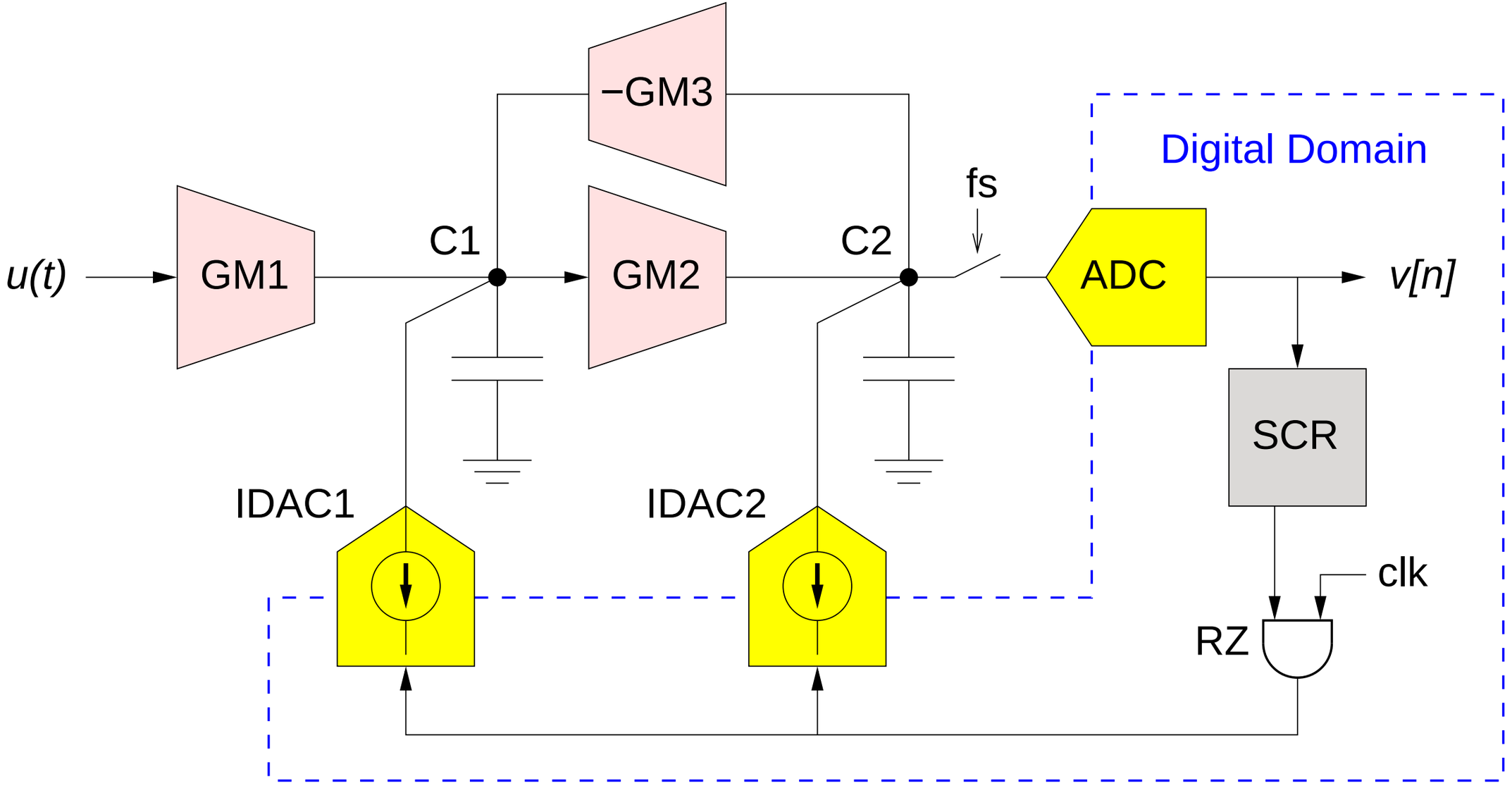
After amplitude equalization



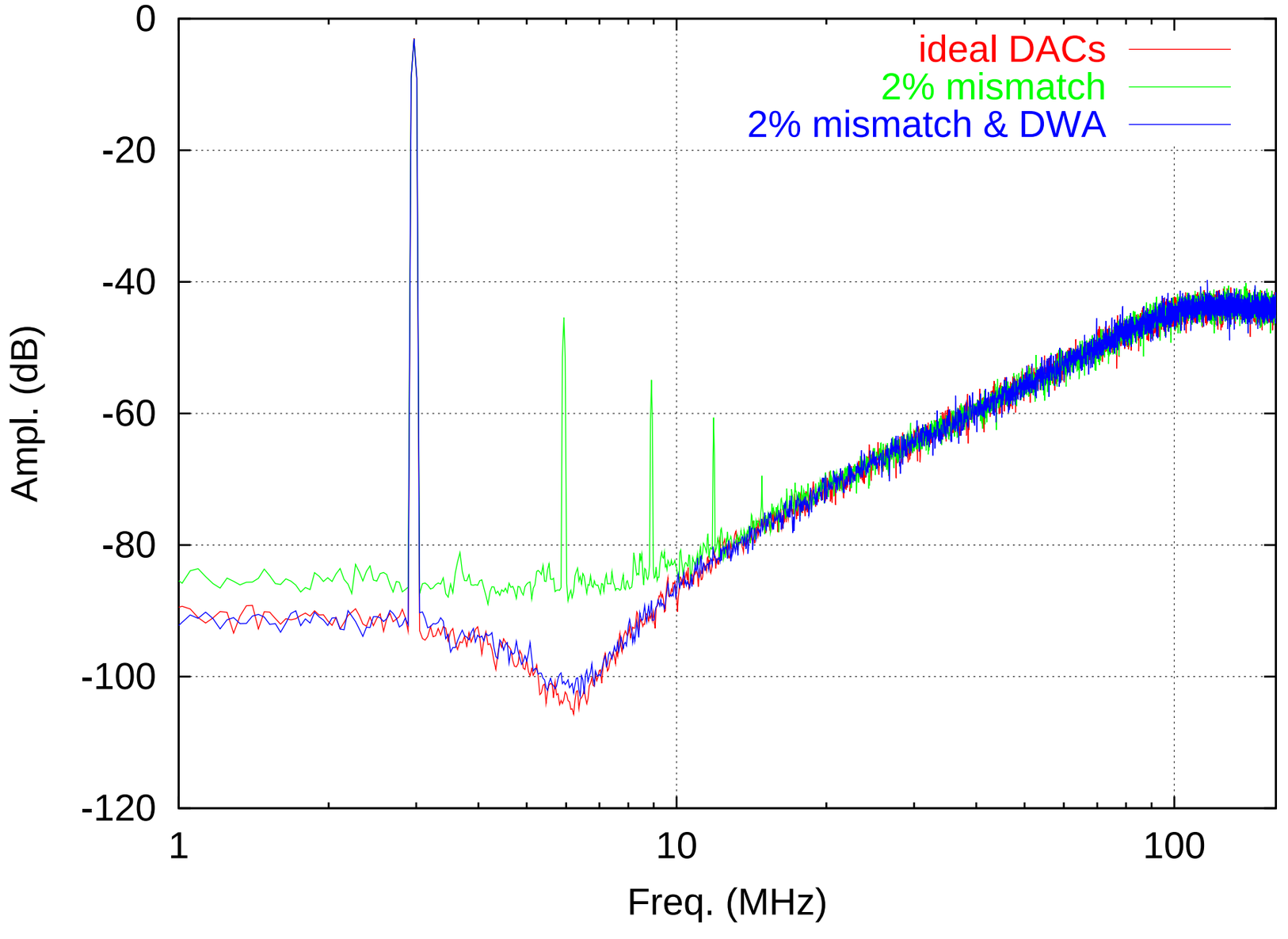
- Second−order NTF
- Optimized zero: +3dB SNR
- 3−bit ADC and DAC
- RZ DAC: less sensitive to:
  - ADC metastability
  - Clock jitter



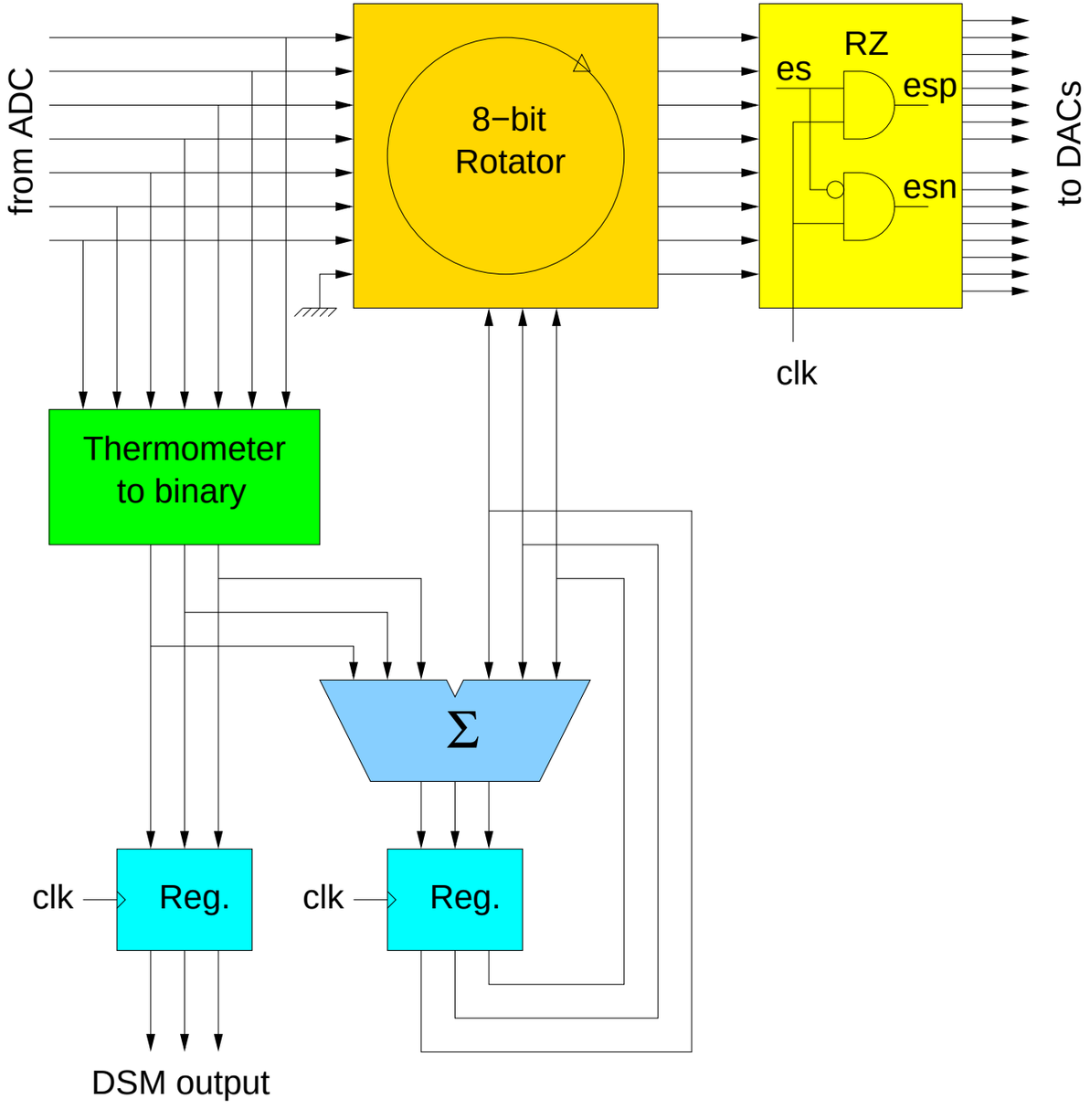
Gm−C Implementation (Real DSM, Single−ended)



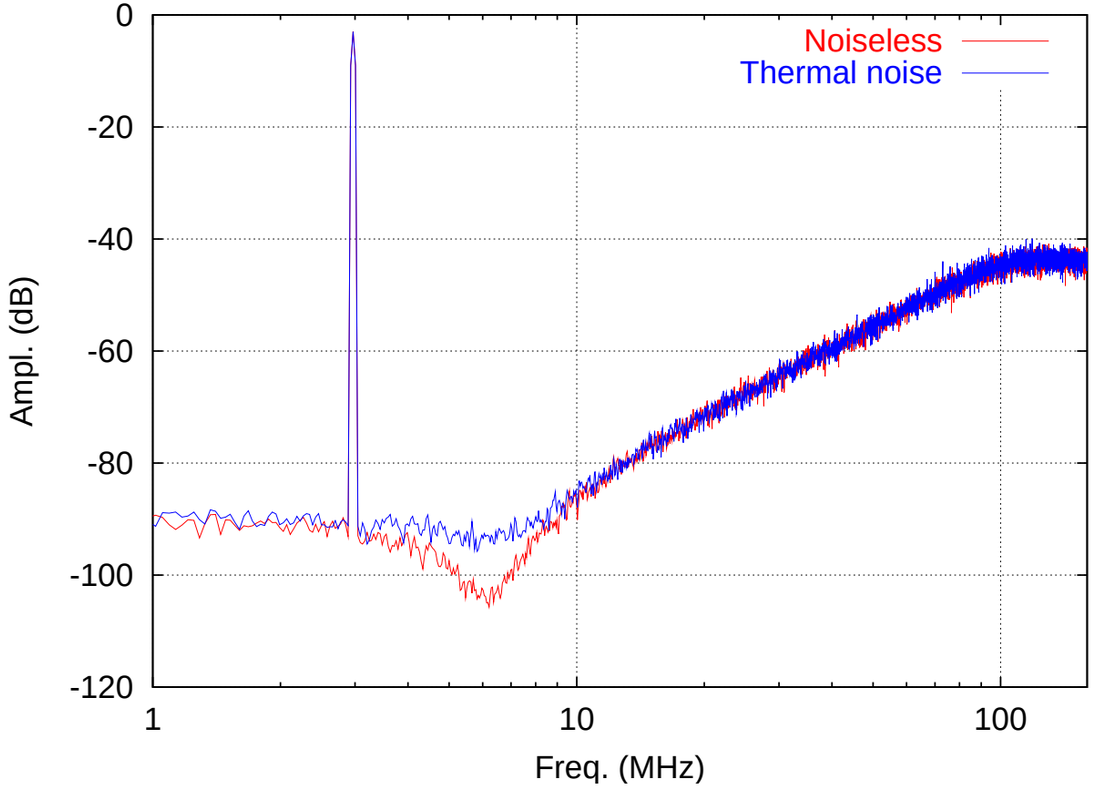
Multibit DACs: Overcoming nonlinearity using dynamic element matching



DWA logic (scrambler)



Thermal noise



Noise simulation parameters:

GM1: 1000 µA/V C1: 5.165 pF

GM2: 200 µA/V C2: 0.376 pF

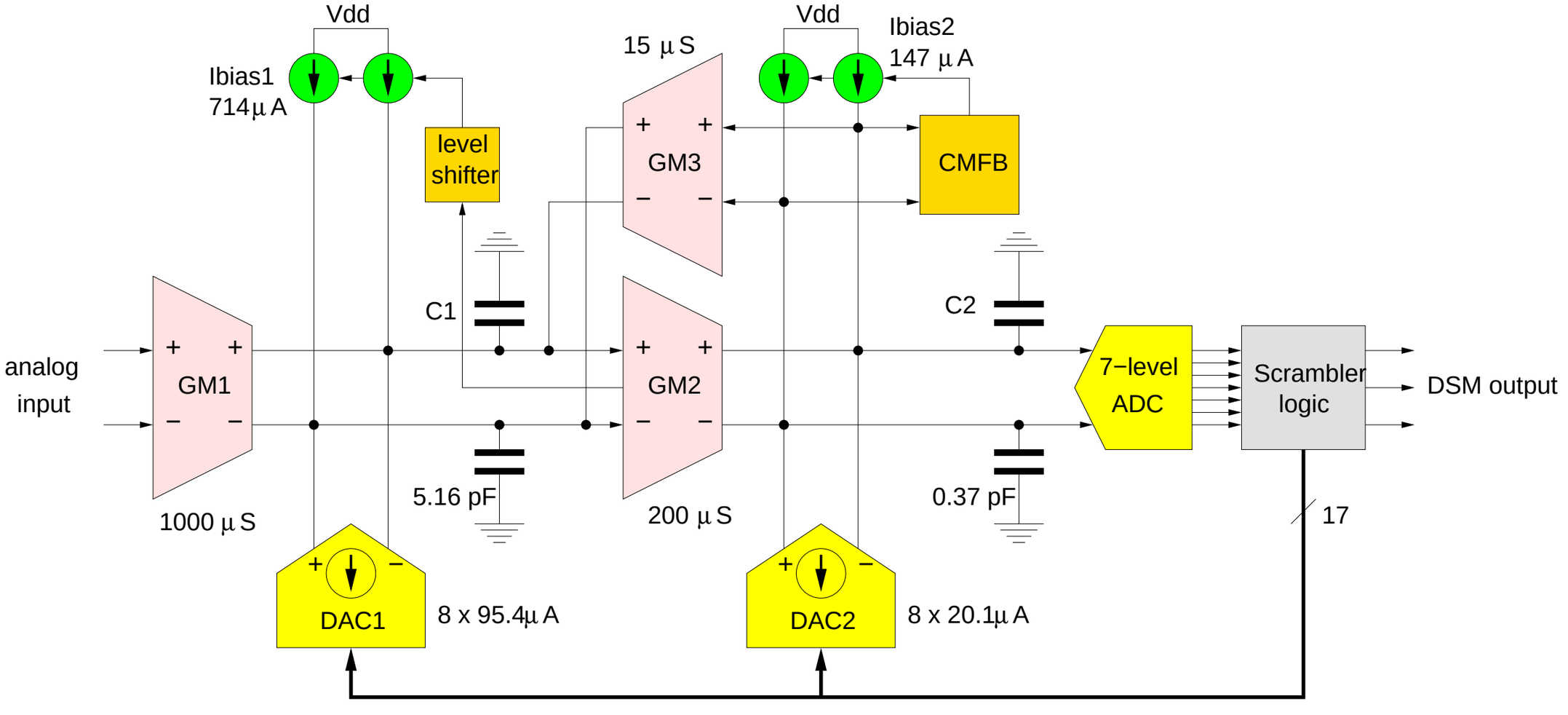
GM3: 15 µA/V

Ib1: 714 µA Idac1: 95.4µA

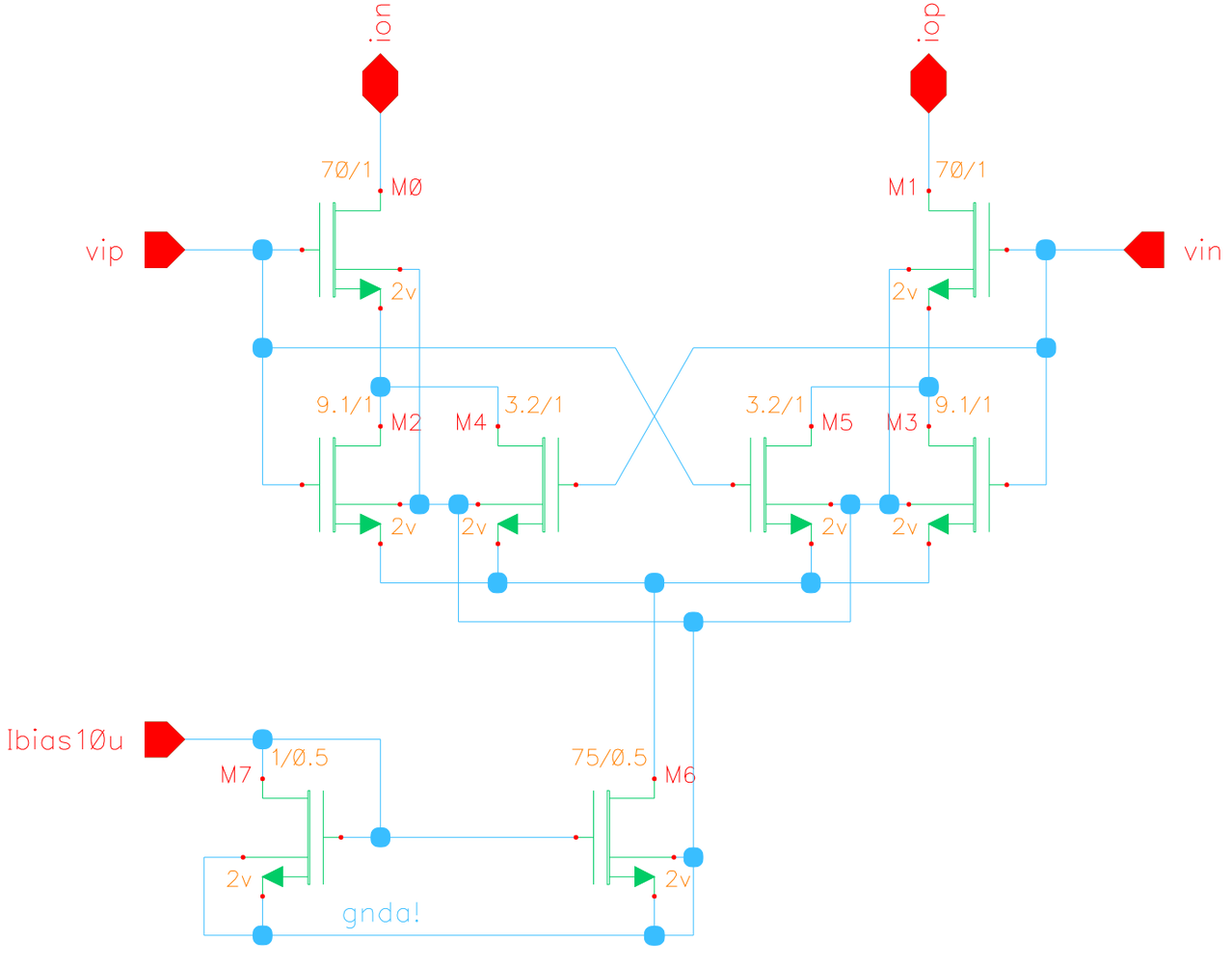
Ib2: 147 µA Idac2: 20.1µA

Performance loss: 2 dB SNR

Real DSM. Detailed schematic

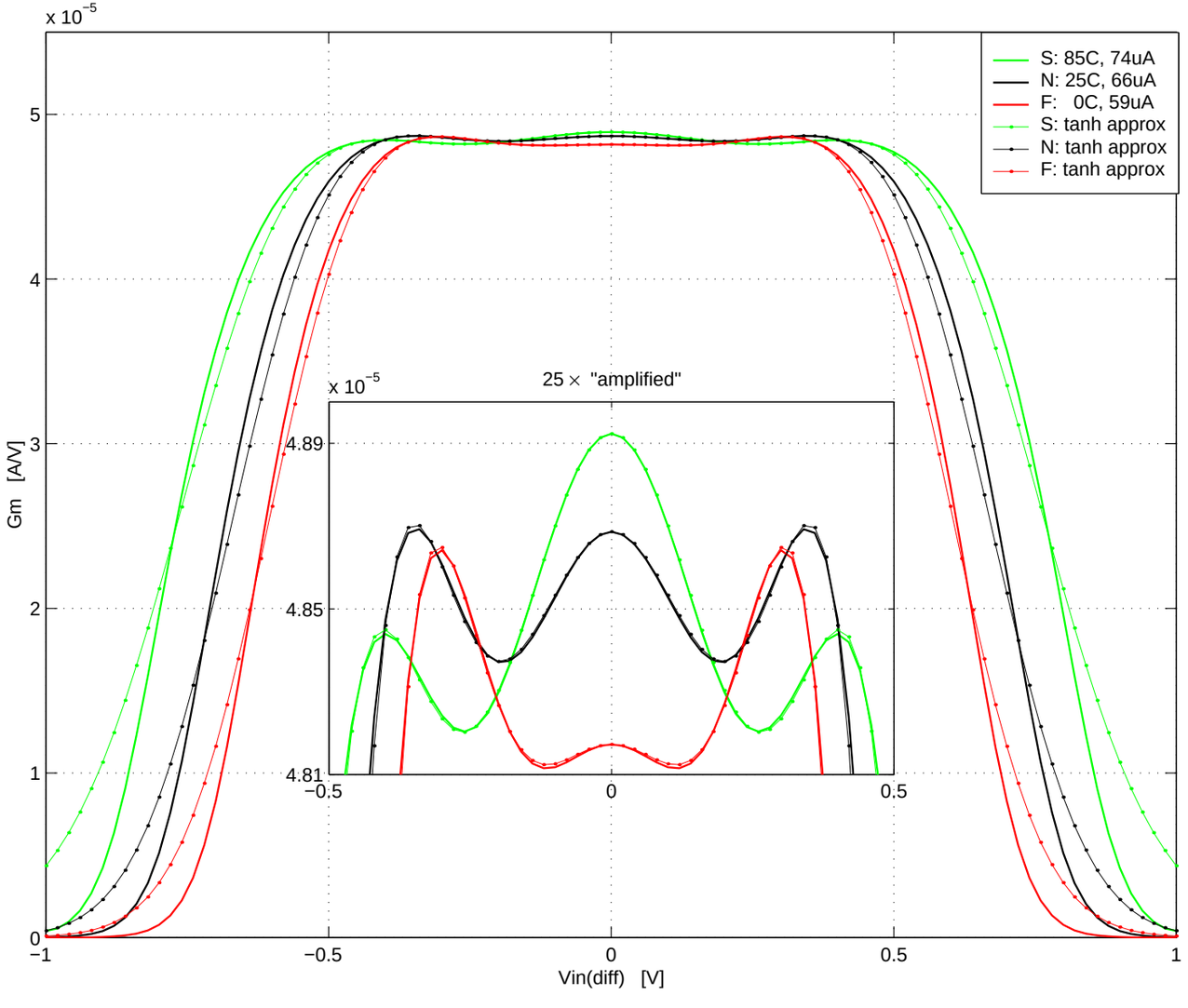


Circuit Elements: Transconductors



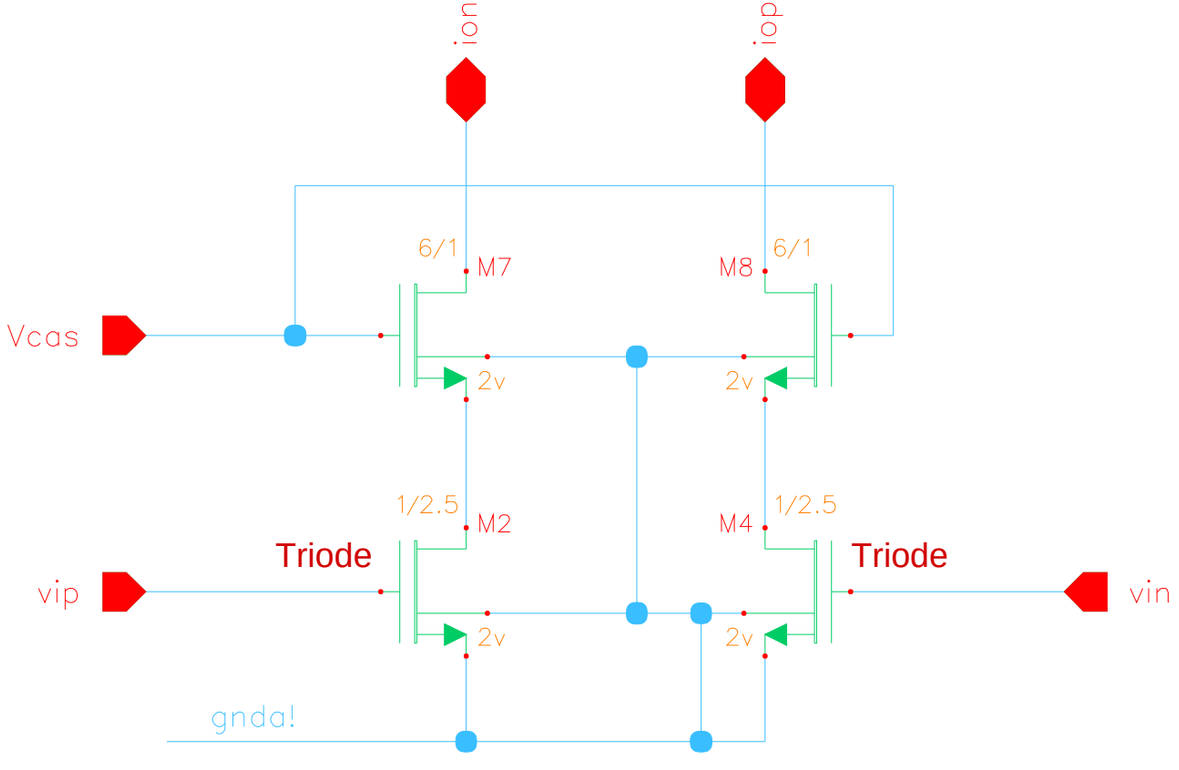
- Large dynamic range
- Unipolar output
- External tuning
- Vladimir's patent (2001)

Circuit Elements: Transconductor's nonlinear G_m



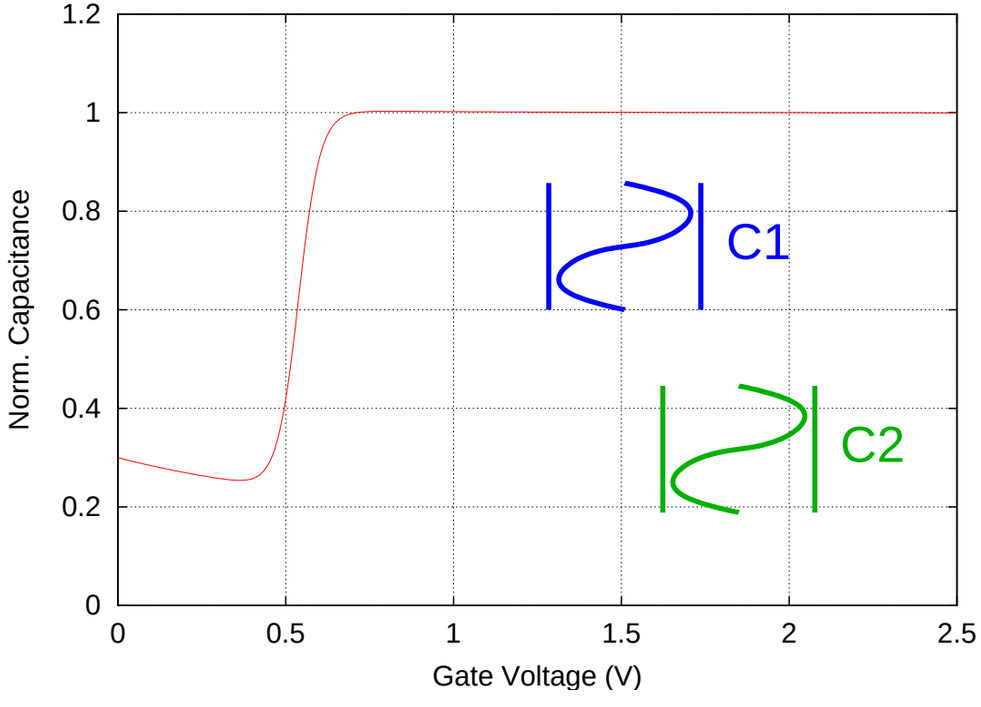
$$G_m(x) = G_m(0)\frac{\partial}{\partial x}\left\{\tanh\left(x + \frac{0.82}{3}x^3 + \frac{2.14}{5}x^5 - \frac{0.60}{7}x^7\right)\right\}$$

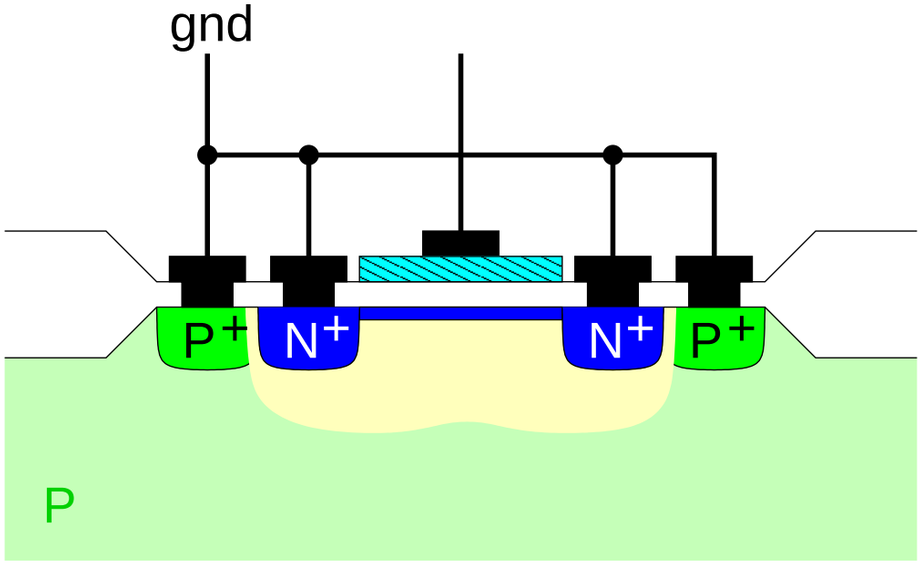
Circuit Elements: Small Transconductors (GM3)



- Pseudodifferential: poor common mode rejection
- Good linearity
- Low accuracy: Gm depends on Vcas and Cm(Vin)
- Low power efficiency

Circuit Elements: Capacitors: Inversion MOSFETs

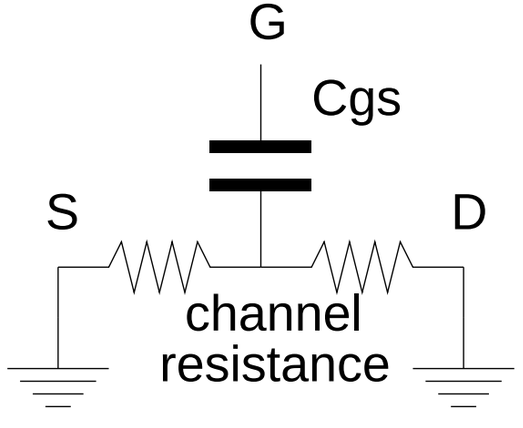




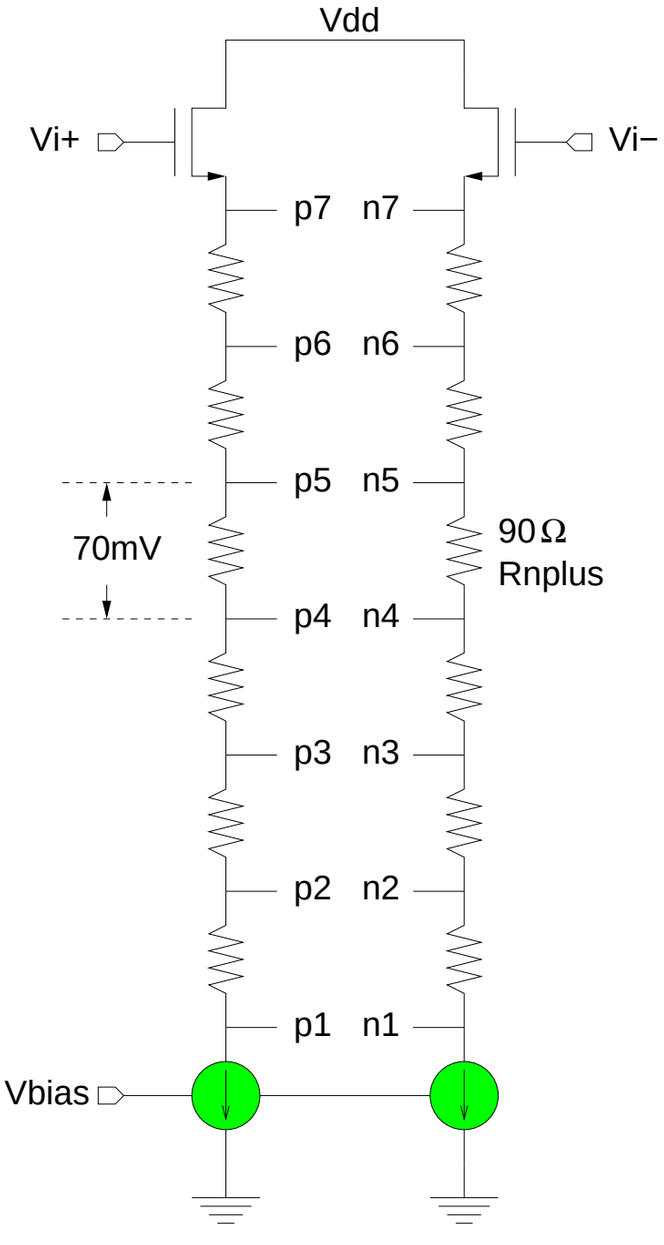
Channel resistance is not simulated unless

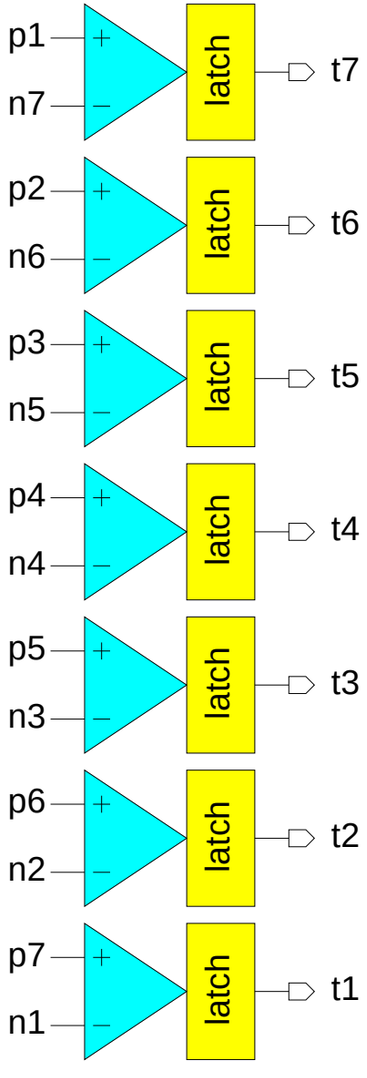
"nqsmod=1" is specified on every capacitor

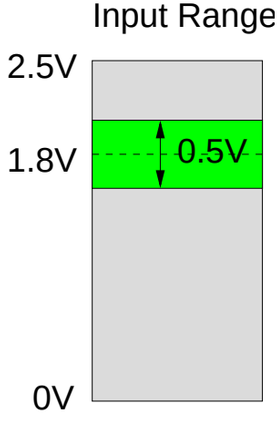
Big capacitors must be split into parallel, small, capacitors to improve their Q



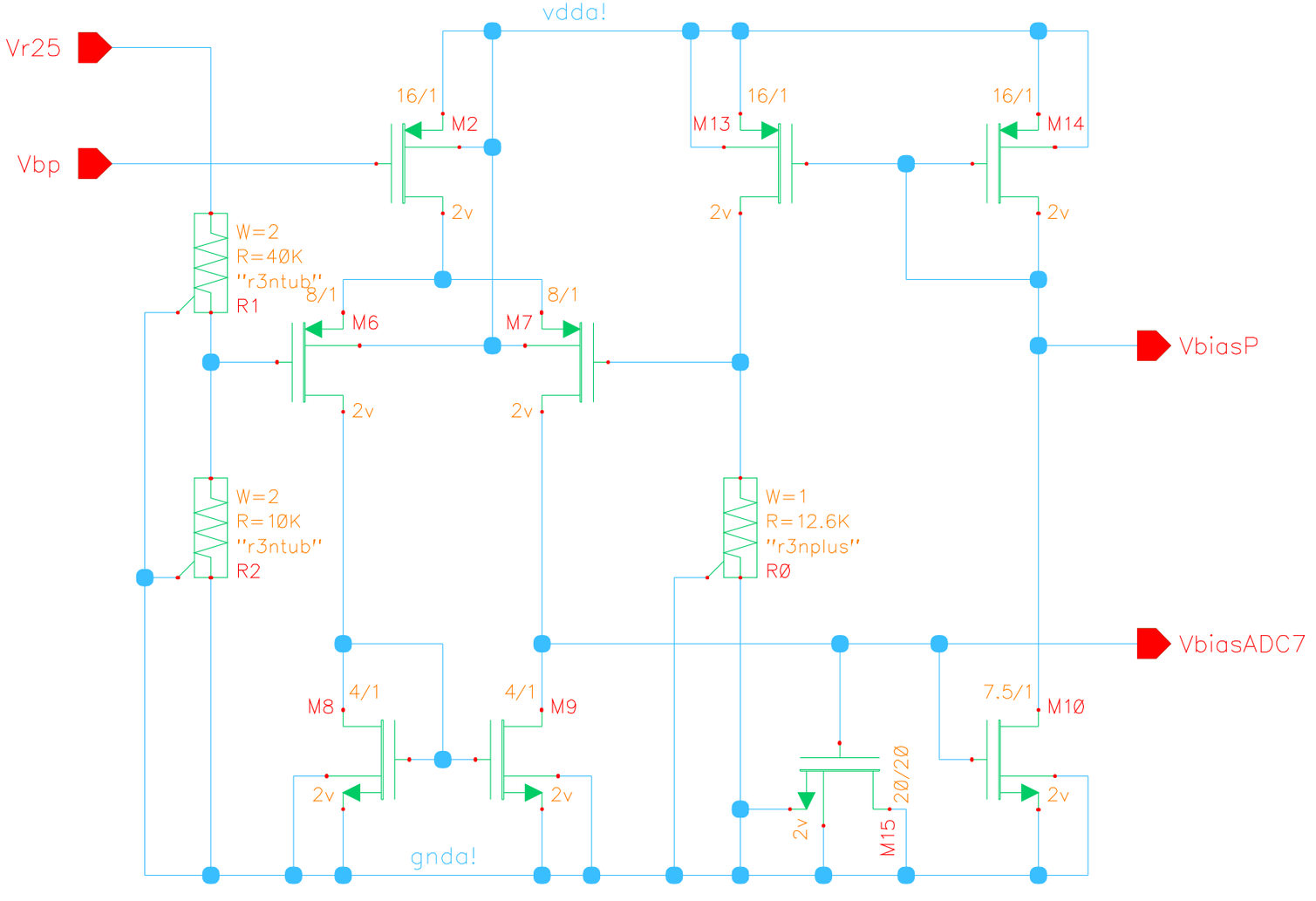
Circuit Elements: ADC





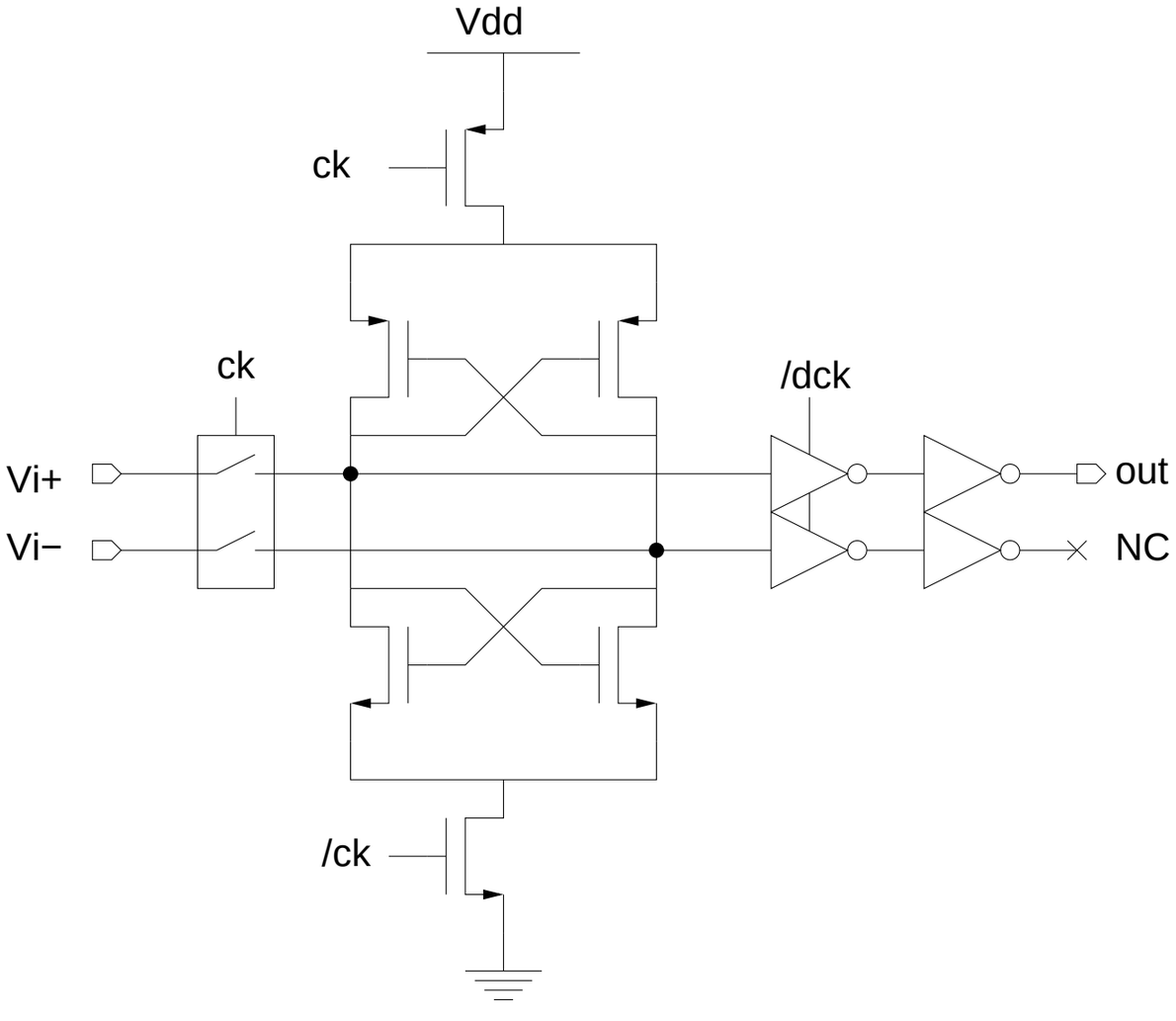


Circuit Elements: ADC biasing

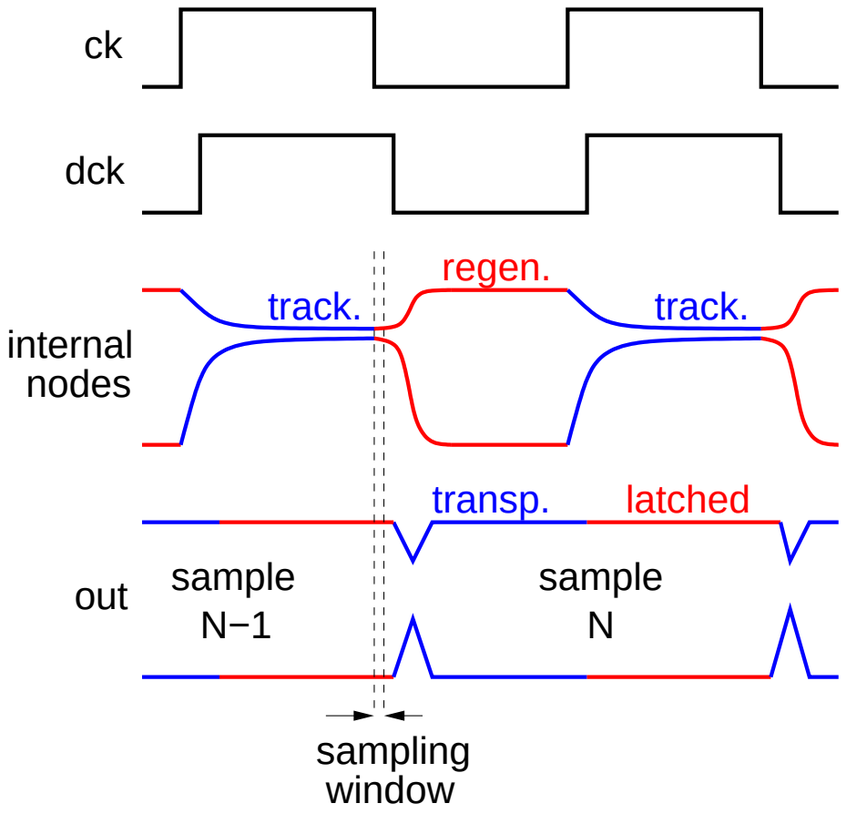


Circuit Elements: ADC's comparators

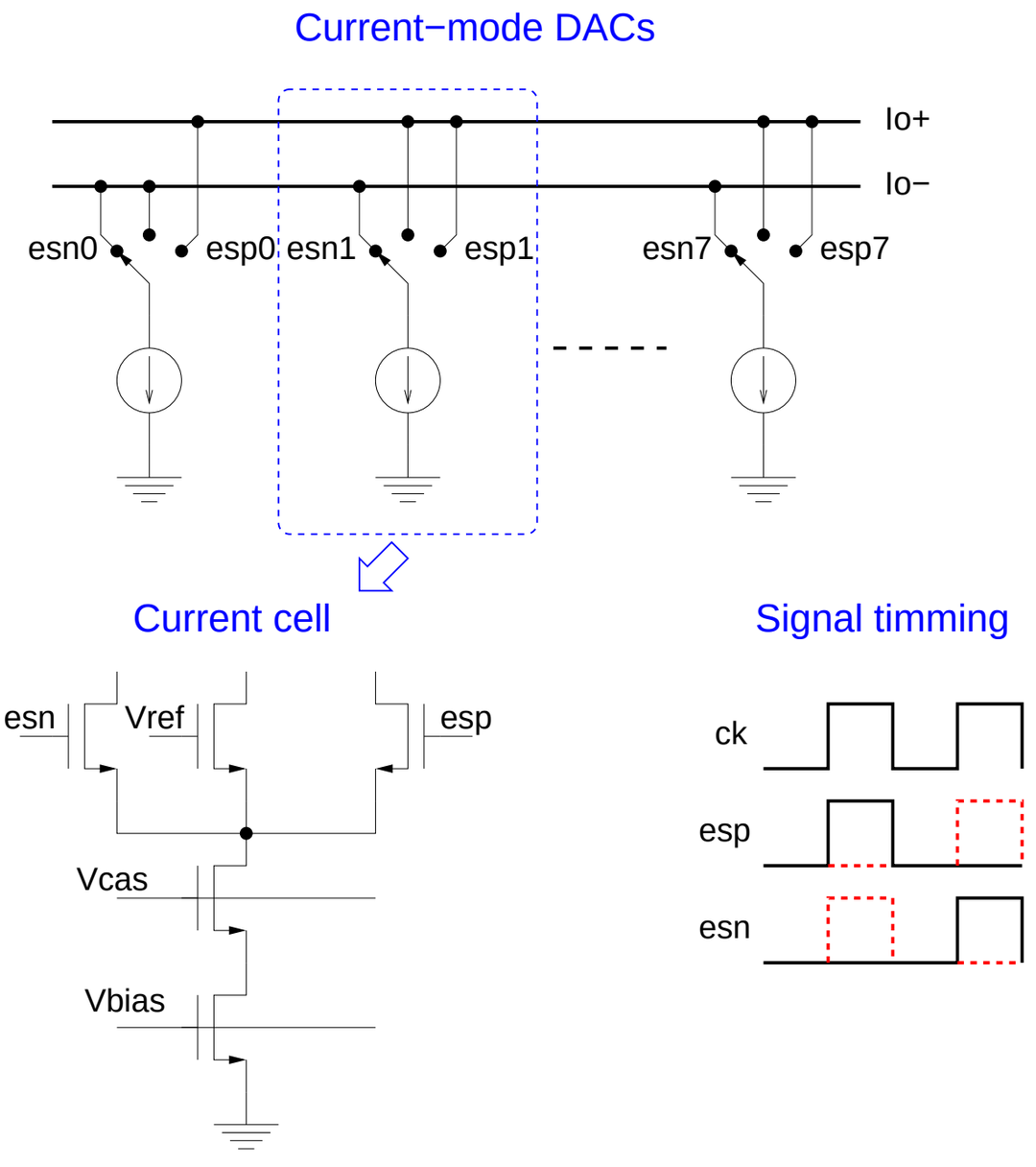
Comparator & Latch



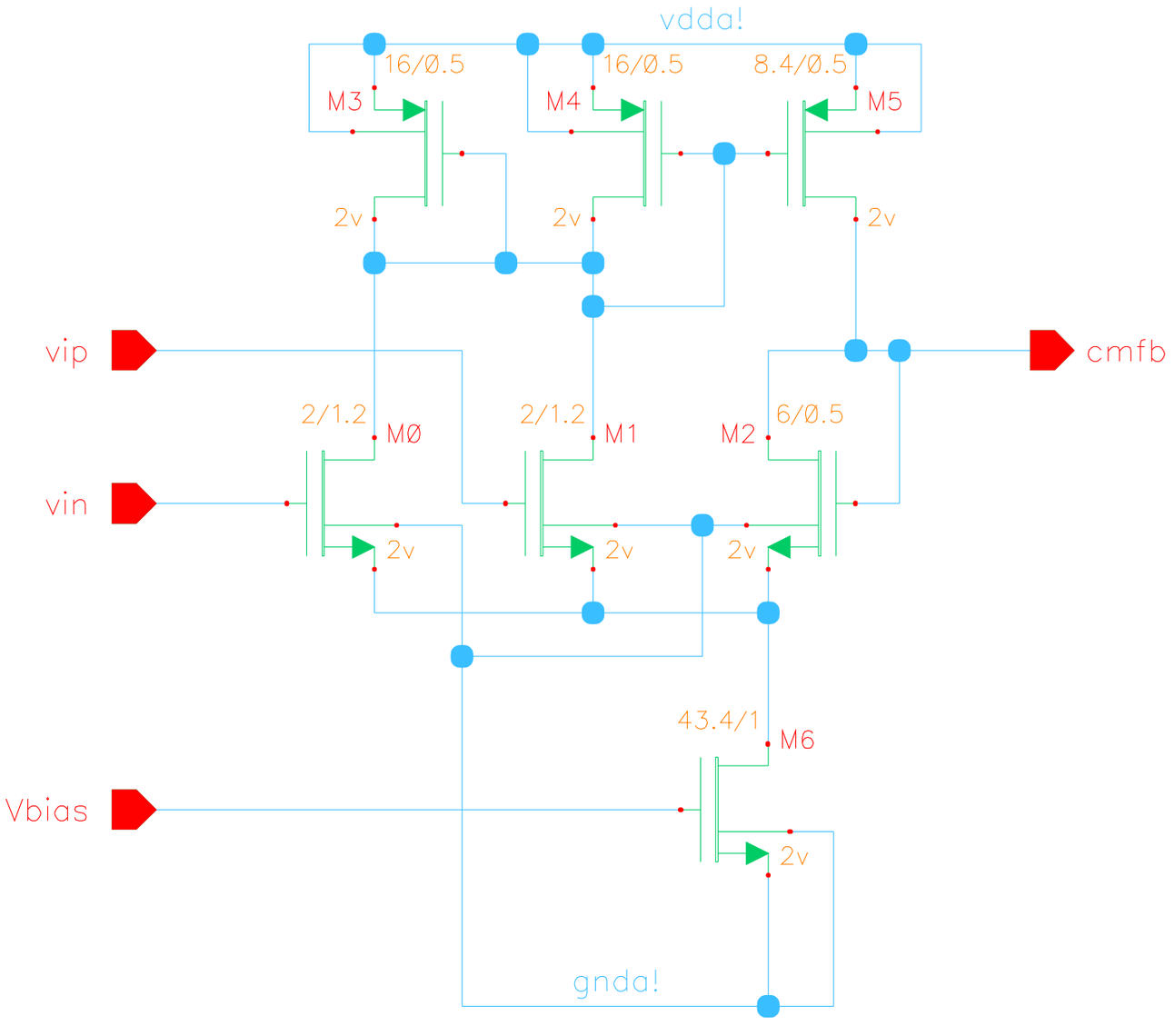
Signal Timming



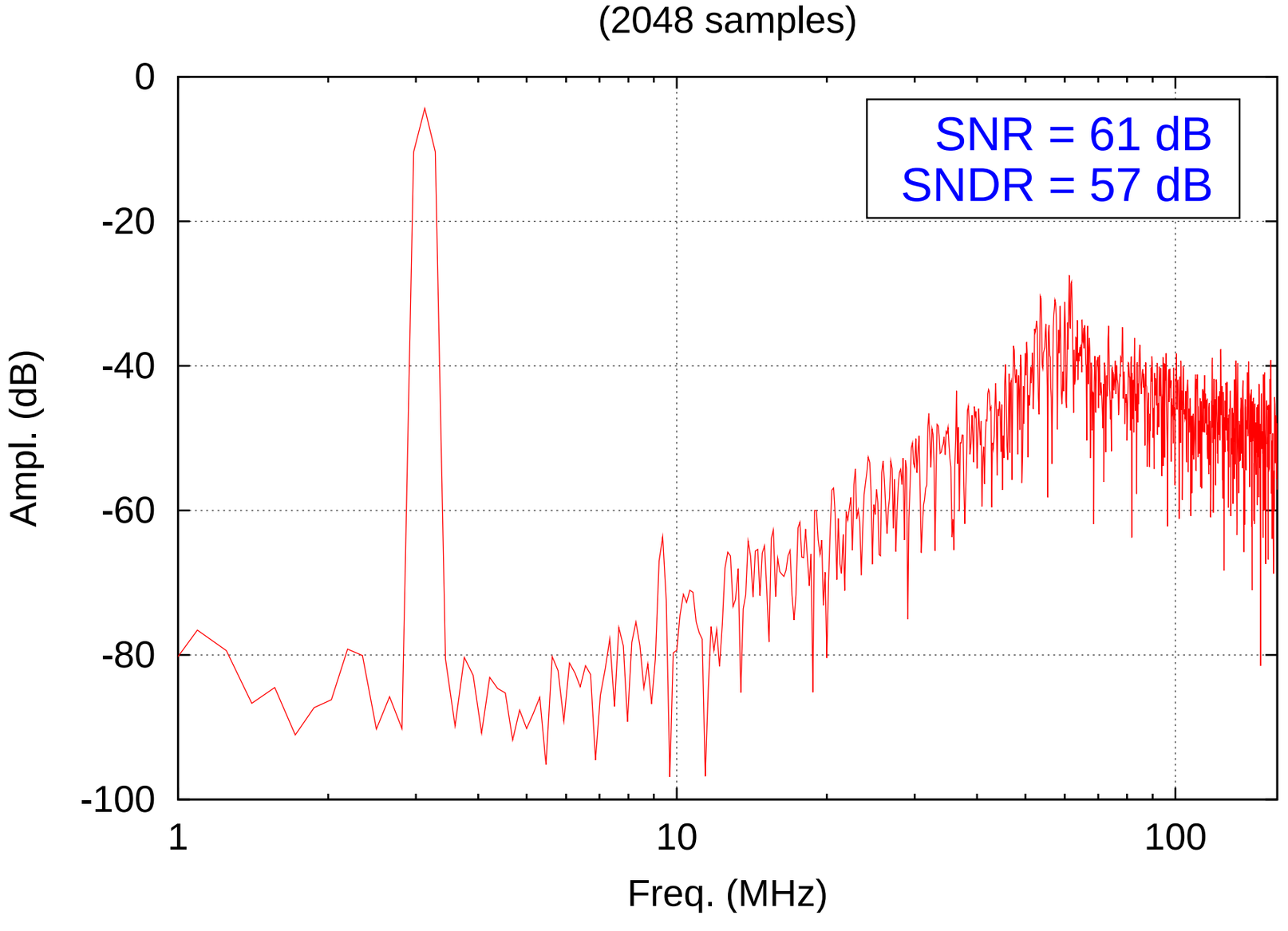
Circuit Elements: Current-mode DACs



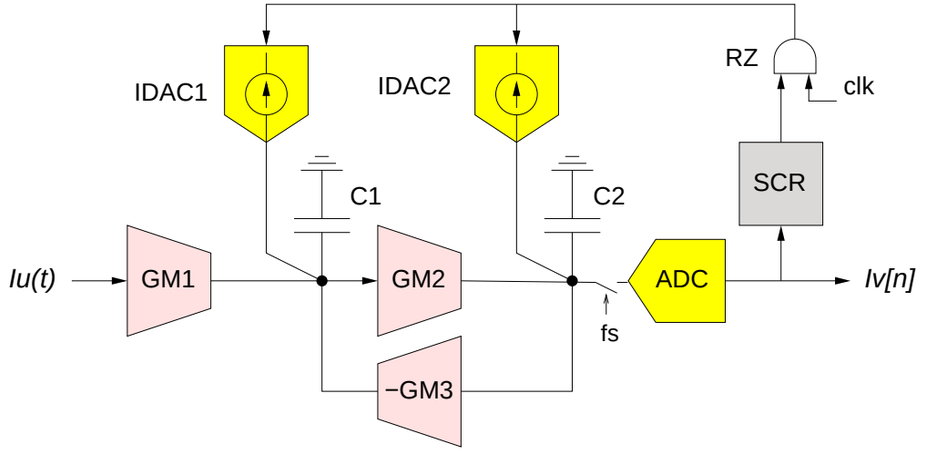
Circuit Elements: CMFB



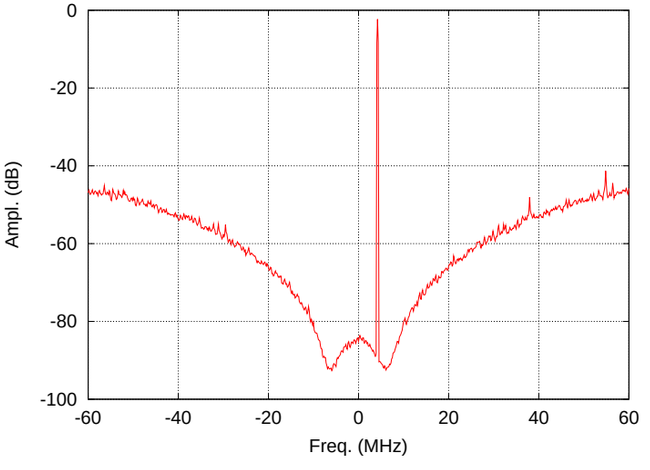
Real DSM results (spectre simulation with extracted blocks)

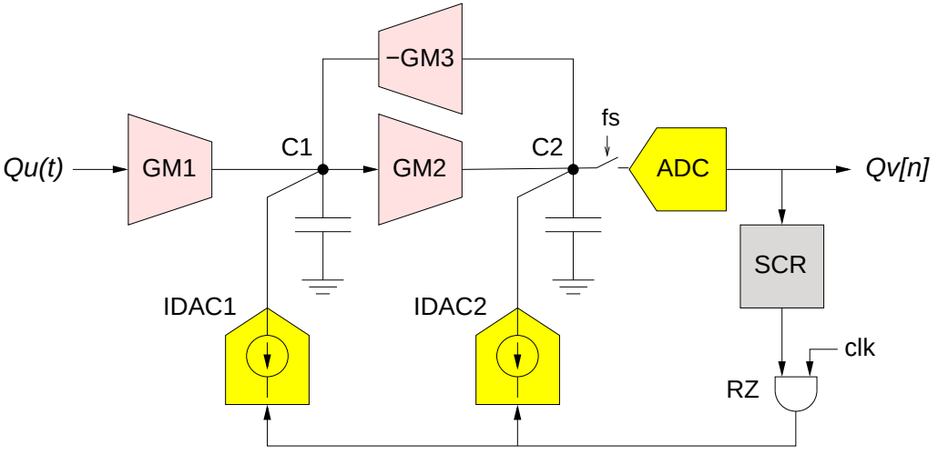


Complex DSM schematic

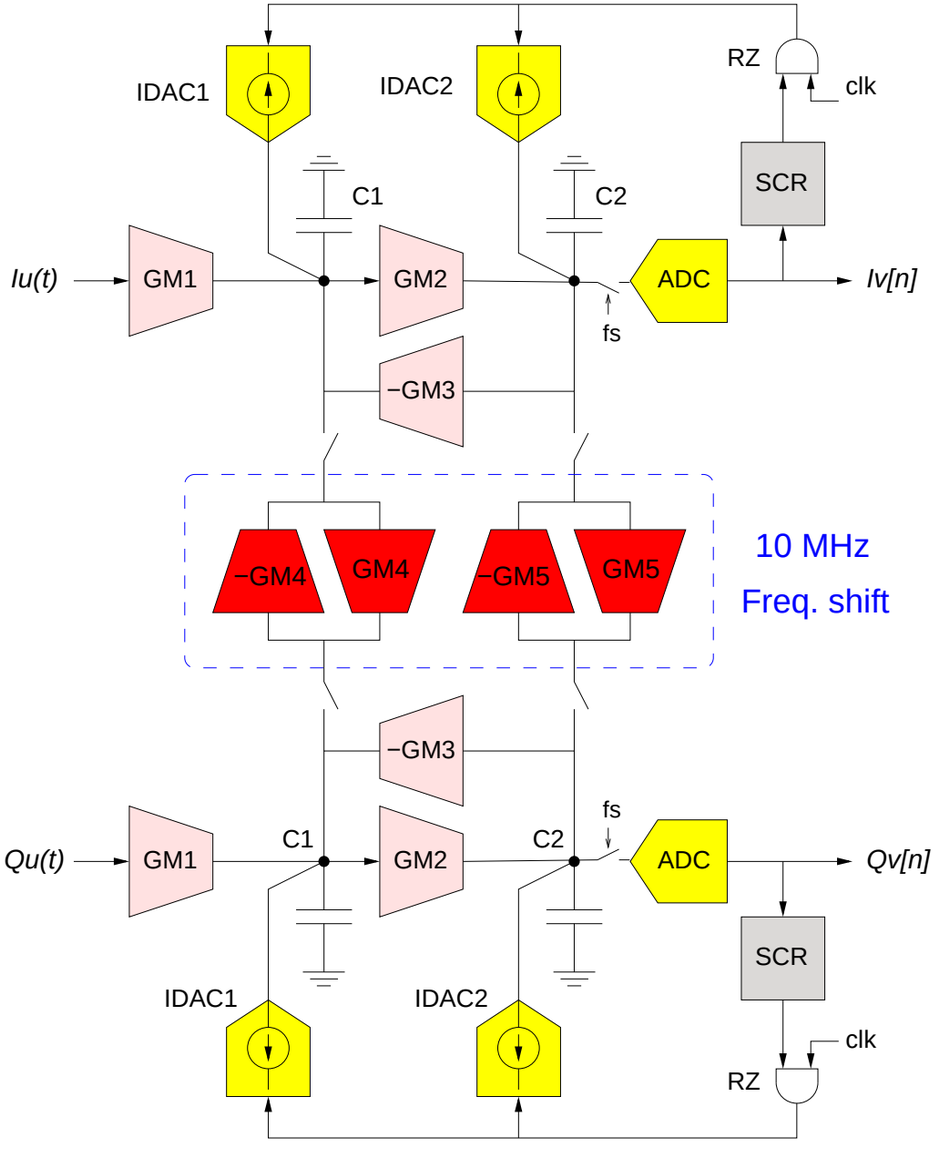


Two real modulators

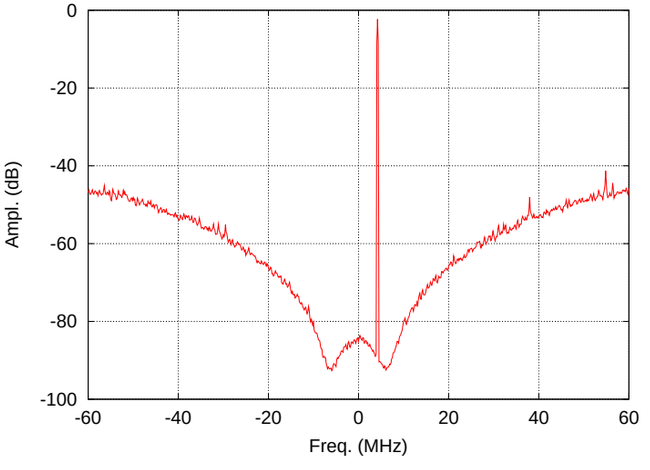




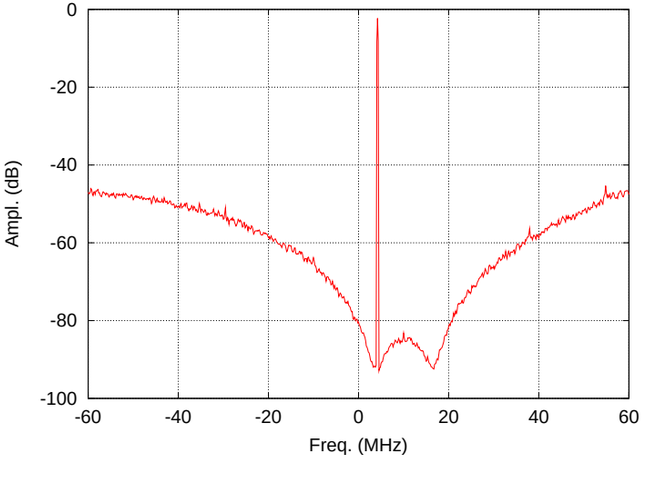
Complex DSM schematic



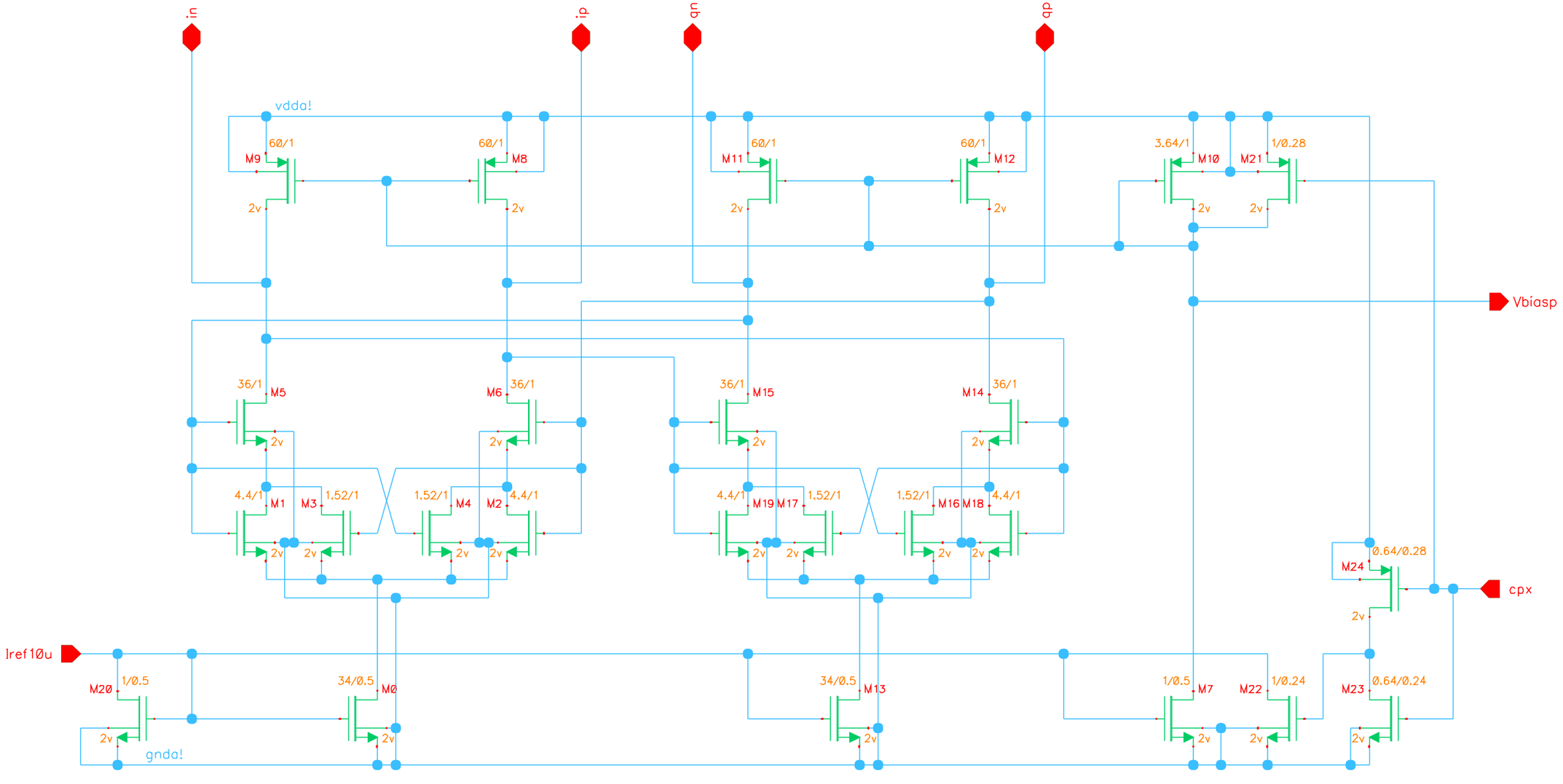
Two real modulators



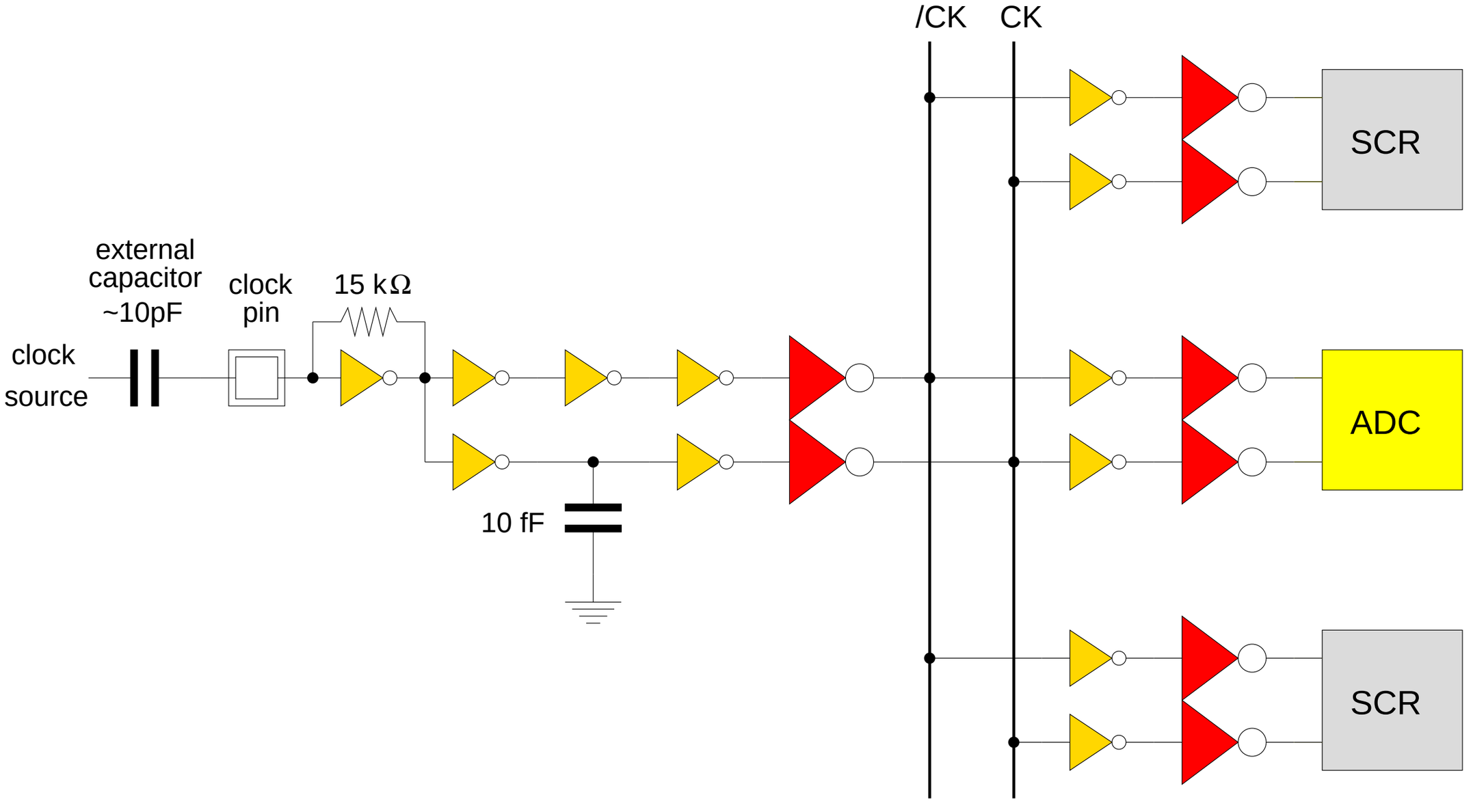
Complex modulator



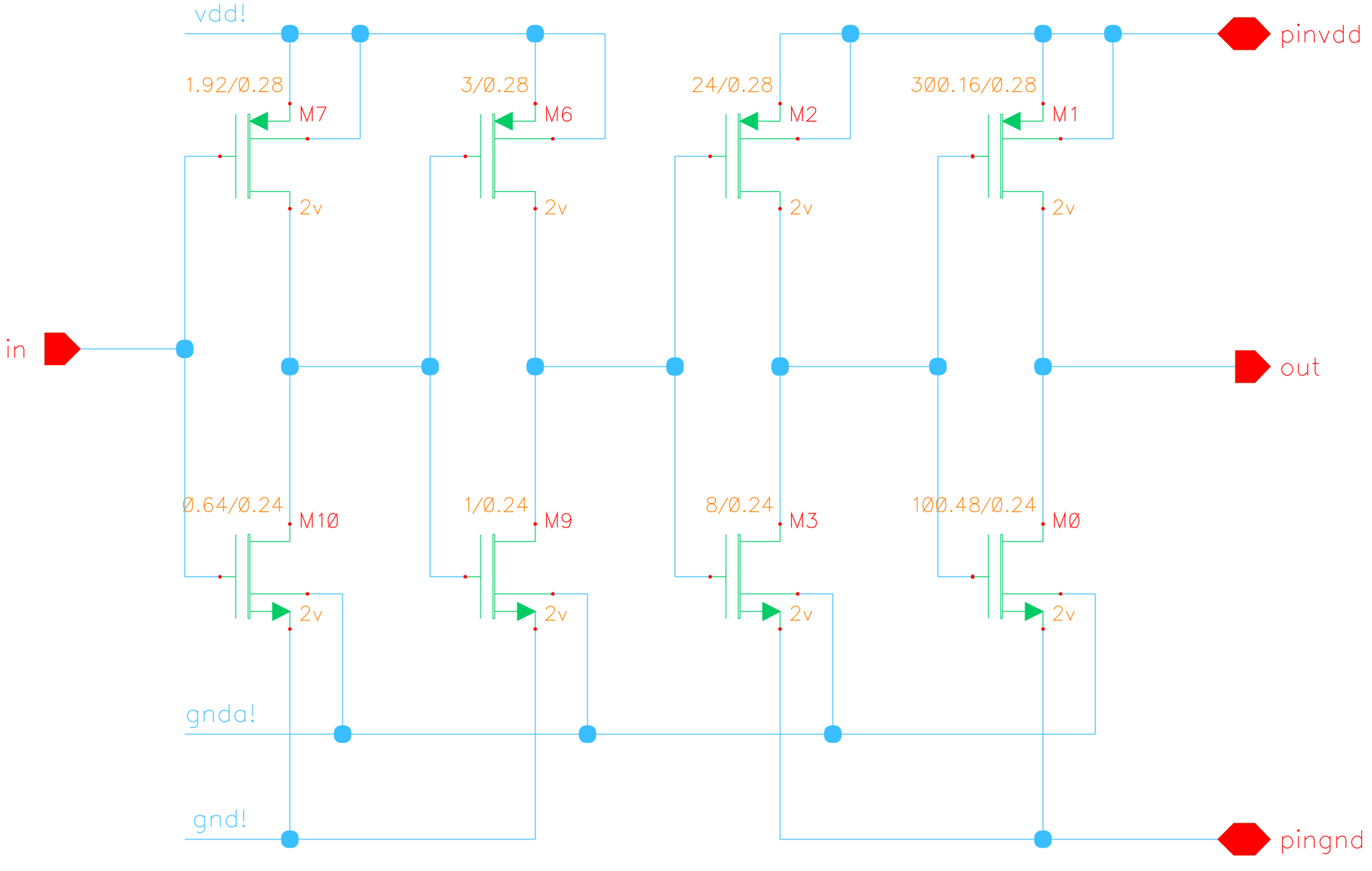
Cross-coupled transconductor switching



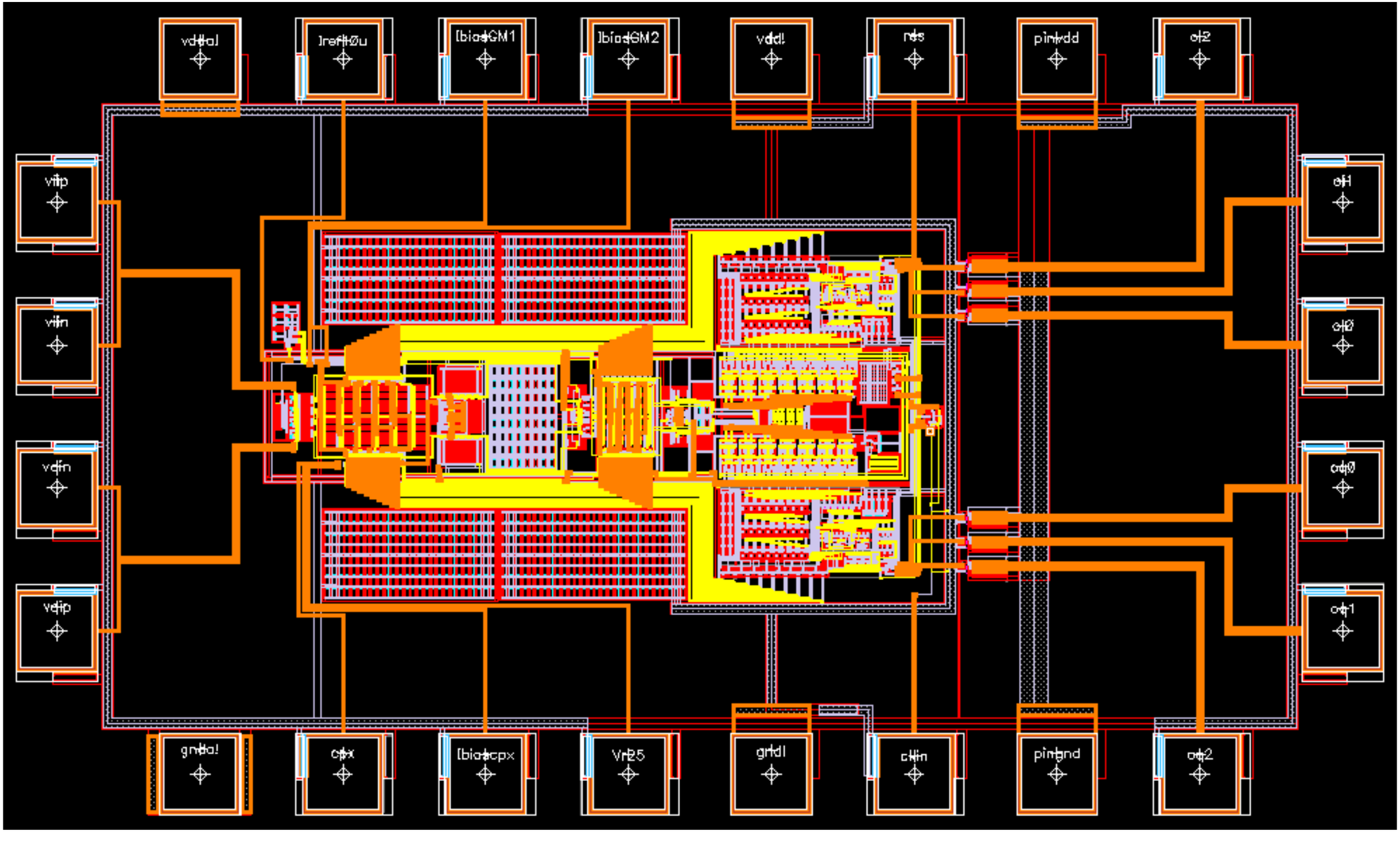
Clock distribution



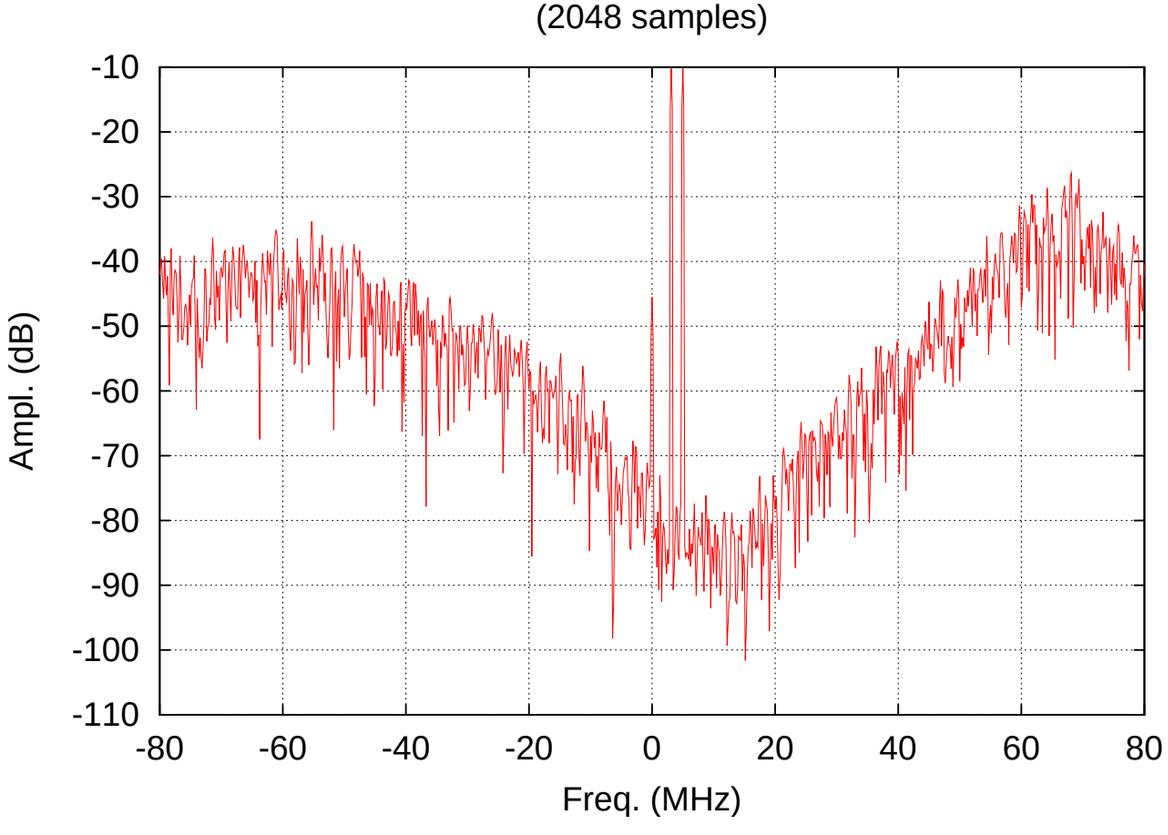
Pin drivers


vdd!
1.92/0.28
M7
3/0.28
M6
24/0.28
M2
300.16/0.28
M1
pinvdd
2v
2v
2v
2v
in
out
0.64/0.24
M10
1/0.24
M9
8/0.24
M3
100.48/0.24
M0
2v
2v
2v
2v
gnda!
gnd!
pingnd

Circuit Layout (2.5-V, 0.25-μm CMOS, 1480$\times$880 μm^2)



Simulated results (extracted circuit)



- Full extracted circuit with parasitic capacitances
- Two−tone test show no intermodulation products
- SNR: 55 dB (+3dB dual tone)
- Total power ~25 mW

Before chip submission

⇨ Chip completion.

- ✔ Antenna check
  - Is it removed from Cadence?
- ✔ Fill patterns
  - What are they for?
  - Are they really needed?

⇨ Other issues....

Setup for measurement