A dual-mode, complex, ΔΣ ADC in CMOS for Wireless-LAN receivers.

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Abstract

In this work a dual-mode complex multibit continuous-time ΔΣ modulator for a standard $0.25\mu m$ CMOS technology is presented. This modulator is intended for the analog-to-digital conversion in multi-mode wireless-LAN receivers (802.11a/b/g) which require wide bandwidth and moderate resolution. Then, a low oversampling ratio of 16 along with a clock frequency of 320 MHz provides a signal bandwidth of 20 MHz for a 9-bit resolution with a second-order modulator. The modulator can be configured for two different modes of operation depending on the type of radio receiver chosen: "zero-IF" (ZIF) and "low-IF" (LIF). The former mode is better suited for 802.11b, while LIF mode is more adequate for 802.11a/g applications. The loop filter is based on transconductors and MOS-capacitors allowing for low power consumption and small chip area. The modulator also includes two 3-bit quantizers, both with their corresponding DWA scrambler. The supply voltage is 2.5V and the measured power consumption is 32 mW. Experimental results using both sine-wave and OFDM signals are presented. The obtained SNR and SNDR are 55dB and 53.5dB, respectively. A high image rejection of 47dB is achieved owing to proper layout techniques. When using OFDM signals, a minimum error vector magnitude of 1.3% is obtained. Finally, the active chip area is $0.44mm^2$.

Keywords: Delta-Sigma, complex, continuous-time, Wireless-LAN

I. Introduction

The demand of low cost transceivers for IEEE802.11 wireless LAN [1] has resulted in the design of highly-integrated receivers based on zero-IF (ZIF) or low-IF (LIF) architectures, instead of the classical heterodyne receiver which requires expensive off-chip filters. Depending on the standard, IEEE802.11/a/b/g, a particular architecture is more advantageous than the other. Thus, for CCK modulation (802.11b) a ZIF receiver should be used while, for OFDM modulation (802.11a/g) the LIF receiver is more suitable.

In these receivers, the total power consumption has to be kept low to extend the battery life of portable systems resulting in a continuous demand for low power circuit blocks. Among these blocks, the analog to digital converters are typically responsible for a noticeable fraction of the total power budget. When ADCs are Nyquist-rate converters, they have to be preceded by a high-order, high dynamic-range channel selection / anti alias filter. This filter can be difficult to design and result in an increased power consumption and image rejection degradation due to channel matching issues. A better design can be based on the use of an oversampled ΔΣ converter [2–4]. In this case, most of the filtering is moved into the digital domain, where no matching issues exist, and power consumption can benefit from technology scaling.

The obvious disadvantage of ΔΣ ADCs is the high clock rate required. In order to keep the clock frequency under reasonable limits the oversampling ratio (OSR) have to be reduced while still maintaining the required resolution for the converter. This can be achieved using multibit quantizers. The DAC linearity issues of these multibit converters can be overcome by using dynamic element matching techniques such as data-weighting-averaging [5, 6]. If the loop filter of the ADC is made using continuous-time circuits (CT) [7] instead of the well known discrete-time (DT) blocks, the total ADC power can be keep low even for sampling frequencies in the hundreds of megahertz range.

Moreover, the complex nature of the received signal would demand two identical ADCs. The sampling frequency would be doubled for LIF receivers using Nyquist-rate ADCs with respect to a ZIF receiver, resulting in a waste of power. Conversely, if a ΔΣ ADC with a complex loop filter is used the sampling rate remains the same and no extra power is needed.

In this work we report a complex, continuous-time, multibit, dual-mode ΔΣ ADC intended for IEEE802.11a/b/g wireless-LAN receivers.

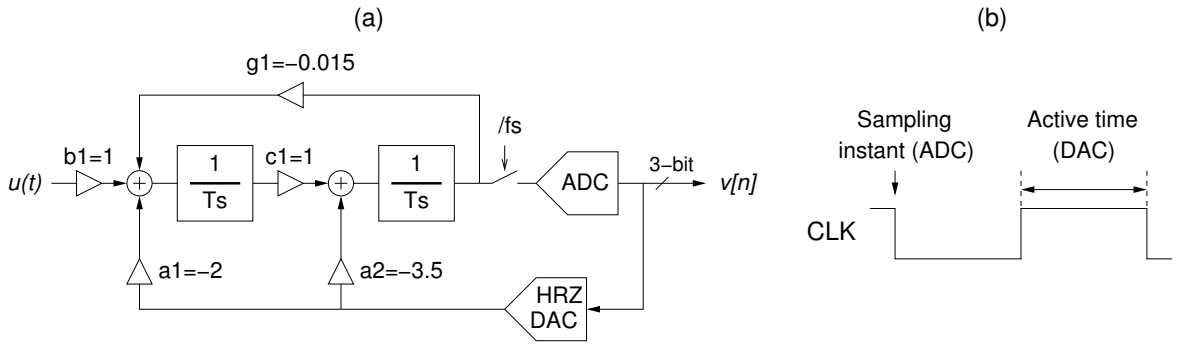

Fig. 1. (a) Diagram of the second-order, continuous-time, multibit, real modulator and (b) Timing.

II. Complex ΔΣ modulator design

The target SNR was 60dB allowing 5dB of design margin above the required receiver SNR of 55dB. In order to achieve the target resolution with an OSR of only 16, a second-order, multibit ΔΣ modulator with a 3-bit quantizer and zero-optimized NTF was chosen.

The design of the complex modulator begun with the corresponding design of a CT modulator for each of the two channels of the complex modulator in ZIF mode. The block diagram of this real modulator is shown in Fig. 1(a). The coefficients were obtained by mapping the NTF of the CT modulator to that of an equivalent DT modulator using the modified Z-transform [8] taking into account the timing of the HRZ DAC waveform.

The ADC samples its input on the falling edge of the clock, but its output is not needed until the second half of the clock cycle owing to the HRZ waveform (Fig. 1(b)). In this way, the ADC has half a cycle to perform the analog-to-digital conversion and, the effect of the ADC's comparator's metastability on modulator performance is minimized [7]. The DAC is turned on and off on each cycle providing a half-delayed, return-to-zero signal (HRZ). Modulators using return-to-zero signals exhibit less performance degradation due to turn-on / turn-off transients of the DAC because these transients do not depend on previous output data [9, 10], although they exhibit higher clock jitter sensitivity.

The coefficients shown in the modulator of Fig. 1(a) are not scaled. Scaling can be applied to adjust the amplitude distribution of the two integrators to proper values without changing the NTF. This scaling was done taking into account the input range of the transconductors that will be used for the integrators ($\pm 500mV$).

The CT integrators of Fig. 1(a) are implemented as transconductors loaded with capacitors, resulting in the schematic of Fig. 2 (one half). The sampling is carried out only at the ADC, while the loop filter is a CT circuit providing implicit aliasing rejection for this kind of modulator [7]. The DAC of Fig 1(a) is replaced by two current-output DACs, implemented as arrays of identical, switchable, current sources controlled by a thermometer-code digital input. Multibit modulators are sensitive to DAC nonlinearity. In order to reduce this effect, a scrambler, SCR, is added between the ADC output and the DAC inputs. This circuit improves the linearity of the DACs by selecting a different set of DAC elements on each sample, thus performing dynamic element matching. A data weighted averaging algorithm (DWA) [5, 6] was chosen for the scrambler due to its simplicity and because system level simulations show that this algorithm is effective enough to remove the effect of mismatches of DACs elements as high as 2% or more. Quadrature DEM algorithms have been proposed in order to improve the image rejection of complex ΔΣ ADCs [11, 12]. However, these algorithms can not correct the mismatch between the I & Q channels of the whole complex modulator, that, in our case can be as high as those of DAC's elements. In our design, a simpler, independent scrambler is used for each real modulator and image rejection performance is obtained through proper layout techniques. The layout of the elements of the I & Q channels, including DAC elements, capacitor elements, transconductors, and the resistors of the ADCs were interlaced and laid out following a common-centroid topology.

Two real modulators can be combined into a single complex modulator as can be seen in Fig 2. Without the cross-coupling transconductors, each real modulator works independently and the resulting NTF of the complex modulator is centered around DC (ZIF mode). If transconductors GM_4 and GM_5 are enabled, a +10 MHz frequency shift is obtained (LIF mode) . Therefore, by enabling the coupling transconductors we can change from a modulator for zero-IF receivers (ZIF mode) to a modulator for low-IF receivers (LIF mode). The optimum modulator mode can be selected dynamically in a multi-mode receiver based on this ADC.

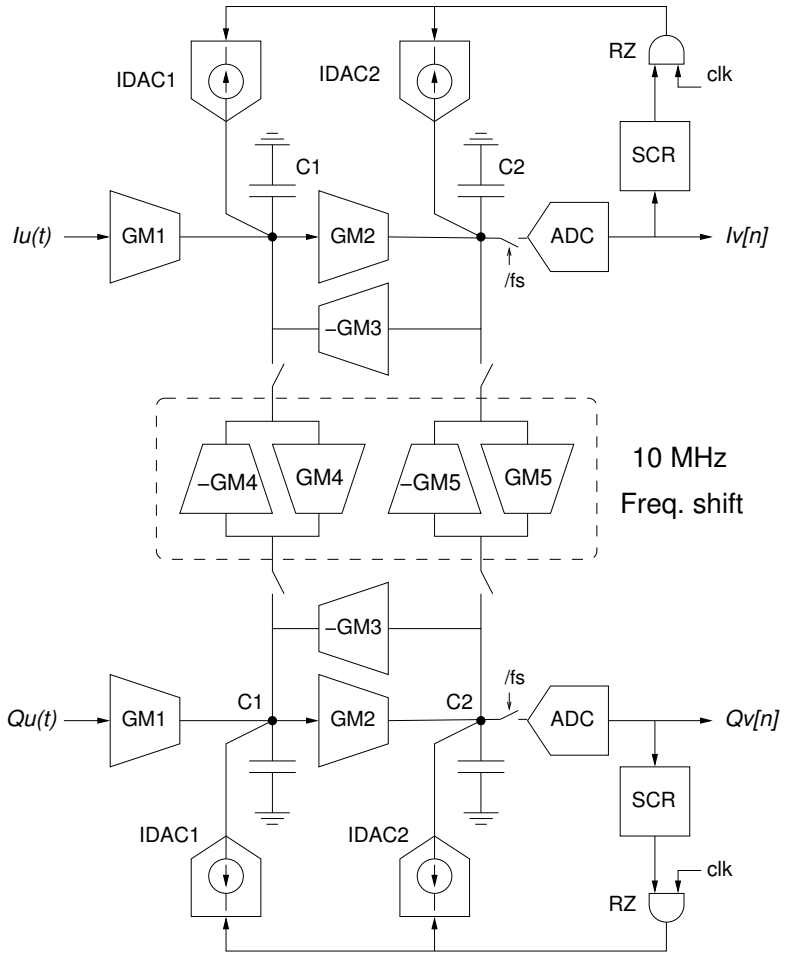

Fig. 2. Complex modulator schematic.

The modulator architecture was tested using a behavioral-level simulator, including non-ideal effects such as nonlinear transconductors, integrators with finite DC gain and a nondominant pole, mismatch, thermal noise, clock jitter, etc. The modulator showed low sensitivity to process variation, allowing for relative variations higher than a 20% in the main modulator elements, namely, transconductors, capacitors and DACs. The assumed relative mismatch was estimated at 1%, resulting in no significant loss of SNR when the scramblers are active, and an image rejection about -35dB. Experimental results shows that this mismatch estimation was quite pessimistic (See section IV).

III. Circuit implementation

The modulator was implemented in a standard, 0.25 μm, 4-metal layer CMOS technology using only core transistors, operating at a supply voltage of 2.5 volts and a clock frequency of 320 MHz. The input signals are differential with a full-scale range of $\pm$500mV (-9dBV).

The integrators were built using transconductors and capacitors (Gm-C). This approach had the advantage of a simpler circuit structure resulting in lower power consumption than other approaches, for instance, based on operational amplifiers. In our case, the target specifications for resolution and linearity are relaxed enough to allow the use of the Gm-C approach.

The nominal values for transconductor and capacitor are listed in Table I. The size of GM_1, C_1, GM_2 and C_2 were determined taking into account the contribution of thermal noise to the total ADC noise, and by making it nondominant (about -6 dB below quantization noise) to avoid the degradation of the effective resolution of the converter. On the other hand, if the thermal noise is made much lower than the quantization noise, there will be a noticeable increase in power

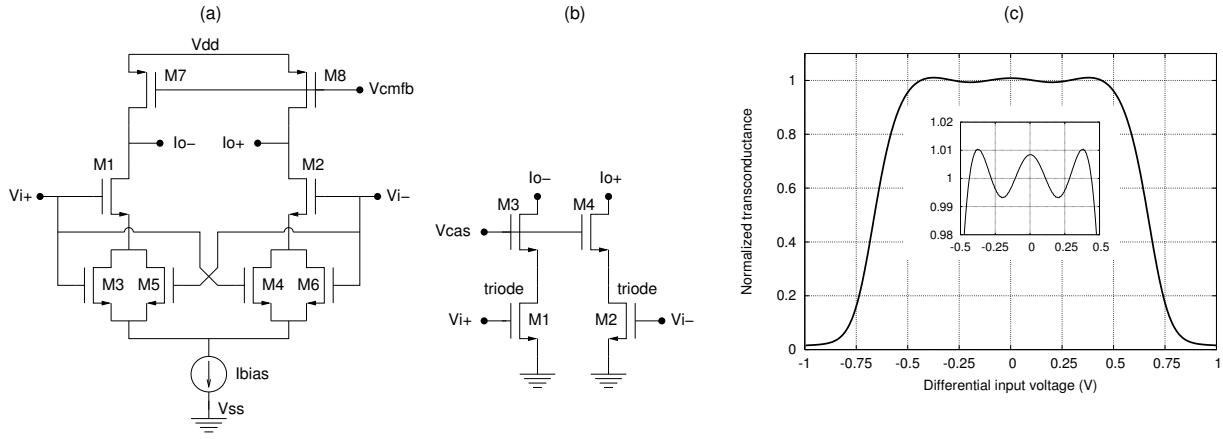

Fig. 3. Schematic of transconductors: (a) GM_1, GM_2, GM_4 and GM_5. (b) GM_3. (c) Normalized transconductance for transconductors GM_1, GM_2, GM_4 and GM_5. A zoom of the upper part of the curve is shown in the inset.

TABLE I

NOMINAL TRANSCONDUCTANCE AND CAPACITOR SIZES.

Component	Value
GM_1	$1000\mu A/V$
GM_2	$200\ \mu A/V$
GM_3	$15\ \mu A/V$
GM_4	$325\ \mu A/V$
GM_5	$24\ \mu A/V$
C_1	$5.165\ pF$
C_2	$0.376\ pF$

consumption. Therefore, there is a trade-off between resolution and power consumption. In our case, the resolution penalty due to thermal noise is about 1dB.

GM_3 was obtained from the frequency of the optimized zero of the NTF, ω_{oz}:

$$GM_3 = \frac{\omega_{oz}^2}{GM_2 C_1 C_2} \tag{1}$$

And GM_4 and GM_5 were obtained from the frequency shift of the complex modulator ($\omega_{sh} = 2\pi \cdot 10\,MHz$):

$$GM_4 = \omega_{sh} C_1 \quad ; \quad GM_5 = \omega_{sh} C_2 \tag{2}$$

The transconductor schematics are shown in Fig 3. Note that GM_3 has a different, simpler, structure (Fig 3(b)) than the other transconductors due to its small transconductance. The structure of Fig 3(a) was proposed in [13]. It is a low-noise, highly linear transconductor whose normalized transconductance is shown in Fig 3(c). In the -0.5 to +0.5 voltage range, the ripples of the transconductance are only about 1%, providing a low distortion for the modulator. This is particularly significant for the input transconductors, because their distortion is unshaped by the loop filter. Transconductor GM_3 is implemented using MOSFETs operating in triode region. This transconductor also exhibits a good linearity, although it is not highly power-efficient (lower transconductance than the transconductors of Fig 3(a) for the same current consumption). However, these transconductors do not have a noticeable impact on the total power consumption due to their small value.

Capacitors were implemented as inversion MOS capacitors. These capacitors are, in fact, N-channel MOSFET transistors with grounded source and drain terminals, and therefore neither special cells nor technology options are required. In addition, the high capacitance density of MOS capacitors minimizes the chip area. The variation of the capacitance for the intended ranges is quite small, about 0.1%. The distortion introduced by the nonlinear capacitance is masked by the distortion of the transconductors.

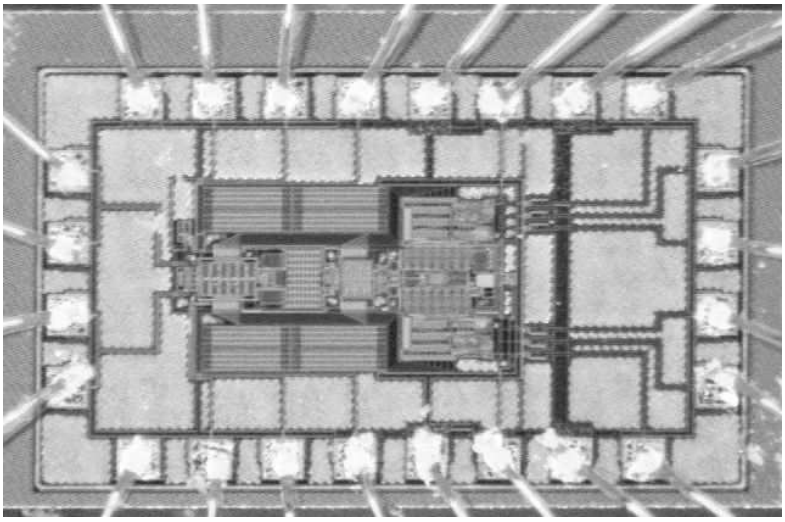

Fig. 4. Photograph of the test chip bonded to a PCB.

The flash ADC consists of a differential input buffer and a voltage shifter based on two resistor strings, and seven regenerative comparators and latches. Comparators consist of a pair of input switches, a full-swing latch and two C^2MOS dynamic latches. The time-constant of the comparator is about 50 ps, and the corresponding metastability probability is one cycle every $2 \cdot 10^{10}$ cycles. The estimated offset is 8mV.

Current-output DACs were built using eight identical current cells controlled by a thermometer-code input. Each cell is a cascode current source followed by current-steering switches. The mismatch between current cells was minimized using a common-centroid layout for DACs. Also, I and Q channel DAC cells are interlaced to improve image rejection. The effect of these mismatches is further reduced by the DWA algorithm whose implementation is presented in the next subsection.

IV. Experimental results

The proposed converter was fabricated and a test chip was bonded to a PCB using a room-temperature, conductive glue; the chip photograph is shown in Fig 4. The chip area is $1480 \times 880\ \mu m^2$ including pads. Without pads, the active area is reduced by 2/3. The chip was powered by three separate power supplies, all of them operating at 2.5 V. A power supply was provided for analog circuitry, another power supply was used for digital circuitry, and the third power supply was used only for output pin drivers. The power consumption, not including pin drivers, was 30.4 mW for the modulator operating in the ZIF mode and 32 mW for LIF mode. This small difference is due to the coupling transconductors (Fig 2) that are disabled in the ZIF mode. The power consumption of the digital blocks was 12 mW in both modes, and the power consumption of the pin drivers was about 10 mW. This later power consumption is highly dependent on the load capacitance.

For measurements, the input is a complex differential signal obtained either from a Direct Digital Synthesizer (DDS) or from a programmable vector signal generator, capable of generating OFDM signals. The clock signal is obtained from a 320 MHz sine-wave RF generator. The output bits are acquired by a high-speed logic analyzer and then transferred to a computer for further processing.

A set of measurements were performed using complex sine-wave input signals. These signals were obtained from an Analog Devices AD9854 DDS, evaluation board. When the cross-coupling transconductors (Fig 2) are disconnected (ZIF mode), the modulator can be viewed as two independent real, single-input modulators. The corresponding output for these modulators is shown in Fig 5(a) for a 3.125MHz, -13dBV single-tone input. When the two modulators are considered as a complex modulator, the corresponding output includes both positive and negative frequencies (Fig 5(b)). The noise floor shape follows the designed NTF where the two zeros are still visible, although they are filled with noise due to several nonideal effects including finite integrator gain, thermal noise and clock jitter. In addition to the input test tone, several other tones are present at the output. The observed DC level corresponds to about 10mV. The image frequency, IM, (at -3.125MHz) is 47.2dB lower than the input signal. This high image rejection is achieved mainly due to the proper layout of the circuit and it is high enough to operate the receiver without any ADC calibration. Several harmonics can also be

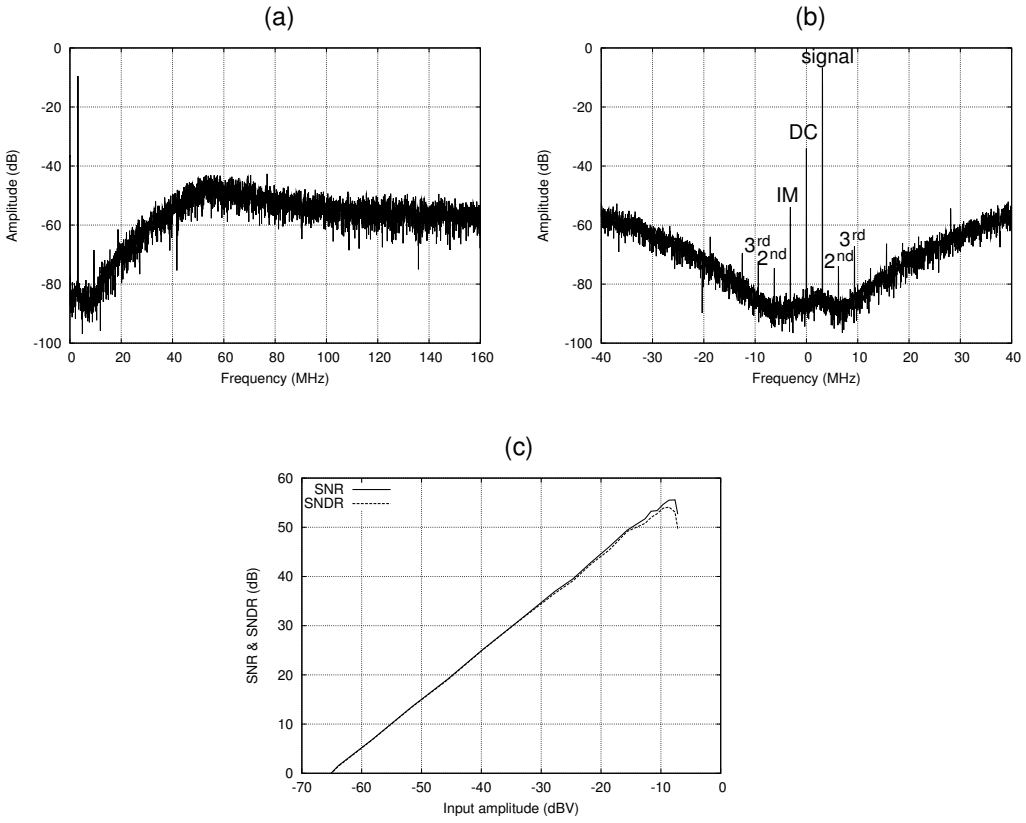

Fig. 5. Output spectra for (a) single real modulator, (b) complex, ZIF mode, modulator (detail), and (c) SNR and SNDR plots as a function of the input amplitude.

observed in the output spectrum, but their amplitudes are small. They are mainly originated by the input transconductor, according to the simulations carried out using its nonlinear transfer characteristic. The total harmonic distortion (THD) for -13dBV input is -58dBc. The measured SNR for this input amplitude is 51.8dB. In Fig 5(c) the SNR and SNDR of the complex modulator in ZIF mode are plotted as a function of the input amplitude. A peak SNR and SNDR of 55.5dB and 53.9 dB are obtained, respectively, for an input amplitude of -9dBV. The effect of distortion is small and only noticeable at high input amplitudes.

By enabling the cross-coupling transconductors, the NTF of the modulator is shifted +10 MHz (LIF mode). The output spectrum for an input amplitude of -13dBV is shown in Fig 6(a). In this plot, the first minimum of the NTF is not easy to see because there is some noise around the input tone, but it is still visible for lower input amplitudes. The DC component corresponds to 8mV. The image rejection is the same as for the ZIF mode, that is 47.2dB confirming a better channel matching than that assumed in simulations. For this amplitude, the THD is -58.3dBc and the SNR is 51.1dB. In Fig 6(b), the SNR and SNDR of the modulator operating in LIF mode is plotted as a function of the input amplitude. The peak values for SNR and SNDR are 54.5 dB and 53.5 dB, respectively, for a -9dBV input amplitude.

The measured SNR and SNDR are less than 1dB below the results obtained from a transistor-level simulation using the extracted circuit from the layout of the actual chip. These simulations did not include thermal noise. Therefore, the thermal noise level is not responsible for performance degradation. The observed SNR decrease with respect to that of an ideal modulator can be attributed to the combined effect of several nonidealities such as finite DC gain in integrators, excess loop delay and clock jitter.

A set of measurements were carried out using modulated OFDM signals in order to test the performance of the modulator for the intended application. In Fig 7(a) the spectrum of a converted baseband OFDM signal is shown with the modulator working in ZIF mode. After demodulating the converted signal, the corresponding constellation of Fig 7(b) is obtained. The error vector magnitude (EVM) for all subcarriers is about 1% rms, well below the maximum 5.6% required for an error-free reception [1]. Similar measurements were done for the LIF mode, obtaining a minimum EVM value of 1.3%

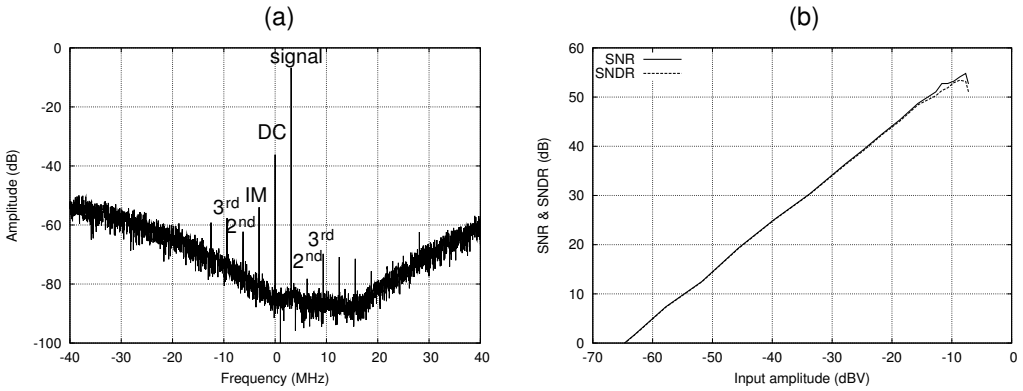

Fig. 6. (a) Output spectrum for complex, LIF mode, modulator (detail), and (b) SNR and SNDR plots as a function of the input amplitude.

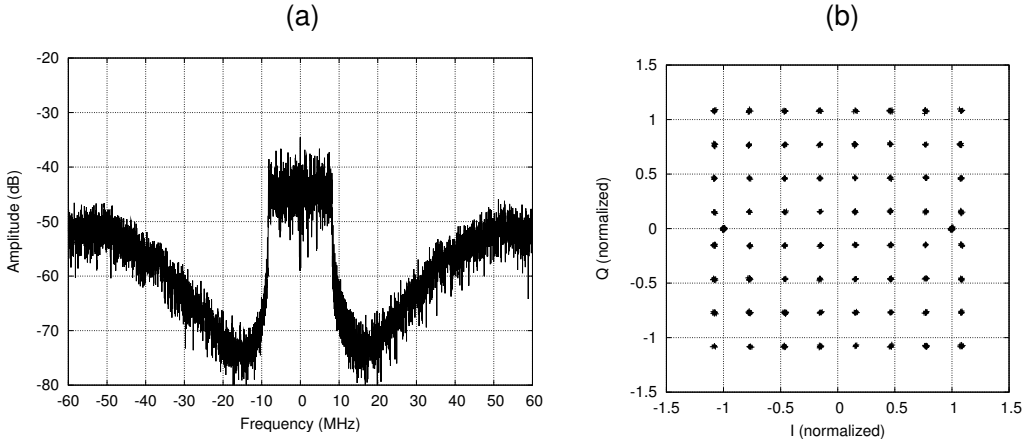

Fig. 7. (a) Output OFDM spectrum for ZIF mode. (b) Its corresponding constellation.

rms.

V. Conclusions

In this work, a complex multibit continuous-time $\Delta\Sigma$ modulator intended for IEEE 802.11a/b/g wireless LAN receivers was designed, fabricated and measured. The modulator can operate on two modes named as ZIF and LIF. In the ZIF mode the modulator acts as two independent real (single input) modulators and it exhibits a NTF that is symmetrical around DC. In the LIF mode, the two real modulators are cross-coupled and the resulting NTF is shifted +10 MHz, making it adequate for the optimal digitization of signals from low-IF radio receivers. The modulator is capable of achieving almost 55 dB of peak signal to noise ratio when running at 320 MHz with an oversampling ratio of 16, which gives a signal bandwidth of 20 MHz. It was designed in a 0.25 μm standard CMOS technology with a 2.5 V power supply.

The measured modulator performance is summarized in Table II.

TABLE II

MODULATOR PERFORMANCE

Technology	$0.25\mu m$, 4M1P, CMOS	
Area w. pads	$1.3mm^2$	
Area w.o. pads	$0.44mm^2$	
Supply voltage	$2.5V$	
Experimental results	ZIF mode *(-10...+10MHz)*	LIF mode *(0...+20MHz)*
Power consumption		
Analog	$18.4mW$	$20mW$
Digital	$12\ mW$	$12mW$
Total	$30.4mW$	$32mW$
peak SNR	$55.5dB$	$54.5dB$
peak SNDR	$53.9dB$	$53.5dB$
ENOB	$8.9bits$	$8.7bits$
Image rejection	$47.2dBc$	$47.2dBc$
DC offset	$10mV$	$8mV$
EVM (min)	1%	1.3%

REFERENCES

[1] IEEE Std., "Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer specifications," Tech. Rep., IEEE Std, 2000.

[2] R. van Veldhoven, "A triple-mode continuous-time sigma-delta modulator with switched-capacitor feedback DAC for a GSM/EDGE/CDMA2000/UMTS receiver," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, December 2003.

[3] S. Paton, A. Di Giandomenico, L. Hernández, A. Wiesbauer, P. Pötscher, and M. Clara, "A 70-mW 300-MHz CMOS continuous-time sigma-delta ADC with 15-MHz bandwidth and 11-bits of resolution," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1062, July 2004.

[4] K. Philips, "A 4.4mW 76dB complex delta-sigma ADC for Bluetooth receivers," *IEEE ISSCC Digest of technical papers*, pp. 64–65, February 2003.

[5] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit delta-sigma A/D and D/A converters using data weighted averaging," *IEEE Transactions on circuits and systems-II: Analog and Digital signal processing*, vol. 42, no. 12, pp. 753–762, December 1995.

[6] R. Schreier, B. Zhang, "Noise-shaped multi-bit D/A converter employing unit elements," *IEE Electronics Letters*, vol. 31, no. 20, pp. 1712–1713, September 1995.

[7] J. A. Cherry and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for high speed A/D conversions*, Kluwer Academic Publishers, 2000, ISBN: 0-7923-8625-6.

[8] Hassan Aboushady, *Design for reuse of current-mode continuous-time sigma-delta analog-to-digital converters*, Ph.D. thesis, University of Paris VI, Dep. Electronics, Communications and Computer Science, January 2002.

[9] R. Mittal and D. J. Allstot, "Low-power high-speed continuous-time sigma-delta modulators," *IEEE ISCAS*, pp. 183–186, 1995.

[10] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS sigma-delta modulator for speech coding with 80 dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1873–1880, December 1996.

[11] L. J. Breems, E. C. Dijkmans, and J. H. Huijsing, "A quadrature data-dependent DEM algorithm to improve image rejection of a complex sigma-delta modulator," *IEEE Journal of solid-state circuits*, vol. 36, no. 12, pp. 1879–1886, December 2001.

[12] R. Schreier, "Quadrature mismatch shaping," *IEEE International symposium on circuits and systems*, vol. 4, pp. 675–678, 2002.

[13] Y. Palaskas, Y. Tsividis, V. Prodanov, and V. Boccuzzi, "A 'divide and conquer' technique for implementing wide dynamic range continuous-time filters," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 297–307, February 2004.