A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers

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***Abstract*—We present an experimental continuous-time complex delta-sigma multi-bit modulator, implemented in standard 0.25-μm CMOS technology and meeting all major requirements for application in IEEE 802.11a/b/g wireless LAN receivers. The clock frequency is 320 MHz, producing an oversampling ratio of 16 for 20 MHz channel bandwidths. The modulator supports two operation modes for zero-IF and low-IF receiver architectures respectively, requires a single 2.5-V power supply, and dissipates only 32 mW of power. The measured peak signal-to-noise ratio is 55 dB. Further experimental results using sine-wave and OFDM test signals are also presented.**

***Index Terms*—Analog-to-digital conversion, sigma-delta modulation, wireless LAN.**

I. Introduction

WIRELESS-LANs based on the IEEE 802.11 standard achieve high data rates through the use of wide channel bandwidths and efficient modulation techniques such as CCK and OFDM (802.11a/b/g standards). The economic drive for low cost and low power mandates the use of highly integrated transceivers based on zero-IF (ZIF) or low-IF (LIF) architectures. The former are well suited for 802.11b applications since the CCK modulation allows AC baseband coupling, thus eliminating any signal-related DC offsets. For 802.11a/g OFDM applications where baseband AC coupling is very difficult, LIF receivers at 10 MHz are better suited, especially since the adjacent channel rejection specifications are relaxed. Therefore, in multi-mode 802.11a/b/g applications, it is beneficial to use a single ADC block to digitize either an I/Q-pair of real signals for CCK or a single 10-MHz-centered LIF signal for OFDM.

The high dynamic range of 802.11a/g OFDM enforces fundamental limitations on the minimum power dissipation achievable. For example, a substantial power penalty is paid when using typical Nyquist-rate ADCs preceded by high-order, high dynamic range fully integrated channel filters. A better design for low power would be to employ over-sampled A/D conversion preceded by low-order channel filters [1]. Furthermore, this approach would yield superior I/Q-balance properties over the channel bandwidth. In order to prove the feasibility of such an attractive architecture, it is necessary to first demonstrate a low-power $\Delta\Sigma$ ADC meeting the 802.11 requirements.

Single-bit $\Delta\Sigma$ ADCs are widely used in low-speed applications, such as audio, where a very high oversampling ratio (OSR) with respect to the input signal bandwidth is easily attainable. In the case of 802.11a/g wireless-LAN receivers where the channel bandwidth is 20 MHz, a similar frequency-scaled design would result in gigahertz clock frequencies. This operating speed is too fast and not practical for currently available CMOS technology. In addition, the classical $\Delta\Sigma$ ADCs are built as discrete-time circuits with switched-capacitor integrators. Discrete-time circuits require operational amplifiers with gain-bandwidth products about 2 to 10 times the clock frequency (depending on the closed-loop gain of each particular integrator) which would lead to high power consumption and noise.

In order to realize a practical $\Delta\Sigma$ ADC for 802.11, two changes are applied with respect to conventional topologies. First, a multi-bit quantizer is used instead of the widely popular single-bit design. This achieves a reasonably high signal-to-noise ratio (SNR) with a low OSR [1]. The alternative possibility for increased SNR, i.e., employing a high-order loop filter, would result in potential stability problems and high sensitivity to coefficient variations. The inherent DAC nonlinear characteristic, which is the main drawback of multi-bit quantizers, can be compensated using dynamic element matching techniques [2], [3]. Second, the loop-filter of the ADC is implemented as a continuous-time (CT) circuit. In this way, the bandwidth and power requirements for this block are minimized even at high sampling clock frequencies [4]–[6].

Recently, CT $\Delta\Sigma$ ADC designs in CMOS have grown in popularity. Their low-power potential for medium/high (10–15 bits) resolution and narrow bandwidth (1–2 MHz) has been proven by several successful designs [7]–[10]. Furthermore, recent CT $\Delta\Sigma$ ADCs have also targeted wideband (10–20 MHz) 10–13-bit resolution applications [11]–[13]. These are attractive since equivalent switched-capacitor implementations pose great challenges on the circuit design and require power-hungry opamps [14].

The ZIF and LIF receivers perform RF to IF conversion by generating an in-phase IF component called I and a quadrature IF component called Q. These components, which are necessary to carry the desired channel information and remove the RF image (image rejection) can be mathematically represented

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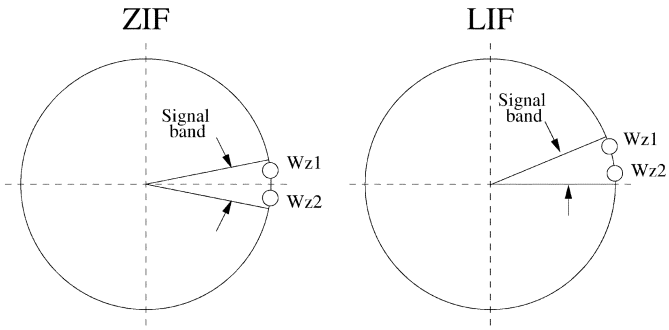


Fig. 1. Location of the NTF zeros in the Z-domain for the ZIF and LIF modes. The signal bandwidth is 20 MHz.

as the real and imaginary parts of a complex IF signal. The digitization of this complex IF signal requires a complex ADC, which in the case of ZIF may be just a pair of two real conventional ADCs. However, for LIF the use of two real ADCs would double the clock frequency and the digitizing bandwidth. This must be done to capture the IF signal but it wastes power since it is not necessary to digitize the negative frequencies where the adjacent channel resides and there is no desired channel energy. A complex $\Delta\Sigma$ ADC with a signal band that includes only the positive frequencies can be designed using two conventional $\Delta\Sigma$ ADCs clocked like in the ZIF case complemented with proper cross-coupling elements [15]. This topology yields a complex noise transfer function (NTF) shifted toward the positive frequencies, centered at 10 MHz and having a bandwidth of 20 MHz. The power dissipation of this complex ADC is not substantially higher than that of a dual real ADC for ZIF because the cross-coupling elements have a small contribution to the total power budget.

In this paper, we report the first complex, continuous-time $\Delta\Sigma$ ADC designed for IEEE 802.11a/b/g wireless LANs. The proposed complex CT $\Delta\Sigma$ ADC has the lowest power consumption (32 mW for complex operation, 15 mW for single real ADC) and smallest active chip area (0.44 mm^2) within the medium resolution (10 bit) and wide bandwidth (10–20 MHz) state-of-the art $\Delta\Sigma$ ADCs [11]–[14]. The low power consumption is achieved by choosing a simple second-order 3-bit modulator, by employing low-noise and high-linearity *Gm-C* integrators in the loop filter, and by judicious analog design.

The structure of the modulator and the circuit implementation are shown in Sections II and III, respectively. Experimental results, using both sine-wave and OFDM inputs, are presented and discussed in Section IV. Conclusions are summarized in Section V.

II. Complex $\Delta\Sigma$ Modulator Design

A. Architecture Selection

The design's peak SNR target was set to 60 dB, to allow 5 dB margin above the required 55 dB. In order to achieve this SNR with an OSR of only 16, a second-order, multi-bit $\Delta\Sigma$ modulator with a 3-bit quantizer and zero-optimized NTF [16] was chosen. We started with a NTF for a discrete-time $\Delta\Sigma$ modulator and mapped it to a CT modulator. In Fig. 1, the location of the zeros of the discrete-time modulator NTF is shown for both

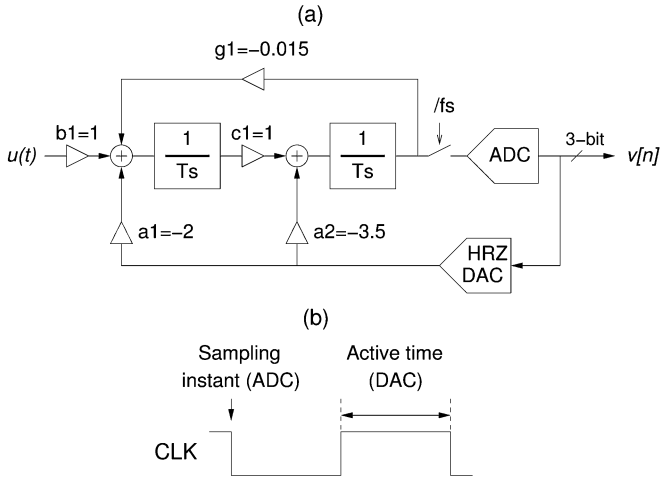


Fig. 2. (a) Diagram of the second-order, continuous-time, multibit, real modulator and (b) Timing.

the zero-IF mode (ZIF mode) and low-IF mode (LIF mode). In both cases, the NTF can be written as

$$\mathrm{NTF}(z) = z^{-2}(z - W_{Z1}) \cdot (z - W_{Z2}) \tag{1}$$

where W_{Z1} and W_{Z2} are the zeros for the selected mode (ZIF or LIF).

As mentioned before, the ZIF mode is intended for direct-conversion receivers, where the signal band is centered at DC. Therefore, the two NTF zeros are complex conjugate, and then the modulator can be built with two isolated real modulators, each having the following NTF:

$$\mathrm{NTF}(z) = 1 - 1.98792z^{-1} + z^{-2}. \tag{2}$$

In the LIF mode, the NTF shows a frequency shift toward positive frequencies (+10 MHz). The two zeros are no longer complex conjugate, and the resulting NTF has complex coefficients implemented as a coupling between the I and Q modulators. The corresponding zero values are

$$\begin{aligned} W_{Z1} &= (0.9534 + j0.3015) \\ W_{Z2} &= (0.9963 + j0.0863). \end{aligned} \tag{3}$$

B. CT Modulator Implementation

The realization of the ZIF/LIF complex modulator began with the design of a real CT modulator, which would be used in a pair of two identical blocks for ZIF mode. The block diagram of this circuit is shown in Fig. 2(a). The coefficients were obtained by mapping the NTF of the CT modulator to (2). The modified Z-transform [17] was used taking into account the timing of the half-return-to-zero (HRZ) DAC waveform.

The ADC in Fig. 2(a) samples its input on the falling edge of the clock, but its output signal is not needed in the closed-loop system until the second half of the clock cycle due to the HRZ waveform [Fig. 2(b)]. In this way, the ADC has half a cycle to perform the analog-to-digital conversion. The effect of the ADC comparator metastability on modulator performance is reduced [6]. The DAC is turned on and off on each cycle providing a half-delayed, return-to-zero signal. Modulators using return-to-

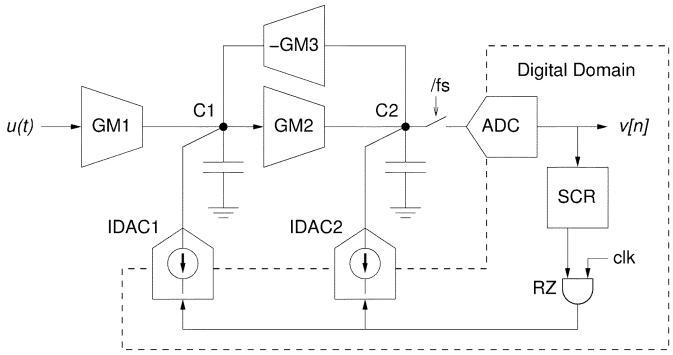


Fig. 3. Block diagram of a *Gm-C* implementation of the real modulator.

zero signals exhibit less performance degradation due to turn-on/turn-off transients of the DAC because these transients do not depend on previous output data [4], [5]. However, they exhibit higher clock jitter sensitivity.

The coefficients shown in the modulator of Fig. 2(a) realize the correct NTF but do not provide optimum dynamic range. Scaling may be applied to adjust the amplitude distribution of the two integrators to proper values without changing the NTF. Such scaling was done taking into account the input range of the transconductors used in the integrators ($\pm$500 mV).

The CT integrators of Fig. 2(a) are implemented as transconductors loaded with capacitors, resulting in the schematic of Fig. 3. Note that while this schematic shows a single-ended circuit for clarity, the actual modulator was built using fully differential circuits.

As can be seen in Fig. 3, the sampling operation occurs only at the ADC input, while the loop filter is a CT circuit providing implicit aliasing rejection for this type of modulator [6]. The DAC of Fig. 2(a) is replaced by two current-output DACs, implemented as arrays of identical, switched current sources controlled by a thermometer-code digital input. Multi-bit modulators are sensitive to DAC nonlinearity. In order to reduce this effect, a scrambler, SCR, is added between the ADC output and the DAC inputs. This circuit improves the linearity of the DACs by selecting a different set of DAC elements on each sample, thus performing dynamic element matching. A data weighted averaging algorithm (DWA) [2] was chosen for the scrambler due to its simplicity and because system level simulations show that this algorithm is good enough to remove the effects of DAC element mismatches as high as 2% or even more. Quadrature DEM algorithms have been proposed in order to improve the image rejection of complex $\Delta\Sigma$ ADCs [18], [19]. However, these algorithms cannot correct the mismatch between I and Q channels of the entire complex modulator. In this case, such mismatches can be as high as those of the DAC elements. In our design, a simpler, independent scrambler is used for each real modulator and image rejection accuracy is obtained through proper layout techniques. The layout of the elements in the I and Q channels, including the DAC elements, the capacitor units, the transconductors, and the resistors of the ADCs, were interlaced and laid out following a common-centroid topology.

Two real modulators can be combined into a single complex modulator as can be seen in Fig. 4. Without the cross-coupling

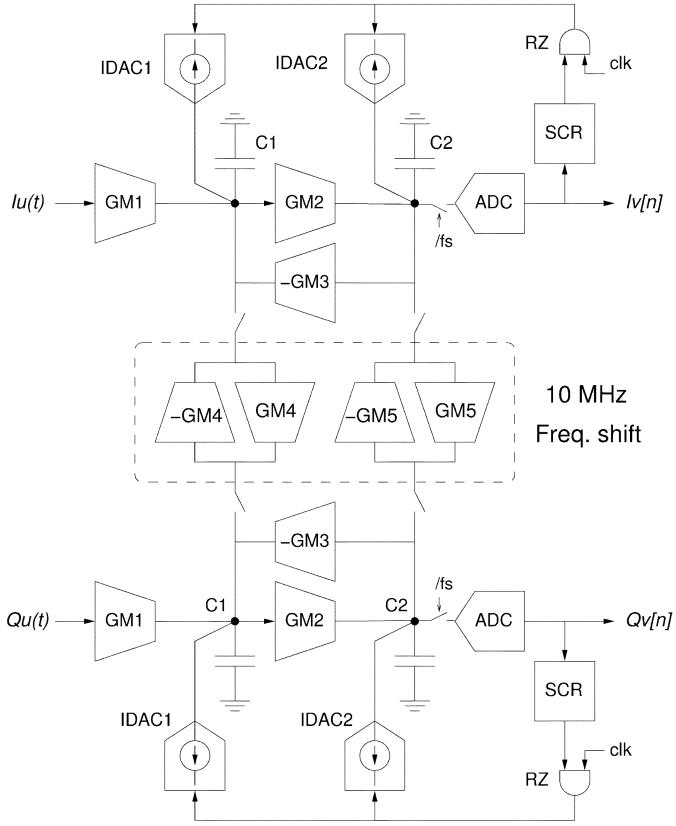


Fig. 4. Complex modulator schematic.

transconductors, each real modulator works independently and the resulting NTF of the complex modulator is centered around DC [Fig. 5(a), ZIF mode]. If transconductors GM_4 and GM_5 are enabled, a $+10$ MHz frequency shift is obtained [Fig. 5(b), LIF mode] . Therefore, by enabling the coupling transconductors we can change from a modulator for zero-IF receivers (ZIF mode) to a modulator for low-IF receivers (LIF mode). The optimum modulator mode can be selected dynamically in a multimode receiver based on this ADC.

C. Impact of Nonideal Effects on Performance

The modulator architecture was verified using a behavioral-level simulator, including nonideal effects such as nonlinear transconductors, integrators with finite DC gain and a nondominant pole, mismatches, thermal noise, and clock jitter. Some of these nonideal effects have been included in the simulated spectra of Fig. 5. The modulator showed low sensitivity to process variation, allowing for higher than 20% relative variations in the main modulator elements, namely, transconductors, capacitors, and DACs. The assumed relative mismatch was estimated at 1%, resulting in no significant SNR loss when the scramblers are active, and in an approximately 35 dB image rejection. Experimental results show that this mismatch estimation was pessimistic (see Section IV).

CT modulators are known to be sensitive to clock jitter because the inaccuracies of the clock signal are translated into a charge error at the output of the DACs [6]. If the clock jitter is the only source of noise present, and if only the jitter of the first

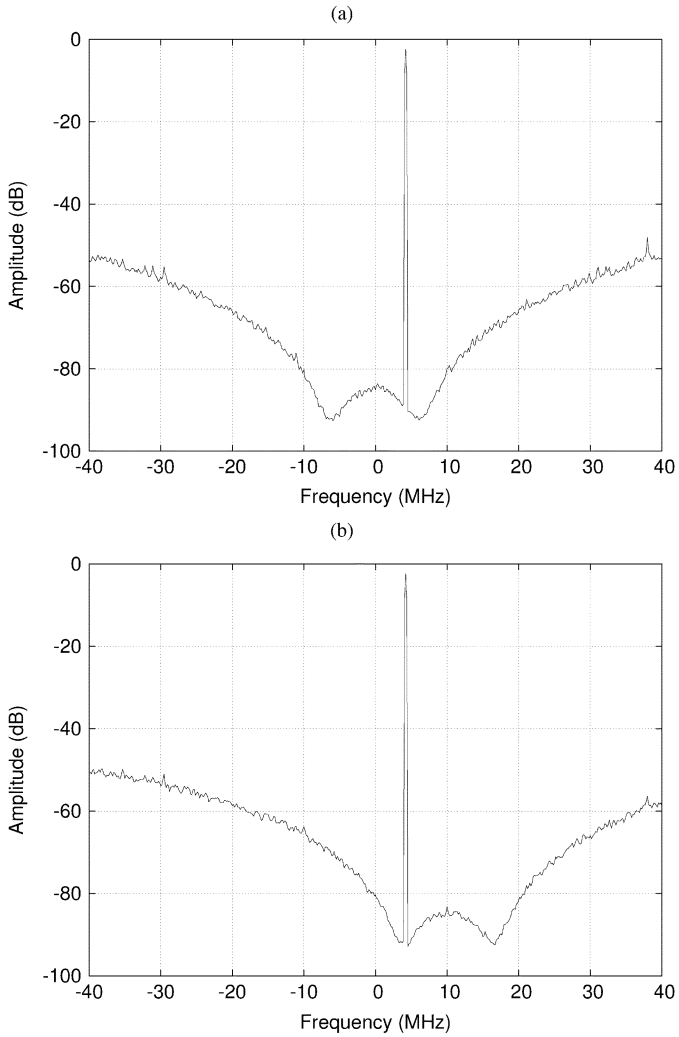


Fig. 5. Simulated spectra for (a) ZIF mode. (b) LIF mode. Simulations were done using a behavioral ADC model including finite DC gain, an integrator nondominant pole, and thermal noise. Clock jitter is not included in order to keep the NTF notches clearly visible. A 4.3 MHz complex test tone has been applied to the inputs.

DAC is considered (the following DAC noise is shaped and can be neglected), the expected SNR for the modulator of Fig. 2 is

$$\mathrm{SNR(dB)} = 10 \cdot \log_{10}\left(\frac{\mathrm{OSR}}{32\dfrac{\sigma^2_{\mathrm{jitter}}}{T^2}}\right) \tag{4}$$

where σ_{jitter} is the standard deviation of the clock period (jitter) and T the nominal clock period (3.125 ns). Therefore, a clock signal with a jitter level better than 4 ps is required ($\sigma/T < 0.12\%$) in order to avoid a significant performance degradation.

III. Circuit Implementation

The modulator was implemented in a standard 0.25-μm 4-metal layer CMOS technology using only core transistors. It operates with a supply voltage of 2.5 V and at a clock frequency of 320 MHz. The input signals are differential with a full-scale range of $\pm$500 mV peak ($-$9 dBVrms). The functional blocks of the modulator are described next.

TABLE I
Nominal Transconductance and Capacitor Sizes

Component	Value
GM_1	1000μA/V
GM_2	200 μA/V
GM_3	15 μA/V
GM_4	325 μA/V
GM_5	24 μA/V
C_1	5.165 pF
C_2	0.376 pF

A. Gm-C Integrators

The integrators were built using transconductors and capacitors (*Gm-C*). This approach had the advantage of a simpler circuit structure and lower power consumption than other approaches, such as those based on operational amplifiers. In this case, the specifications for resolution and linearity are not overly demanding and allow the use of the *Gm-C* approach.

The nominal transconductor and capacitor values are listed in Table I. The size of GM_1, C_1, GM_2 and C_2 were determined taking into account the contribution of thermal noise to the total ADC noise, and by making this noise nondominant (about -6 dB below quantization noise) to avoid the degradation of the effective resolution of the converter. If the thermal noise is made much lower than the quantization noise, there will be a noticeable increase in power consumption. Therefore, there is a trade-off between resolution and power consumption. In this case, the resolution penalty due to thermal noise is about 1 dB.

GM_3 was obtained from the frequency of the optimized zero of the NTF, ω_{oz} [16]

$$GM_3 = \frac{\omega_{oz}^2}{GM_2 C_1 C_2} \tag{5}$$

and GM_4 and GM_5 were obtained from the frequency shift of the complex modulator ($\omega_{\mathrm{sh}} = 2\pi \cdot 10$ MHz)

$$GM_4 = \omega_{\mathrm{sh}} C_1 \quad GM_5 = \omega_{\mathrm{sh}} C_2. \tag{6}$$

The transconductor schematics are shown in Fig. 6. Note that GM_3 has a different, simpler, structure than the other circuit due to its small transconductance [Fig. 6(b)]. The structure of Fig. 6(a) was described in [20]. It is a low-noise, highly linear transconductor whose normalized transconductance is shown in Fig. 7. In the -0.5 to $+0.5$ voltage range, the ripples of the transconductance are only about 1%, providing a low distortion for the modulator. This is particularly significant for the input transconductors, because their distortion is unshaped by the loop filter. Transconductor GM_3 is implemented using MOSFETs operating in triode region. This transconductor also exhibits good linearity, although it is not highly power-efficient (lower transconductance than the transconductors of Fig. 6(a) for the same current consumption). However, the use of these transconductors does not have a noticeable impact on the total power consumption due to their small value.

Capacitors were implemented as inversion MOS capacitors. These are, in fact, N-channel MOSFET transistors with grounded source and drain terminals, and therefore neither special cells nor special technology options are required. In

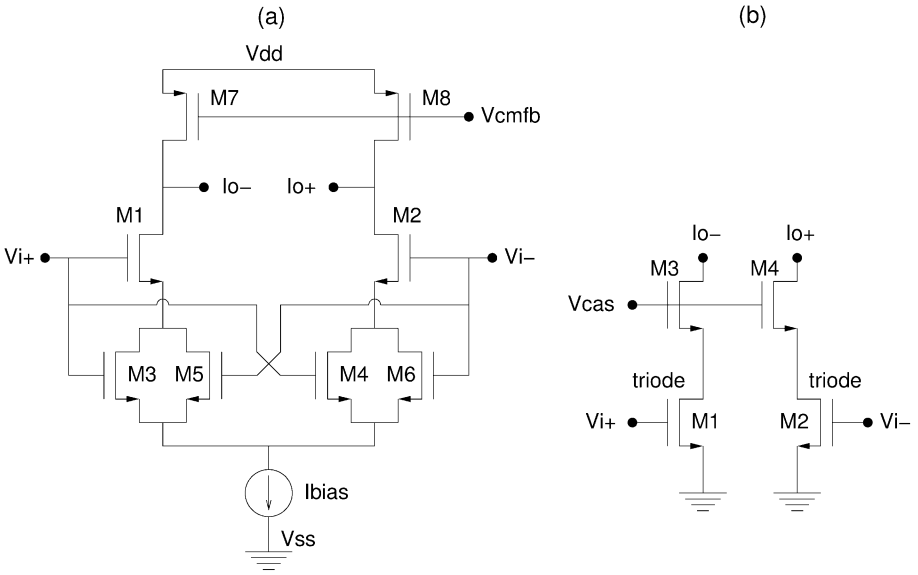


Fig. 6. Schematic of transconductors: (a) GM_1, GM_2, GM_4 and GM_5. (b) GM_3.

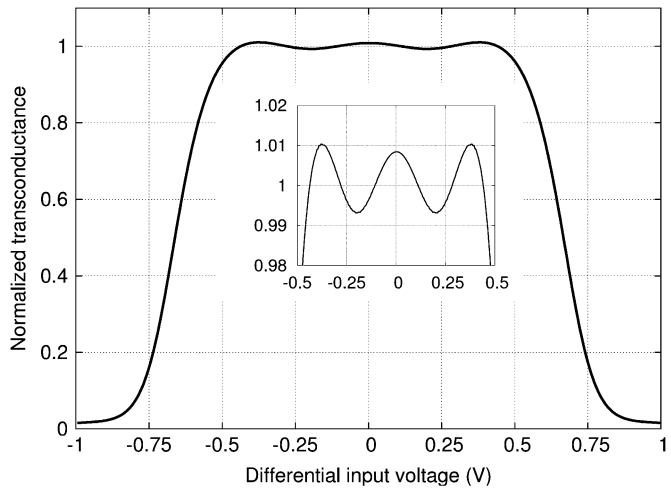


Fig. 7. Normalized transconductance for transconductors GM_1, GM_2, GM_4, and GM_5. A zoom of the upper part of the curve is shown in the inset.

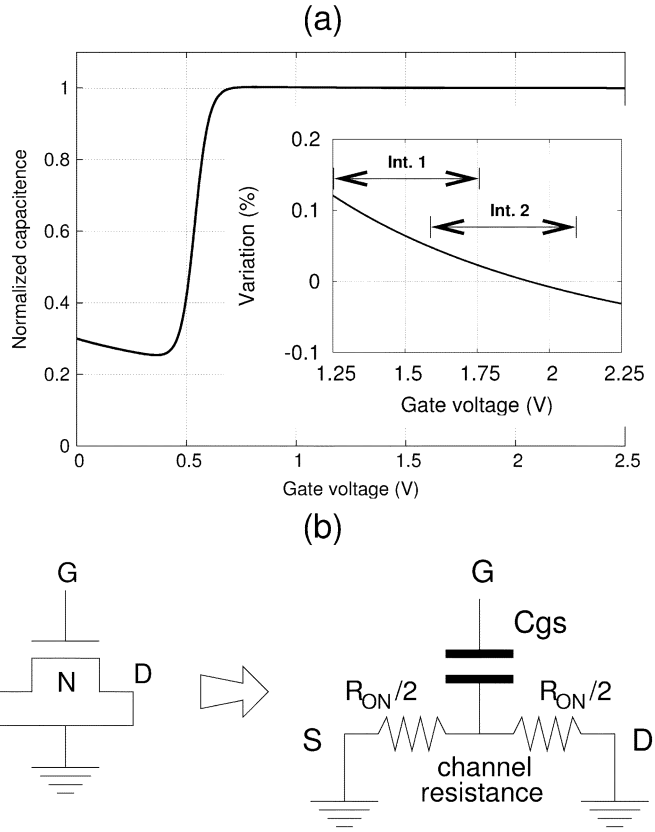


Fig. 8. MOS capacitors. (a) Capacitance versus voltage. The normalized capacitance variation along with the output voltage range of the two integrators is shown in the inset. (b) Equivalent model of the MOS capacitor.

addition, the high capacitance density of MOS capacitors reduces the chip area. The corresponding capacitance-voltage curve is included in Fig. 8(a) along with the output voltage ranges of the two integrators. As can be seen, the variation of the capacitance for the intended ranges is quite small, about 0.1%. This distortion introduced by the nonlinear capacitance is masked by the distortion of the transconductors. In Fig. 8(b), the equivalent circuit of the capacitor is shown. The series resistance of the capacitor, R_S, depends on the common-mode voltage at the output of the integrator. Its value is

$$R_S \simeq \frac{R_{\rm ON}}{4} = \frac{1}{4K_p\frac{W}{L}(V_{\rm CM} - V_{\rm TH})} \tag{7}$$

where $V_{\rm CM}$ is the common-mode voltage at the integrator output, $V_{\rm TH}$ is the threshold voltage for N-channel devices, and W and L are the width and length of the capacitor's gate. This resistance introduces a zero in the transfer function of integrators and it can change the NTF of the modulator significantly. In order to reduce this effect, the capacitors have to be split into small sections connected in parallel. In this way, the total series resistance is divided by the number of sections (if the capacitor aspect-ratio is kept constant).

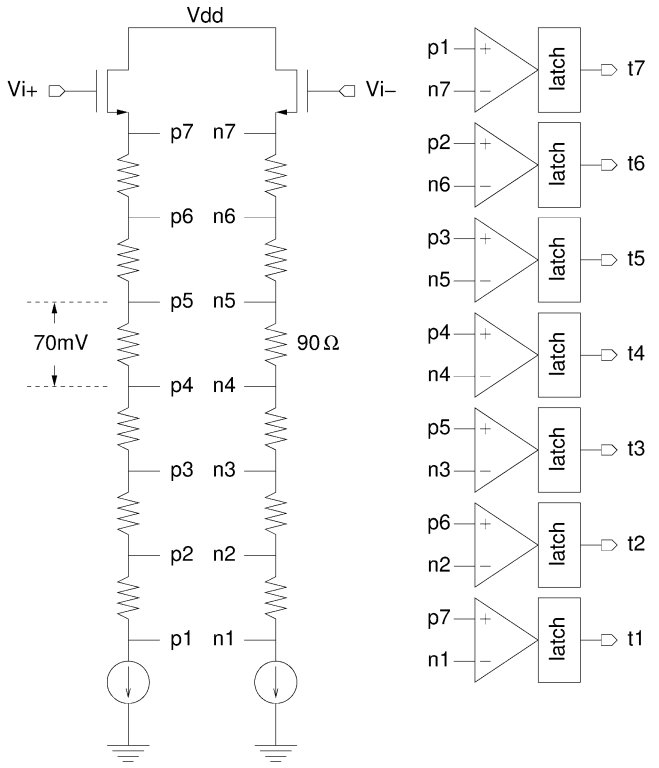


Fig. 9. Schematic of the differential-input 3-bit flash ADC.

B. Flash ADC

The flash ADC schematic is shown in Fig. 9. It consists of a differential input buffer, a voltage shifter based on two resistor strings, and seven regenerative comparators and latches. The resistor strings are biased by a constant current providing a 70-mV voltage drop between consecutive taps. The value of resistors, 90 Ω, was chosen to give fast settling during the ADC's track phase.

The comparator schematic is shown in Fig. 10(a). It consists of a pair of input switches, a full-swing latch and two C^2MOS dynamic latches. The corresponding timing is shown in Fig. 10(b). The comparator can operate in two different phases: when CLK is high, the input switches are on and internal nodes track the input voltage. Then, when CLK changes to low, the input switches turn off, sampling the input voltage, and the latch is connected to power busses. A strong positive feedback leads it to regeneration. Thus, the initial voltage difference increases exponentially until it reaches the power supply values. During the next track phase, the previous output data is held in the output latch. This latch uses a delayed clock signal to avoid disturbing regeneration at its beginning and thus reduces the effect of kick-back noise. The time-constant of the comparator is about 50 ps, and the corresponding metastability probability is one cycle every $2 \cdot 10^{10}$ cycles. The estimated offset is 8 mV.

C. Current-Mode DACS

Current-output DACs (Fig. 11) were built using eight identical current cells controlled by a thermometer-code input. Each cell is a cascode current source followed by three current-steering switches. Switches controlled by esn and esp

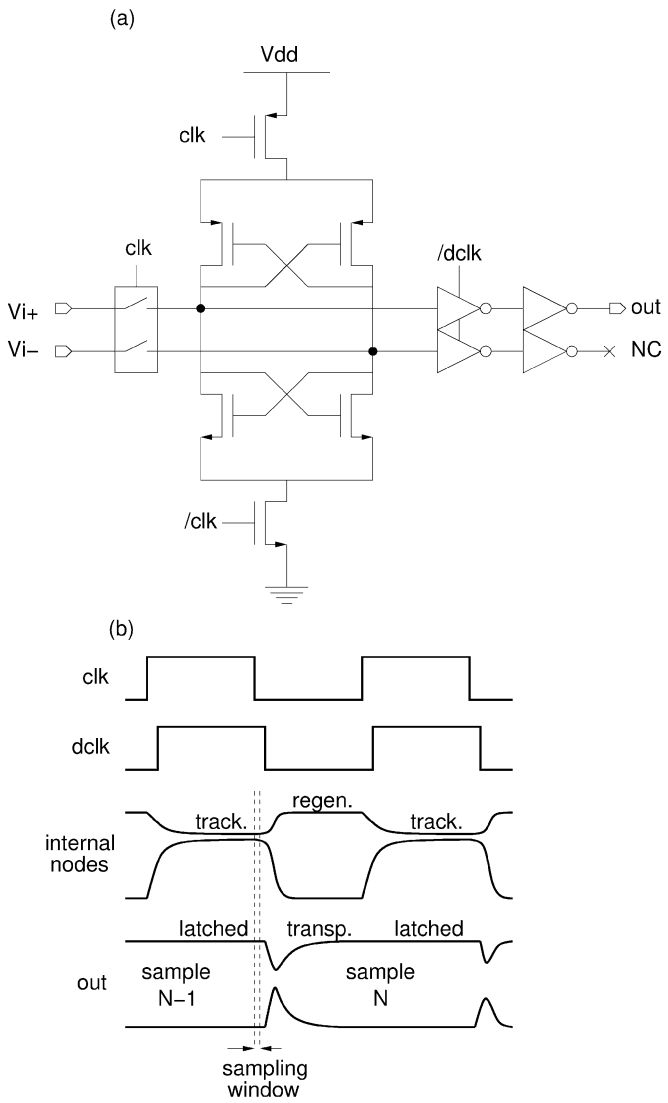


Fig. 10. (a) Schematic of comparators and latches. (b) Timing diagram.

steer the current toward the positive or negative output bus depending on the input data (these signals are generated by the digital logic discussed in the following subsection). These switches can only be on during half of the clock period (HRZ DAC) as can be seen in Fig. 11. When esp and esn are both off, the third switch, whose gate is connected to a constant reference voltage, $V_{\rm ref}$, remains on, avoiding transients on the current source devices that are always working in saturation. This results in some power consumption penalty. However, this extra power consumption was estimated at only about 10% of the total modulator power consumption. In this off state, four cells are connected to the positive output node and four cells to the negative output one, resulting in a zero differential output current.

Since the DACs are built using only N-channel devices, they can only sink current and this has to be compensated by a proper constant current biasing implemented with P-channel devices (not shown).

The mismatch between current cells was minimized using a common-centroid layout for DACs. Also, I and Q channel DAC cells are interlaced to improve image rejection. The effect

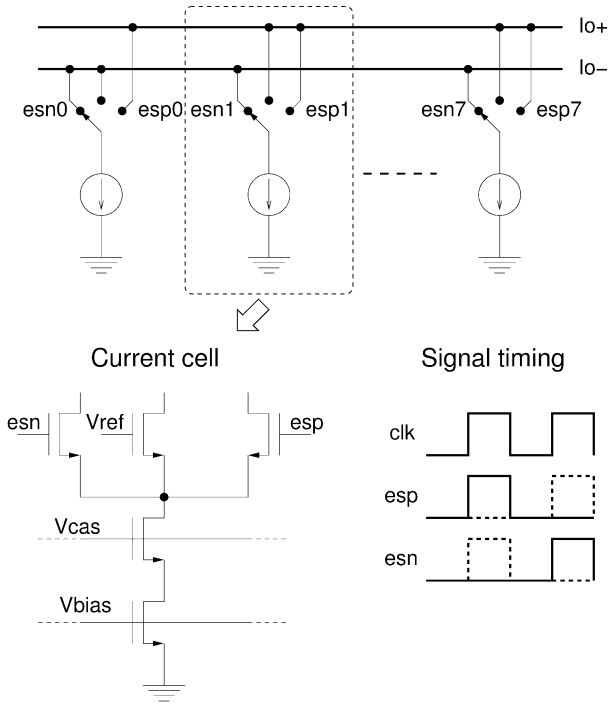


Fig. 11. Schematic of current-output DACs and related signal timing.

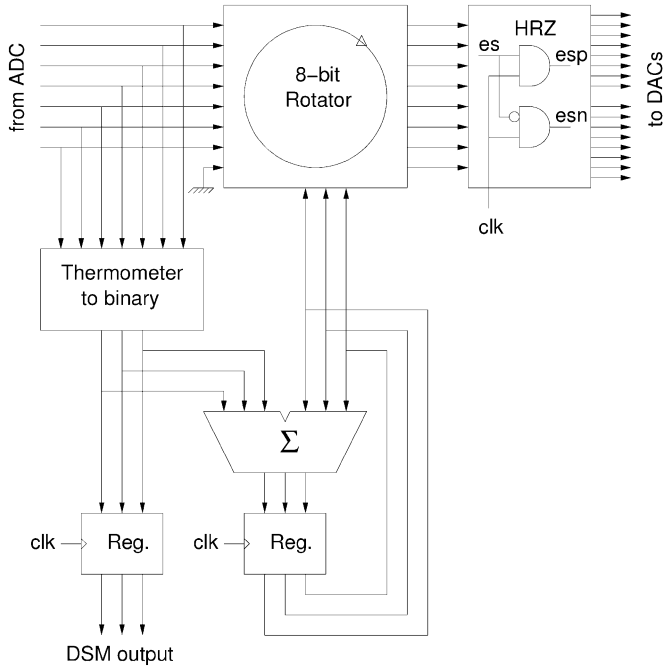


Fig. 12. Block diagram of the digital logic of a real modulator.

of these mismatches is further reduced by the DWA algorithm whose implementation is presented in the next subsection.

D. Digital Logic

Certain parts of the modulator are implemented in the digital domain. The digital logic diagram is shown in Fig. 12. It includes a thermometer-to-binary-code converter, an 8-bit combinatorial rotator and the associated DWA logic, and the HRZ logic. The DWA algorithm is based on the rotation of the thermometer-code output with a rotation index that is incremented

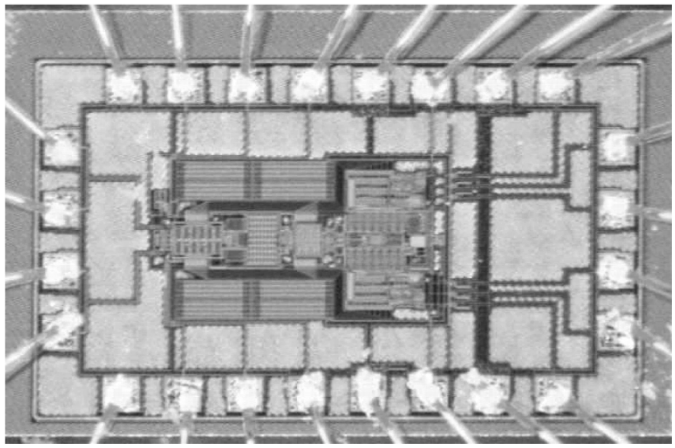


Fig. 13. Photograph of the test chip bonded to a PCB.

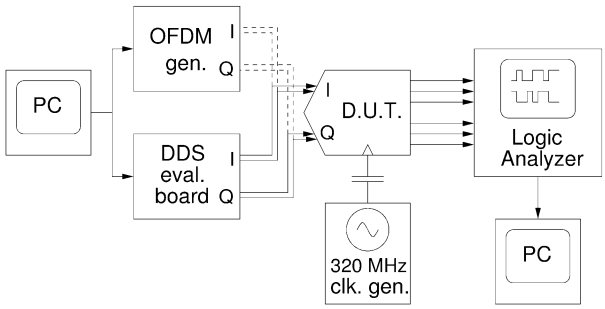


Fig. 14. Experimental setup for measurements.

by the value of the modulator output on each sample. In this way, the nonlinearity of DACs is translated into a first-order shaped noise floor owing to the element scrambling. The HRZ logic generates the signals to drive the DAC inputs.

IV. Experimental Results

The converter was fabricated and a test chip was bonded to a PCB using a room-temperature conductive glue; the chip photograph is shown in Fig. 13. The chip area is 1480×880 μm^2 including pads. Without pads, the active area is reduced by 2/3. The chip was powered by three separate power supplies, all operating at 2.5 V. A power supply was provided for analog circuitry, another power supply was used for digital circuitry, and the third power supply was used only for output pin drivers. The power consumption, not including pin drivers, was 30.4 mW for the modulator operating in the ZIF mode and 32 mW for LIF mode. This small difference is due to the coupling transconductors (Fig. 4) that are disabled in the ZIF mode. The power consumption of the digital blocks was 12 mW in both modes, and the power consumption of the pin drivers was about 10 mW. This latter figure is highly dependent on the load capacitance.

The experimental setup for measurements is shown in Fig. 14. The input is a complex differential signal obtained either from a direct digital synthesizer (DDS) or from a programmable vector signal generator, capable of generating OFDM signals. The clock signal is obtained from a 320-MHz sine-wave RF generator. The output bits are acquired by a high-speed logic analyzer and then transferred to a computer for further processing.

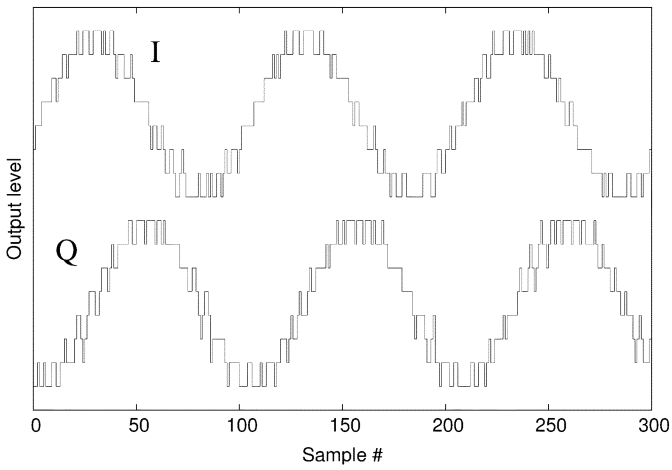


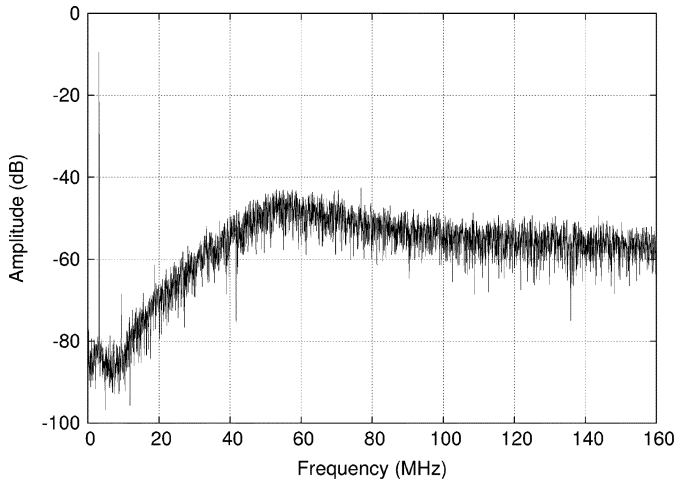
Fig. 15. Time-domain output for a complex, +3.125-MHz full-scale sine-wave input. (The waveforms are shifted on the Y-axis for the sake of clarity).

A. Sine-Wave Based Measurements

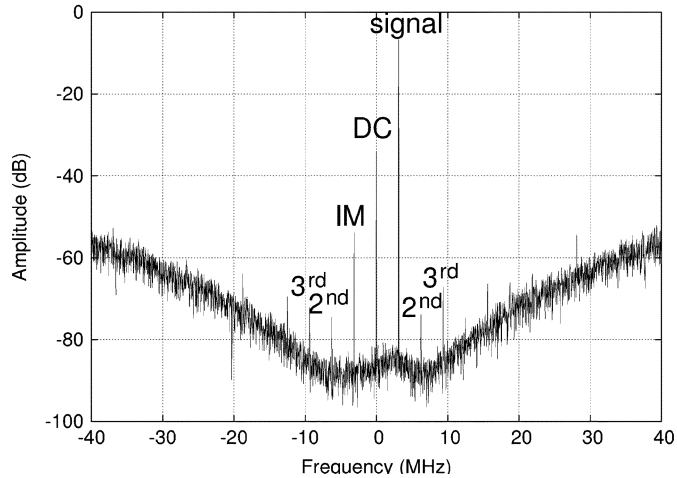
A set of measurements were performed using complex sine-wave input signals. These signals were obtained from an Analog Devices AD9854 DDS evaluation board. To allow for image-rejection measurements, the input signal to the modulator had to be a complex sine-wave with accurate quadrature. The DDS output already provides high phase accuracy, but some calibration was needed in order to cancel the gain imbalance of I and Q outputs. After calibration, the output presents only a positive frequency, with more than 60 dB of image frequency attenuation, 13 dB higher than the measured image rejection of the test chip.

In Fig. 15, an example of the output waveforms is shown. The output sine-wave is distorted by quantization noise, and parameter extraction is difficult. Therefore, the output signal is translated into the frequency domain using FFT.

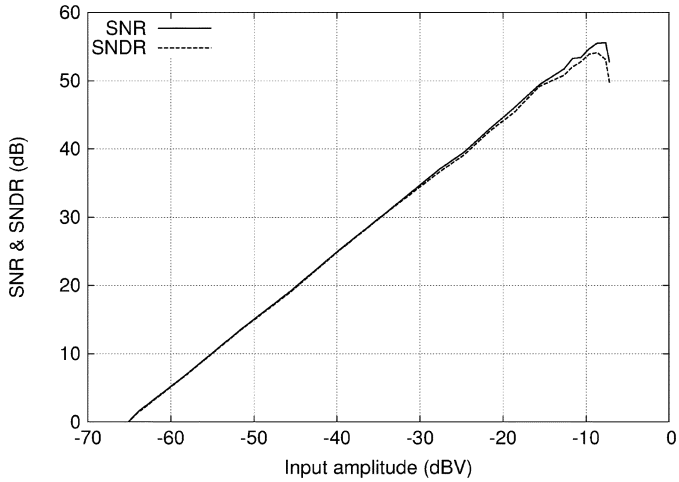
When the cross-coupling transconductors (Fig. 4) are disconnected (ZIF mode), the modulator can be viewed as two independent real, single-input modulators. The corresponding output for these modulators is shown in Fig. 16(a) for a 3.125-MHz −13-dBV single-tone input. When the two modulators are considered as a complex modulator, the corresponding output includes both positive and negative frequencies [Fig. 16(b)]. The noise floor shape follows the designed NTF where the two zeros are still visible, although they are filled with noise due to several nonideal effects including finite integrator gain, thermal noise and clock jitter. In addition to the input test tone, several other tones are present at the output. The observed DC level corresponds to about 10 mV. The image frequency (IM) at −3.125 MHz is 47.2 dB lower than the input signal. This high image rejection is achieved mainly due to the proper layout of the circuit and it is high enough to operate the receiver without any ADC calibration. Several harmonics can also be observed in the output spectrum, but their amplitudes are small. They are mainly originated by the input transconductor, according to simulations using its nonlinear transfer characteristic. The total harmonic distortion (THD) for −13 dBV input is −58 dBc. The measured SNR for this input



(a)



(b)



(c)

Fig. 16. Output spectra for (a) single real modulator, (b) complex ZIF-mode modulator (detail), and (c) SNR and SNDR plots as a function of the input amplitude.

amplitude is 51.8 dB. In Fig. 16(c) the SNR and SNDR of the complex modulator in ZIF mode are plotted as a function of the input amplitude. A peak SNR and SNDR of 55.5 dB and 53.9 dB, respectively, are obtained for an input amplitude of

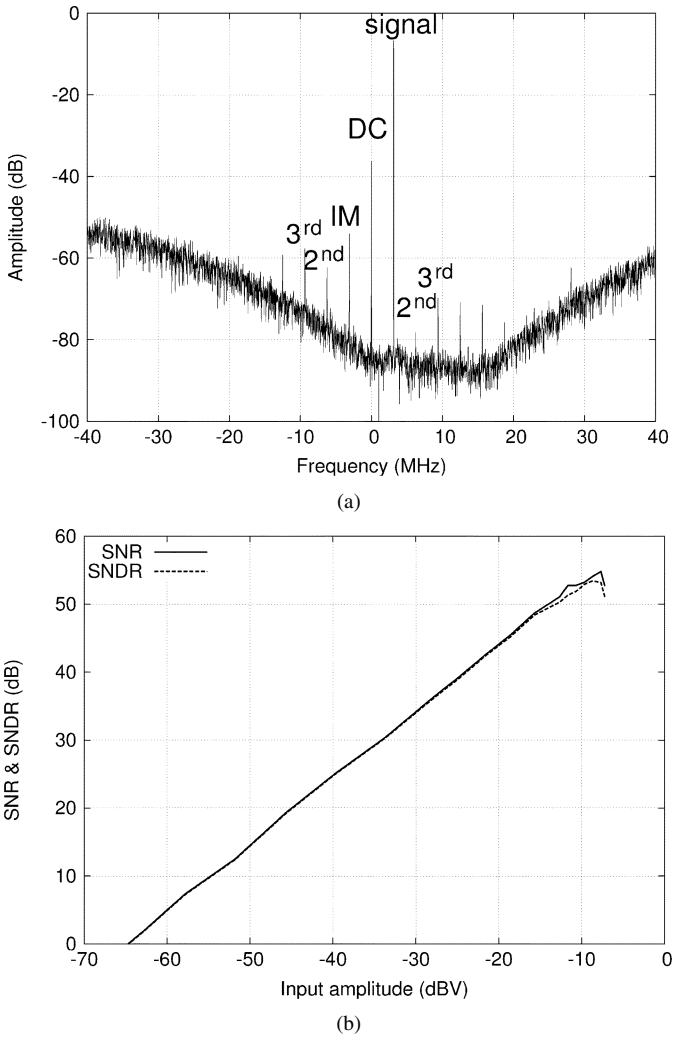


Fig. 17. (a) Output spectrum for complex, LIF mode, modulator (detail), and (b) SNR and SNDR plots as a function of the input amplitude.

−9 dBV. The effect of distortion is small and only noticeable at high input amplitudes.

By enabling the cross-coupling transconductors, the NTF of the modulator is shifted +10 MHz (LIF mode). The output spectrum for an input amplitude of −13 dBV is shown in Fig. 17(a). In this plot, the first NTF minimum is not obvious because of the noise around the input tone, but it is visible for lower input amplitudes. Also, the frequency shift is not exactly 10 MHz due to the inaccurate coupling between the real and imaginary channels of the modulator, but the impact on the ADC performance is not noticeable. The DC component corresponds to 8 mV. The image rejection is the same as for the ZIF mode's 47.2 dB, showing better channel matching than that assumed in simulations. For this amplitude, the THD is −58.3 dBc and the SNR is 51.1 dB. In Fig. 17(b), the SNR and SNDR of the modulator operating in LIF mode is plotted as a function of the input amplitude. The peak values for SNR and SNDR are 54.5 dB and 53.5 dB, respectively, for −9-dBV input amplitude.

The effect of distortion can also be checked using a two-tone test. In Fig. 18 the output spectrum for a two tone input is shown. The input amplitude of each tone was half of that corresponding to the peak SNR value from Fig. 17(b) (i.e., −15 dBV). The

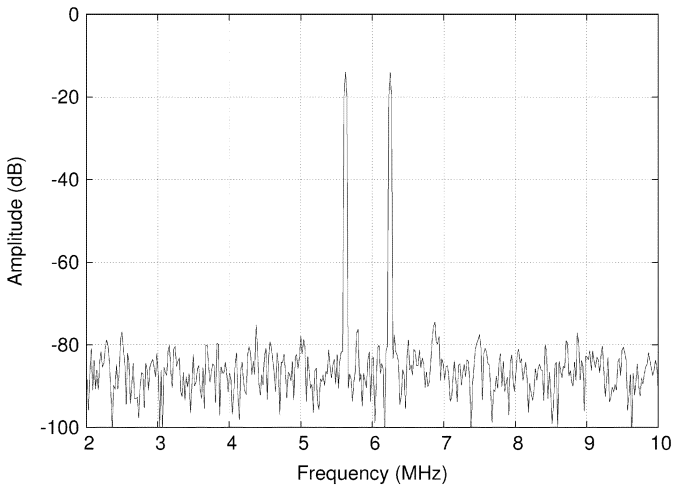


Fig. 18. Intermodulation test. Output spectrum for a two-tone input.

intermodulation products are barely visible, giving a spurious-free dynamic range of more than 60 dB.

The measured SNR and SNDR are less than 1 dB below the results obtained from a transistor-level simulation using the extracted circuit from the chip layout. These simulations did not include thermal noise. Therefore, thermal noise level is not responsible for performance degradation. The observed SNR decrease with respect to that of an ideal modulator can be attributed to the combined effect of several nonidealities such as finite DC gain in integrators, excess loop delay and clock jitter.

B. Clock Jitter Measurements

The observed SNR depends on the clock input amplitude. The clock signal was a sine-wave obtained from an RF generator. This sine-wave is amplified by the input CMOS inverter resulting in an internal clock that is an almost trapezoidal waveform with sharp edges. The input clock has a finite slew-rate, which is proportional to its amplitude. If noise is present at the clock input, it is translated into internal clock jitter that can degrade the SNR.

The jitter generated by noise at the clock input is

$$\sigma_{\text{jitter}} = \frac{T\sigma_v}{2\pi A} \tag{8}$$

where σ_v is the equivalent input voltage noise (rms) and A is the clock signal amplitude. By combining this (8) with (4), and including an additional, uncorrelated, constant source of noise, N, which accounts for quantization noise and all other sources of noise, the following relationship is obtained:

$$\text{SNR(dB)} = -10 \cdot \log_{10}\left[2\left(\frac{\sigma_v^2}{4\pi^2 A^2} + N^2\right)\right]. \tag{9}$$

In Fig. 19, the measured SNR for a single tone input of −13 dBV is plotted as a function of the clock amplitude together with a curve fit to (9). The agreement with experimental data is excellent. This fit gives a value for σ_v of about 6 mV rms, which suggests that the equivalent input noise of the clock is dominated by power supply noise rather than thermal noise. In order to reduce the effect of clock jitter the final clock signal used for

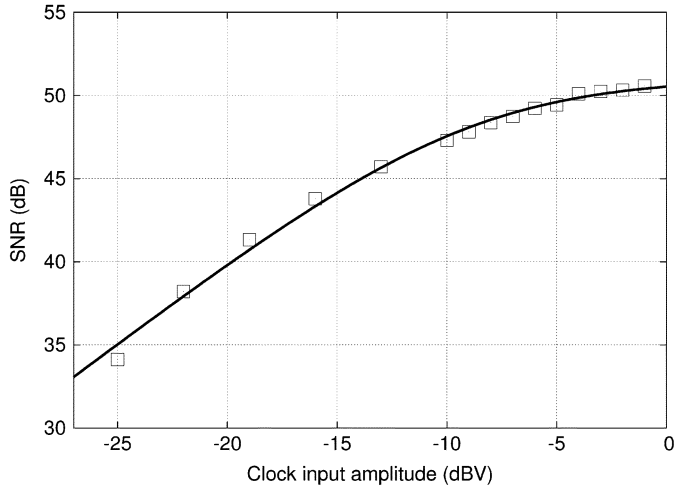
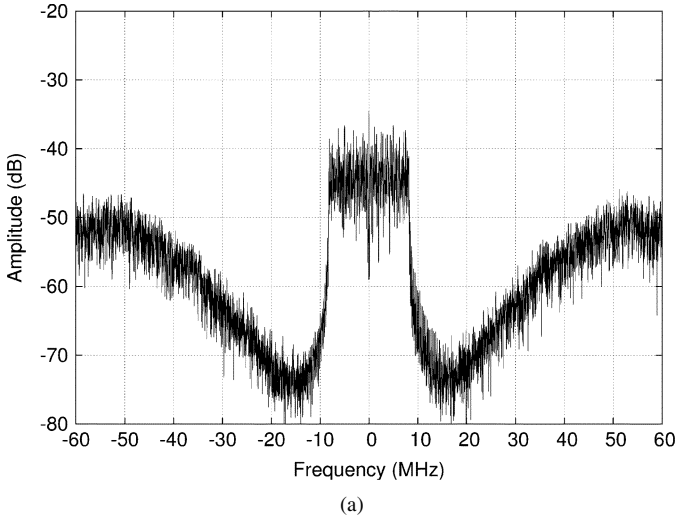
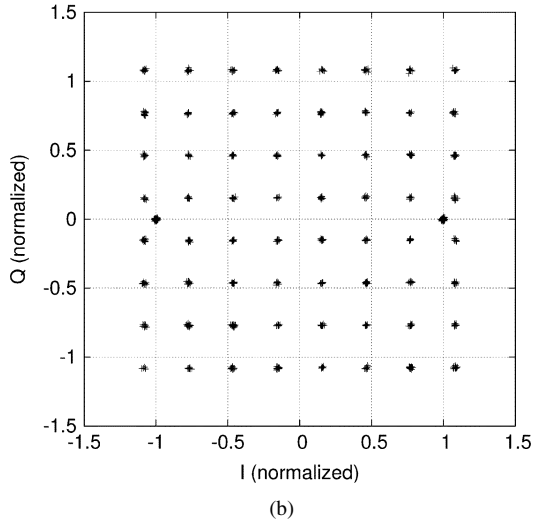


Fig. 19. SNR as a function of the clock amplitude (squares). The clock signal is a sine-wave. Test tone amplitude was −13 dBV. A curve fit to Eq. (9) is included as a solid line.



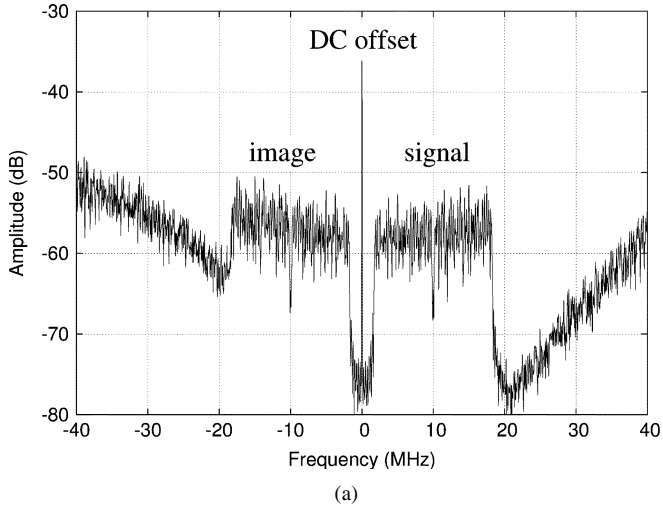
(a)



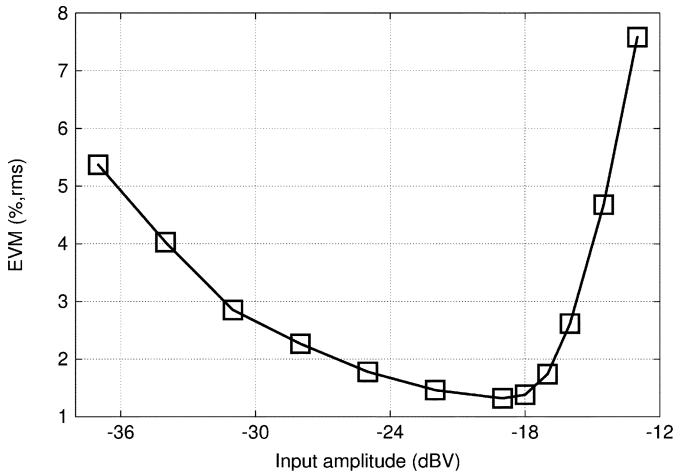
(b)

Fig. 20. (a) Output OFDM spectrum for ZIF mode. (b) Its corresponding constellation.

all measurements was an amplified and clipped sine-wave with sharp edges, giving an estimate for jitter of $\sigma_{\text{jitter}} = 0.75$ ps ($\sigma_{\text{jitter}}/T = 0.024\%$ rms).



(a)



(b)

Fig. 21. (a) Output spectrum for LIF mode. The input signal is a real OFDM signal modulated at 10 MHz and with −37 dBV amplitude. (b) EVM as a function of the input amplitude for LIF mode.

C. OFDM Based Measurements

A set of measurements were carried out using modulated OFDM signals in order to test the performance of the modulator for the intended application. In Fig. 20(a), the spectrum of a converted baseband OFDM signal is shown with the modulator working in ZIF mode. After demodulating the converted signal, the corresponding constellation of Fig. 20(b) is obtained. The error vector magnitude (EVM) for all subcarriers is about 1% rms, well below the maximum 5.6% required for an error-free reception [21].

Similar measurements were done for the LIF mode. In this case, the OFDM signal was modulated with a center frequency of +10 MHz. The signal generator available provided a single RF output, which was connected to the I-channel input of the ADC, while the Q-channel input was grounded. This experimental setup reduced the peak SNR by 3 dB with respect to an ADC with a complex input. Moreover, the negative frequencies are also present at the input reducing further the available dynamic range for the desired signal band. The measured spectrum is shown in Fig. 21(a). The image band has to be rejected by digital filtering using a complex decimator/filter. Alternatively, a −10 MHz frequency shift (mixing) may be performed prior

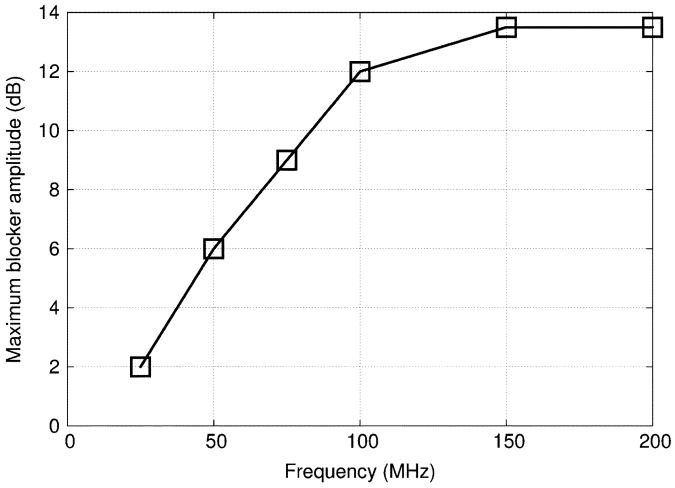


Fig. 22. Maximum allowed out-of-band blocker amplitude, relative to signal, for different frequencies and for LIF mode. Input amplitude: −19 dBV.

to filtering, and then, a conventional decimator/filter would suffice. By computing the corresponding constellation for different input amplitudes, and extracting the EVM, the plot of Fig. 21(b) was obtained. The minimum EVM value is about 1.3% for an input amplitude of −19 dBV.

Finally, an out-of-band, sine-wave interferer (blocker) was added to the 10 MHz-modulated OFDM signal. The amplitude of this blocker was adjusted to obtain an EVM of 3%. The maximum blocker amplitude relative to the signal amplitude is plotted for several frequencies in Fig. 22. For frequencies far away from the signal band, maximum amplitudes higher than 13 dB are allowed. This graph, together with the interference mask specifications [21], can be used to determine the required filter that must precede the $\Delta\Sigma$ modulator.

CT modulators also exhibit implicit anti-alias filtering [6]. The measured alias frequency rejection was about 49 dB for ZIF mode and 47 dB for LIF mode. These values were found to be almost constant throughout the whole alias band (310 to 330 MHz for ZIF mode, and 300 to 340 MHz for LIF mode).

V. Conclusion

A complex multi-bit continuous-time delta-sigma modulator intended for IEEE 802.11a/b/g wireless LAN receivers was designed, fabricated and evaluated. This modulator runs at 320 MHz with an oversampling ratio of 16 for an input signal bandwidth of 20 MHz. It was designed in 0.25-μm standard CMOS technology using a 2.5-V power supply. It achieves approximately 55 dB of peak signal to noise ratio for complex signals. The modulator can operate on two modes: ZIF and LIF. In the ZIF mode it acts as two independent real (single input) modulators and it exhibits a NTF that is symmetrical around DC. In the LIF mode, the two real modulators are cross-coupled and the resulting NTF is shifted +10 MHz, making it adequate for the optimal digitization of signals from low-IF radio receivers. The performance of the complex modulator was tested experimentally using both sine-wave signals and modulated OFDM signals, proving that it meets the requirements for the intended application. The achievable SNR, together with the low distortion, high image frequency rejection, moderate power consumption and relaxed pre-filtering requirements makes this architecture a promising option for high-performance and low-cost, multi-mode, wireless-LAN receivers. The measured modulator performance is summarized in Table II.

TABLE II
Modulator Performance

Technology	0.25 μm 4M1P CMOS	
Area w. pads	1.30 mm^2	
Area w.o. pads	0.44 mm^2	
Supply voltage	2.5 V	
Experimental results	ZIF mode *(-10...+10 MHz)*	LIF mode *(0...+20 MHz)*
Power consumption		
Analog	18.4 mW	20.0 mW
Digital	12.0 mW	12.0 mW
Total	30.4 mW	32.0 mW
peak SNR	55.5 dB	54.5 dB
peak SNDR	53.9 dB	53.5 dB
ENOB	8.9 bits	8.7 bits
Image rejection	47.2 dBc	47.2 dBc
DC offset	10 mV	8 mV
EVM (min)	< 1.0%	1.3%
Blocker rejection		
@ 25 MHz	-	2 dB
@ 50 MHz	-	6 dB
@ 100 MHz	-	12 dB
Alias rejection	49 dB	47 dB

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