TABLE 4—64-BIT MICROPROCESSORS

	Company	EEMBC member	Device family	Bus interface (bits) (address/data)	Architecture type	FPU	MMU	Instruction width (bits)	Hardware multiplication support (bits)
mAgic FPU core	**Atmel** www.nergal.it/magic Enter No. 406	No	mAgic FPU core/mAgic Mate	External: 24, internal: 3×11 2×40	128-bit DSP-VLIW plus 32-bit RISC	IEEE-754-compliant, microcontroller extended single precision (40 bits)	Memory hierarchy: external memory, internal prefetch buffer, internal memory, multiport register file	128 VLIW, 32 RISC	40×40 floating point, 32×32 integer
64-bit MIPS	**Integrated Device Technologies** www.idt.com Enter No. 407	Yes*	RC64575	Multiplexed address/data buses	RISC	Double-precision	64-entry TLB	32	16×16, 32×32
	LSI Logic www.lsil.com Enter No. 408	Yes	EZ4021	64/64	RISC	No	32 dual pairs	32	64×64
	MIPS Technologies www.mips.com Enter No. 409	Yes	20Kc hard core	Optional	RISC	64-bit with paired-single and MIPS-3D enhancements	48 entries, variable page size 4 kbytes 16 Mbytes	32	32×32, 64×64, 32×64
			5Kc fully synthesizable core	Optional	RISC	Optional	64 entries, variable page size 4 kbytes to 16 Mbytes	32	32×32, 64×64, 32×64
	NEC Electronics www.necel.com Enter No. 410	Yes*	VR5432	Internal: 64/64, external: 32/32	RISC	IEEE-754, 64-bit, load and store	48 double-entry TLB, 32-bit physical range of 4 Gbytes	32	32×32
			VR4121	Internal: 32, 16/64	RISC		32 double-entry TLBs, 32-bit physical range of 4 Gbytes	32 and 16	No
			VR4122	Internal: 64, 32, 16	RISC		32 double-entry TLBs, 32-bit physical range of 4 Gbytes	32 and 16	No
			VR4300/10	Internal: 64, external: 32	RISC	IEEE-754-compliant	32 double-entry TLBs, 4 kbytes to 16 Mbytes	32	No
			VR5000	Internal: 64, external: 64	RISC	IEEE-754-compliant	48 double-entry TLBs, 4 kbytes to 16 Mbytes	32	32×32, 32×16
	QED www.qedinc.com Enter No. 411	Yes	RM5200	Internal: 64, external: 32 or 64	RISC	IEEE-754-compliant	96 virtual pages, 4-kbyte to 16-Mbyte pages	32	32×32 multiply/multiply-add
			RM7000	Internal: 64, external: 64	RISC	IEEE-754-compliant	96 virtual pages, 4-kbyte to 16-Mbyte pages	32	32×32 multiply/multiply-add
			RM5700	Internal: 64, external: 32 or 64	RISC	IEEE-754-compliant	96 virtual pages, 4-kbyte to 16-Mbyte pages	32	32×32 multiply/multiply-add
	SandCraft www.sandcraft.com Enter No. 412	Yes	SR1	SysAD 64 (64/36 physical, 133 MHz)	RISC	IEEE-754-compliant	48-entry TLB with odd/even pages per entry (total 96)	32-bit MIPS IV plus extensions	Integer 32×32, integer MAC, floating-point multiplier and MACC
			SR1-GX	SysAD 64 (64/36 physical, 133 MHz)	RISC	IEEE-754-compliant, single/double-precision, dual-vector single-precision	48-entry TLB with odd/even pages per entry (total 96)	32 MIPS IV plus extensions	Integer 32×32, integer MAC, floating-point multiplier and MACC
	Toshiba www.toshiba.com/taec Enter No. 413	Yes*	TX49 core	36/64	RISC	IEEE-754-compliant, single/double-precision	48 double-entry JTLBs, 4-kbyte to 16-Mbyte, two-entry instruction TLB, four-entry data TLB	32	32×32, 64×64
Sun UltraSPARC	**Sun Microsystems** www.sun.com/microelectronics/ Enter No. 414	Yes	UltraSPARC IIe Series (SME1701-CPGA)	External memory: 64 data with ECC	RISC	Quad precision IEEE 1596.5-1992 and single/double precision IEEE 754-1985 implemented in hardware	Entries: 64 data and 64 instruction; page sizes: 8, 64, 512, and 4096 kbytes; virtual/physical address: 44-bit virtual address in, 41-bit physical address out; separate instruction and data MMUs	32	Integer (single operations): 32×32, 64, 64×64,64; integer (multiple/partitioned operations): 8×16, 16 (to four-way); floating-point (single operations): 32×32, 32, 32×32, 64, 64×64, 64, 64×64, 128, 128×128, 128

* Published scores available

CPU frequency (MHz)	Operating voltage (V) (logic/I/O)	Typical power at maximum frequency	Power-down modes	Instruction cache (kbytes)	Data cache (kbytes)	Memory controller	Timers	Additional features	Price (10,000)
100	2.5/3.3	1.4/3.5W	No	8/16	42/62 dual-port RAM	Two/five local-memory-address generators, one external memory and prefetch-buffer-address generator	Three-channel, 16-bit timer/counter	Eight-level advanced interrupt controller, AMBA bus interface, ADC, and DAC	$32/$78
180 to 250	2.5		No	32, two-way-set-associative, lockable per line	32, two-way-set-associative, lockable per line	No	No	No	$42
250	Core: 1.8V	650 mW, 16-byte instruction cache, 16-kbyte data cache		16, set-associative	16, set-associative		One 32-bit (R4000)		ASIC core
400 at 600 at 0.18 µm	1.5 to 1.8, depending on process technology	3.1 mW/MHz	Yes	0 to 64	0 to 64	Optional	No		ASIC core
200 to 250 at 0.18 µm	1.5 to 1.8, depending on process technology	1 mW/MHz		0 to 64	0 to 64	Optional	No	Coprocessor interface, configurable cache sizes, fully synthesizable	ASIC core
167 to 200	2.5/3.3	2.5W		32, two-way-set-associative	32, two-way-set-associative			Dual-issue superscalar, DSP instruction, cache-line locking, JTAG, N-wire	$20 to $25
131 to 168	2.5/3.3	270 mW	Four power-management modes,25-mW sleep mode	16, direct-mapped	8, direct-mapped	Supports ROM, EDO-type DRAM, SDRAM, SROM, and flash	One real-time clock	Supports ISA-bus, keyboard, and touchpanel interface; IR controller; soft-modem interface; DMA; serial interface; interrupt controller; audio interface; ADC; external input clock	$20 to $25
150 to 180	1.8/3.3	350 mW	Four power-management modes, 30-mW sleep mode	32, direct-mapped	16, direct-mapped	Supports ROM, EDO-type DRAM, SDRAM, SROM, and flash	One real-time clock	PCI bus, ISAbus, keyboard, and touchpanel interface; IR controller; soft-modem interface; DMA; serial interface; interrupt controller; audio interface; ADC; external input clock	$33
133 to 167	3.3	1.2W/2.5W	No	16, direct-mapped	8, direct-mapped				$15
200 to 250	3.3	7W/5W	Standby	32, two-way-set-associative	32, two-way-set-associative	L2 cache, secondary cache controller		L2 cache interface as large as 2 Mbytes, dual-issue instruction mechanism	N/A
200 to 400	2.5/3.3	2W		32, two-way-set-associative with locking per set	32, two-way-set-associative with locking per set	RM5271 supports L2 cache	32-bit		N/A
250 to 500	2.5/3.3	4W		16, four-way-set-associative with cache-line locking	16, four-way-set-associative with cache-line locking	Supports L3 cache	32-bit	256-kbyte L2 cache	N/A
200 to 350	1.65/3.3	3W		32, two-way-set-associative with locking per set	32, two-way-set-associative with locking per set	64-bit SDRAM interface to 133 MHz	32-bit	Dual 32-bit PCI at 33/66 MHz, 512-byte SRAM	N/A
333 to 400 typical at 0.18 µm	1.8/3.3			16, two-way-set-associative, 32-byte line	16, two-way-set-associative, 32-byte line, multipolicy	No	One 32-bit	Supports five external interrupts, internal performance counters, debugging capabilities	N/A
333 to 400 typical at 0.18µm	1.8/3.3			16, two-way-set-associative, 32-byte line	16, two-way-set-associative, 32-byte line, multipolicy	No	One 32-bit	Supports five external interrupts, internal performance counters, debugging capabilities	N/A
133 to 200	TX49H: 2.5/3.3, TX49H2: 1.5/3.3	TX4955: TX49 core plus 32-kbyte/32-byte cache, SysAd bus at 133 MHz, TX49H: 1.5W	Reduced frequency, halt, doze	16/32, four-way-set-associative	16/32, four-way-set-associative, write-through, write-back	SDRAM with ECC, high-speed SRAM, flash, ROM, MROM, EEPROM, SRAM	32-bit	PCI Revision 2.2	$25 to $35
400, 500	1.5 to 1.7 at 400 MHz, 1.7 at 500 MHz/3.3	Estimated: 10W at 500 MHz, 7W at 400 MHz	Reduced frequency, dynamically selectable under software control: one-half and one-sixth normal CPU clock, 1.5W, one-sixth mode, 400 MHz normal CPU clock,2.5W, one-sixth: 500-MHz normal CPU clock	16, two-way-set-associative, physically indexed, physically tagged	16, direct-mapped, virtually indexed, physically tagged	PC-100 64-bit SDRAM interface, addresses as much as 2 Gbytes with ECC	No	External PCI bus: 32-bit, 66-MHz, 3.3V PCI 2.1-compatible; on-chip 256-kbyte L2 cache, four-way-set-associative	N/A