TABLE 3—32-BIT MICROPROCESSORS

	Company	EEMBC member	Device family or specific device	Bus interface (address/data) (bits)	FPU	MMU	Instruction width (bits)	Hardware multiplication support (bits)	CPU frequency	Operating voltage (V) (logic/I/O)
486	**AMD** www.amd.com Enter No. 440	Yes	Am486D	32/32	One, 80387-compatible	Yes	32		66, 100, 133	3.3/5
			AMD ÉlanSC400	32/32	No	Yes	32		33, 66, 100	2.7 to 3.6/5
ARC	**ARC Cores** www.arccores.com Enter No. 441	Yes	ARC	24 to 32/32	No	No	32	16×16, 16×16 MAC, 24×24 swap, 32×32	Technology-dependent	Technology-dependent
ARM	**Atmel** www.atmel.com/ Enter No. 442	No	AT91	External: 23/16, internal: 16/32	No	No	16 or 32	32×8	500 Hz to 40 MHz	1.8 to 3.6/ 2.7 to 5.5
	LinkUp Systems www.linkupsys.com Enter No. 443	No	L7200/ L7205	32/32	No	64-entry TLB	32	32×32	64 MHz	3.3
	Triscend www.triscend.com/products/index.html Enter No. 444x	No	A7; FPGA-based CSoC	Internal: 32 read, 32 write/32; external: 8 to 32 read/ 20 to 32	No	Eight protected, cachable, resizable memory regions	32 in ARM state; 16 in Thumb state, resulting in higher code density	32×8 in CPU, various options available in the on-chip programmable logic	As high as 66 MHz	2.5/2.5 to 3.3
Embedded x86	**AMD** www.amd.com Enter No. 445	Yes*	AMD-K6-2E	64/64	One IEEE 754/854-compatible	Yes	32		233, 266, 300, 333, 350, 400 MHz	2.2/3.3
			AMD ElanSC520	32/32	Yes	Yes	32		100, 133 MHz	2.5/5
	National Semiconductor www.national.com Enter No. 446	Yes*	Geode GX1 Processor Series	Internal: 64/64; external: PCI 32 multiplexed	IEEE-754-compatible, single-precision, 64 or 80 bits	Load/store reordering, memory-read bypassing	8, 16, 32, 48	8, 16, 32×8, 16, 32; and all MMX instructions	200 to 300 MHz	1.6 to 2/3.3
Hitachi SH-1	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 447	Yes	SH7020/21 and SH7032/34	24/16	No	No	16	16×16 and 42 MAC	20 MHz	3.3/5
Hitachi SH-2	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 448	Yes	SH7604		No	No	16	32×32 and 64 MAC	28 MHz	3.3/5
			SH7017		No	No	16	32×32 and 64 MAC	28 MHz	5
			SH7050		No	No	16	32×32 and 64 MAC	20 MHz	5
			SH7055		Single precision	No	16	32×32 and 64 MAC	40 MHz	3.3
			SH7045		No	No	16	Hardware multiplier handles 64-bit MAC and divide, 32×32 multiply	33 MHz	3.3/5
Hitachi SH-3	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 449	Yes	SH7077, SH7709A		No	WinCE-compatible	16	32×32 and 64 MAC	60, 80 MHz	3.3

* Published scores available.

Typical power at maximum frequency	Power-down modes	Instruction cache	Data cache	Non-volatile memory type and size	SRAM	Memory controller	Timers	Additional features	Price (10,000)
3W		16-kbyte unified write-back							N/A
2W		8-kbyte unified write-back						Dual interrupt controllers, bidirectional parallel port with EPP mode, XT/matrix keyboard interface, 32 general-purpose I/O pins, IrDA port,PCMCIA 2.1/ two PC-card controllers/slots, LCD graphics controller	N/A
Technology-dependent	Clock gating, sleep mode	Direct-mapped, multiway-set-associative, 0.5 to 32 kbytes				SRAM sequencer	One 24-bit	JTAG debugging port, 8-bit debugging port, 2- to 8-kbyte configurable processor	N/A
140 mW, 40 MHz, 3.3V	Sleep: 2 μA, idle 20 μA	No	No	As much as 2 Mbytes of flash		Eight chip selects; 8-, 16-, or 32-bit fetches, boot remap, pro grammable wait, external wait request	Six 16-bit	Based on ARM7TDMI; 10-bit, eight-channel ADC, two-channel DAC, watchdog timer, oscillator, PLL, as much as 136 kbytes	$7 to $22
390 mW	Deep sleep: 0.06 mW, standby: 2.2 mW, snooze: 16.5 mW, idle: 110 mW, run: 390 mW	2 kbytes, integrated instruction/ data			5 kybtes	SDRAM	Two 16-bit	32-bit ARM 720T plus eight DMA, 52 GPIO, Piccolo DSP; 7205 includes USB host and AC link	L7200: $20, L7205: $25
1650 mW	Power-down and power-management; selectively disable functions, including I/O pins	8-kbyte unified	8-kbyte unified		16 kbytes, also doubles as trace buffer	Glueless interface to 8-, 16-, or 32-bit static SRAM, flash and dynamic SDRAM, 100-pin SIMM	Two dedicated 16-bit, 32-bit watchdog; user can add more using programmable logic	As many as 40,000 on-chip programmable-logic gates to accommodate additional peripherals and coprocessing; more than 120 user-definable I/O pins, four-channel DMA controller, interrupt controller, hardware breakpoint unit, JTAG debugging support	From $12.95
7W		32-kbyte	32-kbyte						N/A
1.6W								Dual interrupt controllers, 32 general-purpose I/O pins, AMDebug technology	N/A
0.8W at 1.6V, 200 MHz; 1.2W at 2V, 300 MHz (assumes 80% active idle)	Active idle (suspend-on-halt): 0.6W at 1.6V, 200 MHz, standby: 170 mW at 1.6V, 200 MHz, sleep: 140 mW at 1.6V, 200 MHz	16-kbyte unified instruction and data, L1, write-back		N/A	N/A	64-bit SDRAM, 66 to 100 MHz, two 168-pin DIMMs, 512 Mbytes total		2-D graphics accelerator, display controller, PCI host controller	N/A
60 at 3.3V, 90 at 5V	Sleep: 40 mA, standby: less than 5 μA				SH7020/21: 1 kbyte, SH7032/34: 4/8 kbytes		Four 16-bit and watchdog	DRAM control; four DMA channels; 32 to 40 GPIOs; 16-, 32-, or 64-kbyte OTP ROM	N/A
60 at 3.3V, 70 at 3.3V	Sleep: 40 mA, standby: less than 5 μA	4-kbyte unified				SDRAM, SRAM, flash	One 16-bit and watchdog	Two-channel DMAC, hardware divide unit	$7 to $10
		1-kbyte, direct-mapped		64, 128 kbytes flash/ROM	3 or 4 kbytes	SDRAM, SRAM, flash	Five 16-bit and watchdog	Two-channel DMAC; eight-channel, 10-bit ADC, 82 GPIOs	$7 to $10
100 mA at 5V, 150 mA at 5V	Sleep: 80 mA at 5V, standby: 1 to 20 uA			128, 256 kbytes flash, ROM	6 or 10 kbytes	SDRAM interface	11 16-bit and watchdog	Four-channel DMAC; 16-channel, 10-bit ADC, 118 GPIOs	$20 to $25
				512 kbytes flash, ROM	32 kbytes	SDRAM interface	11 16-bit and watchdog	Four-channel DMAC; 32-channel, 10-bit ADC; FPU; two-channel CAN V2.0B; JTAG	$35 to $50
160 at 3.3V, 230 at 5V	Sleep: 140 mA, standby: less than 5 μA	1-kbyte, 256-entry, direct-mapped		128, 256 kbytes flash/ ROM/OTP	4 kbytes	SDRAM interface	Five 16-bit and watchdog	Four DMA channels; 82 or 106 GPIOs; eight-channel, 10-bit ADC	$10 to $15
100W at 3V, 240 mA at 3.3V	Sleep: 8 mA, standby: 2 μA	8-kbyte unified				DRAM, SRAM, ROM, and flash	32-bit, three-channel; 16-bit, one-channel; watchdog; real-time clock	Eight-channel, 10-bit ADC; two-channel, 8-bi DAC; four-channel DMAC; smart-card support; 108 GPIOs; IrDA V1.0. SH7077: LCD controller, PCMCIA support, keyboard interface; SH7709A: JTAG	$20 to $30

TABLE 3—32-BIT MICROPROCESSORS (CONTINUED)

	Company	EEMBC member	Device family or specific device	Bus interface (address/data) (bits)	FPU	MMU	Instruction width (bits)	Hardware multiplication support (bits)	CPU frequency	Operating voltage (V) (logic/I/O)
	Hitachi Semiconductor Enter No. 449		SH7708R, SH7718R		No	Addresses 4Gbytes, page-unit sharing, multiple page sizes, 128-entry TLB	16	32×32 and 64 MAC	100 MHz	3.3
Hitachi SH-3DSP	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 450	Yes	SH7729		No	Addresses 4Gbytes, page-unit sharing, multiple page sizes, 128 entry TLB	16	32×32 and 64 MAC	133 MHz	3
Hitachi SH-4	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 451	Yes	SH7750, SH7751	28/32	3-D matrix floating-point multiplier and FPU	Addresses 4Gbytes, page unit sharing, multiple page sizes, 128-entry TLB, WinCE-compatible	16	32×32 and 64 MAC	200, 167, 128 MHz; SH7751: 133, 167 MHz	3.3/1.8
Hitachi SH-DSP	**Hitachi Semiconductor** www.semiconductor.hitachi.com Enter No. 452	Yes	SH7065			No	16, 32	SH7065: 16×16 and 32 one-cycle MAC; SH7615: 32×32 and 64 MAC	60 MHz	3.3
Hyperstone E1	**Hyperstone Electronics** GmbH, E1-32X, E1-32XS, www.hyperstone-ag.com Enter No. 453	No	E1-32X, E1-32XS	Internal: 32; external: 8, 16, 32	No	No	16, 32, 48	16×16, 32×32	50 to 180 MHz	2.5 to 5
Improv Systems	**Improv Systems Inc** www.improvsys.com Enter No. 454	Yes	Jazz Processor	Internal: 12/32; external: 12 to 32/32	No	No	240 (typical 32-bit processor configuration)	32×32 typical; size is user-definable	0 to 200 MHz (0.18 µm CMOS)	1.8 (0.18-µm CMOS)
Infineon Tricore	**Infineon Technologies** www.infineon.com/tricore Enter No. 455	Yes*	V1.3 Core	Internal: 32/32, external: 32/32	No	1-, 4-, 16-, 64-kbyte pages, 128 table entries	16 and 32	Dual 16×16, 16×32, 32×32	0 to 200 MHz	1.8 (core only)
			TC10 GP	Internal: 32/32, external: 32/32	No	No	16 and 32	Dual 16×16, 16×32, 32×32	0 to 80 MHz	2.5/3.3
Intel i960	**Intel Corp** www.developer.intel.com Enter No. 456	Yes		16, 32, 64/16, 32, 64	SB and KB only	Hx only (Rx has MCU)	32, 64 bits	32×32	33, 66, 100 MHz	3.3/5
MIPS 32 bit	**Alchemy Semiconductor** www.alchemysemi.com Enter No. 457	No	Au1000	32/32	No	32 dual-entry, fully associative; page sizes of 4 kbytes to 16 Mbytes; four-entry ITB	32	32×16 MAC; divide hardware; maximum issue rate of one 32×16 MAC per clock	200 to 500 MHz	1.2 to 1.8/3.3
	IDT www.idt.com/products/ Enter No. 458	Yes*	RC32334	26/32	No	64-entry TLB	32	16×16, 32×32	100 to 150 MHz	3.3
	LSI Logic web address Enter No. 459	Yes	EZ4103	32/32	No	64 single entry	32 or 16	32×32	120 MHz worst case	1.8
	MIPS Technologies www.mips.com Enter No. 460	Yes	MIPS32 4Kc synthesizable core 4Kc/4Km/4Kp	32/32	No	32 entries, variable page size 4k-4M (4Kc only)	32	16×16 and 32×16 in one cycle, 32×32 in two cycles; 4Kp: 32×32 in 34 cycles	200 MHz	Process-dependent
	Toshiba www.toshiba.com Enter No. 461	Yes	TX39 core family	32/32	No	64 entry, 4k-4M pages, multihit detection	32 (TX19 supports MIPS16ISA)	32×32	66 to 133 MHz	Internal: TX39H: 3.3/3.3, TX39H2: 2.5/3.3, TX39H3: 1.5/3.3

* Published scores available.

Typical power at maximum frequency	Power-down modes	Instruction cache	Data cache	Non-volatile memory type and size	SRAM	Memory controller	Timers	Additional features	Price (10,000)
120W at 3.3V, 195W at 3V	Sleep: 75 mA, standby: 1 mA	8-kbyte unified				DRAM, SDRAM, flash	32-bit, three-channel; watch-dog; real-time clock	PCMCIA suppor, real-time clock, user break controller, eight GPIOs	$20 to $30
200 mA at 1.9V	Sleep: 75 mA, standby: 15 mA	16-kbyte unified				DRAM, SDRAM, flash	32-bit, three-channel; watchdog; real-time clock	PCMCIA support; real-time clock; user break controller; controls DRAM, SDRAM, flash, eight GPIOs	$20 to $30
N/A	Sleep: 10 mA, standby: 120 µA	8-kbyte, 256-entry, direct-mapped	16-kbyte, 512-entry, direct-mapped			SDRAM, SRAM, ROM, and flash	32-bit, three-channel; watchdog; real-time clock	Four-channel DMAC, smart-card support, 16 GPIOs, IrDA V1.0, JTAG; SH7751 also with PCI	SH7750: $20 to $30, SH7751: $25 to $35
190W at 2.7V, 350W at 2.7V	Sleep: 80 mA maximum, standby: 10 µA maximum	SH7065: none, SH7615: 4-kbyte unified		SH7065: 256 kbtyes flash	8 kbytes		16-bit, eight channel; watchdog	Four-channel DMAC, JTAG, SRAM control, 16-bit integer DSP,106 GPIOs; SH7615 also with 10/100 Ethernet MAC, IrDA V1.0, smart-card support	$25.01 to $50
200 mW	Automatic power-down (10 mW), sleep (clock off); PLL times one-half, one, two, four	128-byte instruction buffer	No		As much as 32 kbytes	Asynchron-ous SRAM, EPROM, flash, FPM/EDO DRAM, SDRAM	32-bit, watchdog	Four interrupt inputs	$8 to $12
Core only: 1.1 mW/MHz, peak; 0.5 mW/MHz typical (at 1.8V, 0.18-µm CMOS)	Core only: idle: 1 mW/MHz, sleep: less than 50 µW at 1.8V, 0.18-µm CMOS	No	No	8 kbytes ROM	54 kbytes	No	Four 16-bit	Multiprocessor ready, task queue, interrupts, various bus interfaces	ASIC core
310 mW	Sleep: 42 mW at 180 MHz; deep sleep, 13 mW at 180 MHz	As much as 32 kbytes, two-way set associative	As much as 32 kbytes, two-way set associative	No	56-kbyte dual-purpose cache/ SRAM under software control	No		255 interrupts, emulation and debugging support	N/A
250 mW	Sleep: 22 mW at 80 MHz, deep sleep: 9 mW at 80 MHz	16-kbyte, two-way set associative	16-kbyte, two-way set associative	No	40-kbyte dual-purpose cache/ SRAM under software control	SDRAM controller	Three gen-eral-purpose, one watch0 dog, one system timer	Eight external interrupts, three GPIOs, on-chip emulation and debugging support	N/A
0.3 to 7W	N/A	4- or 16-kbyte	16-kbyte, two-way set associative	N/A	1 kbyte	128-, 512-Mbyte SDRAM, ECC, EDO, FPM, DRAM	One, four SDRAM output clocks	Application-accelerator unit, PCI-to-PCI bridge, eight GPIOs, six secondary PCI clocks	$41.35 to $97.37
0.5W at 400 MHz, 1.5V	Two idle sleep	16-kbyte, four-way set associative	16-kbyte, four-way set associative	No	No	16/32-bit, 100-MHz SDRAM controller one-half speed of system bus or one-fourth speed of core clock speed; supports SRAM, flash, ROM, and page-mode ROM	Two pro-grammm-able with three matching registers	Two 10/100 Ethernet ports, fast IrDA, USB host/device, DMA, interrupt control, AC-97 link, GPIO, EJTAG, four chip selects, address and data lines can control PC Card/compact flash, LCD, and external-bus interfaces	$50
2W	No	8-kbyte, two-way set associative, lock able per line	2-kbyte, two-way set associative	No	No	DIMM and SO-DIMM SDRAM, ROM, flash SRAM	Three 24-bit	66-MHz PCI, four DMA channels, interrupt controller	$19
60 mW without cache		1- to 32-kbyte, set-associative or direct-mapped	1-to 32-kbyte, direct-mapped	N/A	N/A		Two 32-bit		ASIC core
100 mW at 0.18 µm	0.2 mW at 0.18 µm	0- to 16-kbyte	0- to 16-kbyte	N/A	User-configurable	Optional	Optional	Fully synthesizable core	ASIC core
	Reduced frequency, halt, doze	8- or 16-kbyte, two-way set associative	4- or 8-kbyte, two-way set associative, write-through		No	SDRAM, SGRAM, SMROM flash, ROM, MROM, EPROM, EEPROM, SRAM	24-bit, 32-bit, 40-bit 43-bit,, watchdog, real-time clock	DMAC, INTC, LCD controller, FIR, PCMCIA, PCI Revision 2.2	$15 to $35

TABLE 3—32-BIT MICROPROCESSORS (CONTINUED)

	Company	EEMBC member	Device family or specific device	Bus interface (address/data) (bits)	FPU	MMU	Instruction width (bits)	Hardware multiplication support (bits)	CPU frequency	Operating voltage (V) (logic/I/O)
Mitsubishi M32R/D	**Mitsubishi Electric Electronics USA Inc** www.mitsubishichips.com Enter No. 462	Yes*		External: 24/16; internal: 32/128 data	No	No	16, 32	16×16, 16×32, 32×16, 32×32, MAC instructions	66 or 80 MHz	2.7 to 5.5
Motorola 683xx	**Motorola** www.mot-sps.com Enter No. 463	Yes	68328, 68VZ328	Internal: 32/32; external 16, 24/16, 24	No	No	16 to 112	16×16, 32×32	16 to 33 MHz	3 to 5
			68302, 68360	Internal: 32/32; external 16, 24, 32/16, 24, 32	No	No	16 to 112	16×16, 32×32	16 to 33 MHz	3.3 to 5
			68306, 68340	Internal: 32/32, external: 16, 24, 32/16, 24, 32	No	No	16 to 112	16×16, 32×32		3.3 to 5
Motorola 68xxx	**Motorola** www.mot-sps.com Enter No. 464	Yes	68000	Internal: 32/32, external: 16, 24, 32/16, 24, 32	No	No	16 to 112	16×16, 32×32	8 to 20 MHz	3.3/5
			68020, 68030	32 dynamic	No	No Yes	16 to 112	16×16, 32×32	12 to 50 MHz	5
			68060, 68040	32/32	Yes	Yes	16 to 112	16×16, 32×32	25 to 75 MHz	3 to 5
Motorola ColdFire	**Motorola** www.mot-sps.com Enter No. 465	Yes	5206e	8, 16, 32 dynamic	No	No	16, 32, 48	16×16, 32×32	40, 50 MHz	3.3
			53xx	8, 16, 32 dynamic	No	No	16, 32, 48	16×16, 32×32	66, 90 MHz	3.3
			54xx	8, 16, 32 dynamic	No	No	16, 32, 48	16×16, 32×32	162 MHz	1.8/3.3
Motorola M CORE	**Motorola** www.mot-sps.com Enter No. 466	Yes	MMC2001, MMC2107	24/32			32	16×16, 32×32	As high as 33 MHz	1.8 to 3.6/ 1.8 to 5V
NEC V800	**NEC Electronics** www.necel.com Enter No. 467	Yes	V850 (SA1, SB1, and SF1)	22/16	No	No	16, 32	16×16	SA1, SB1: 20 MHz; SF1: 16 MHz	SA1: 2.7 to 3.6, SB1: 2 to 5.5, SF1: 3.5 to 5.5
		Yes	V853A	22/16	No	No	16, 32	16×16	33 MHz	4.5 to 5.5
		Yes	V850E (MS1, MA1, MA2, IA1)	24 to 26 address, 16 data	No	No	16, 32	32×32	33 to 50 MHz	3 to 3.6
		Yes*	V832	24/32	No	No	16, 32	32×32	143 MHz	2.3 to 2.7/ 3 to 3.6
Nios	**Altera** www.altera.com Enter No. 468	Yes	Nios	32/32	No	No		1 per clock	10 to 50 MHz	1.8
PowerPC	**IBM** www.chips.ibm.com Enter No. 469	Yes*	440GP	32/8, 16, 32	No	64-entry TLB; variable page size	32	32×32, 16×16 MAC	400 to 500 MHz	1.8/2.5 or 3.3
			405GP/ 405CR 401GF	32/8, 16, 32 32/32	No No	64-entry TLB; variable page size No	32 32	32×32, 16×16 MAC 32×32	200 to 266 MHz 50 MHz	2.5/3.3 3.3
			403GA/GB/ GC/GCX	32/32		64-entry TLB; variable page size (GC, GCX)	32	32×32	25 to 80 MHz	3.3
			740/750/ 750CX/ 750CXe	64/32	IEEE-754-compatible, single and double precision	128-entry two-way set associative ITLB and DTLB, hardware reload	32	32, fixed point arithmetic unit	200 to 700 MHz	1.8 to 2.1/1.8, 2.5, or 3.3 (750CX)

* Published scores available.

Typical power at maximum frequency	Power-down modes	Instruction cache	Data cache	Non-volatile memory type and size	SRAM	Memory controller	Timers	Additional features	Price (10,000)
1-Mbyte DRAM product at 66MHz: 396 mW, 2-Mbyte DRAM product at 66 MHz: 462 mW, 2-Mbyte DRAM product at 80 MHz: 544 mW	Standby: 4.95 mW, sleep: 264 mW	4-kbyte unified		No	1- or 2-Mbyte DRAM, no SRAM	Support for as much as 2 Mbytes of on-chip DRAM	No	MAC, BIU	1-Mbyte DRAM: $10.01 to $25 2-Mbyte DRAM: $25.01 to $50
	Stop	No	No	No	No	SDRAM, FPM, EDO	Two	PWM, SPI, LCD	$8 to $11
16 to 25 MHz	360 stop	No	No	No	No	DRAM			$12 to $30
	340 stop	No	No	No	No		One or two	DMA, JTAG	$8.21 to $26.07
		No	No	No	No	No	No	No	$2.80 to $32.25
		256-byte	0- to 256-byte	No	No	No	No	No	$8.35 to $102.74
		4- to 8-kbyte	4- to 8-kbyte	No	No	No	No	JTAG	$36.56 to $300.15
340 to 460 mW	Stop: 214.5, 287.1, halt: 214.5, 287.1	4-kbyte	2-kbyte	No	8 kbytes	FPM, EDO	Two	DMA, JTAG, MAC	$6.99 to $8.69
792 mW	Stop: 171.6, 181.5; halt: 531.3, 660	8-kbyte unified	8-kbyte unified	No	4 kbytes	SDRAM, FPM, EDO	Two	DMA, JTAG, MAC	$11.95 to $14.95
700 mW	Stop	16-kbyte	8-kbyte	No	4 kbytes	SDRAM, FPM, EDO	Two	DMA, JTAG, MAC	$19.95
	Wait, doze, stop			256-kbyte ROM, as much as 256 kbytes of flash	As much as 32 kbytes		Two 16-bit, four-channel, PIT, TOD, watchdog	Eight-channel, 10-bit ADC; PLL, as many as 100 GPIO pins	$10.01 to $25
75 to 125 mW	Halt, idle, stop	No	No	SA1: 256/512-kbyte flash, SB1: 256-kbyte flash, SF1: 128/256-kbyte flash	8 kbytes	SRAM	16-bit, two-channel; 8-bit, four-channel, watch, watchdog	Eight- to 12-channel, 10-bit ADC; eight to nine external interrupts; three- to six-channel RAM; DMA	N/A
365 mW	Halt, idle, stop			128/256-kbyte flash	8 kbytes	SRAM	16-bit, five-channel; watchdog	Two-channel, 12-bit PWM; 12-channel, 10-bit ADC, two-channel,8-bit DAC, 17 external interrupts, five PLLs	N/A
400 to 625 mW	Halt, idle, stop			128 to 256-kbyte flash	4 to 10 kbytes	EDO, SRAM, SDRAM	16-bit, eight-channel	Eight- to 12-channel, 10-bit ADC; four-channel DMAC; 20 to 25 external interrupts; PLL; MA1 has two-channel, 12-bit PWM	N/A
290 mW	Halt, stop	4-kbyte	4-kbyte		Instruction: 4 kbytes, data: 4 kbytes	SDRAM, SRAM	16-bit, two-channel	Four-channel DMAC, nine external interrupts, six or eight PLLs	N/A
	No	No	No	No	2 kbytes	Asynchronous SRAM, flash	Optional	FPGA-based soft core, windowed register file	$7 to $20
3W at 400 MHz	Sleep: 1W	32-kbyte	32-kbyte		8 kbytes	DDR and SDRAM controller	Five	PCI-X, two Ethernet MACs, GPIO, DMA controller	N/A
1.1W at 200 MHz 0.2W	 Wait: 40 mW, doze: 30 mW, nap: 5 mW	16-kbyte 2-kbyte	8-kbyte 1-kbyte		4 kbytes	SDRAM controller	Four Four	PCI, Ethernet MAC, GPIO, DMA controller	$23 to $65 $6.20
0.51W at 80 MHz	Wait: 30 mW, sleep: 0.1 mW	2-kbyte, GCX: 16-kbyte	1-kbyte, GCX: 8-kbyte			DRAM and DMA controllers	Four		$11 to $21
750CX: 6W at 500 MHz	Doze: 2.3W, nap: 250 mW, sleep: 200 mW	32-kbyte	32-kbyte			750CX 256-kbyte internal L2 or as much as 1 Mbyte external L2	Two	Thermal-assist unit, debugging support, performance monitor (750CX)	$50 to $210

TABLE 3—32-BIT MICROPROCESSORS (CONTINUED)

	Company	EEMBC member	Device family or specific device	Bus interface (address/data) (bits)	FPU	MMU	Instruction width (bits)	Hardware multiplication support (bits)	CPU frequency	Operating voltage (V) (logic/I/O)
	IBM Enter No. 469		603e/EM603e	64/32	IEEE-754-compatible, single and double precision	128-entry two-way set associative ITLB and DTLB, software reload	32	32, fixed-point arithmetic unit	100 to 200 MHz	2.5/3.3 and 3.3/3.3
PowerPC	**Motorola** http://motorola.com/PowerPC/ Enter No. 470	Yes	6xx	64/32	IEEE-754 compatible, single and double precision	Four petabytes of VM and 4 Gbytes physical; two 64-entry, two-way set-associative TLBs; two sets of four-entry BATS	32	64, single and double precision	100 to 300 MHz	2.5/3.3
			7xx	MPC745 and 755: 64/32; MPC740 and 750: 64/64	IEEE-754-compatible, single and double precision	Four petabytes of VM and 4 GBytes physical; two 64-entry, two-way set-associative TLBs; two sets of four-entry BATS	32	64, single and double precision	200 to 400 MHz	1.9 to 2.6/ 3.3 to 1.8
			74xx	64/64	IEEE-754 compatible, single and double precision	Four petabytes of VM and 4 GBytes physical; two 64-entry, two-way set-associative TLBs; two sets of four-entry BATS	32, AltiVec SIMD 8, 16, 32, 64, 128		350 to 500 MHz	1.8, 2.15/ 1.8, 2.5, 3.3
			MPC8240, MPC8260, MPC8255	64/64	IEEE-754-compatible, single and double precision	Four petabytes of VM and 4 GBytes physical; two 64-entry, two-way set-associative TLBs; two sets of four-entry BATS	32		100 to 250 MHz	2.5/3.3
			MPC860, MPC855T, MPC850, MPC823e	32/32	No	32-entry TLBs and fully associative instruction and data TLBs	32		50 to 80 MHz	3.3/5 TTL-compatible
ST20	**STMicroelectronics** www.st.com Enter No. 471	Yes*	ST20-C2	32/32	No	No	Native variable length: 8 to 16	16×32	50 to 120 MHz	3.3/1.8
			STi5500	32/32	No	No	Native variable length: 8 to 16	16×32	50 MHz	3.3
Tensilica Xtensa	**Tensilica Inc** www.tensilica.com Enter No. 472	Yes	Xtensa	32/32	IEEE-754-compatible	Optional	16, 24	16×16, 32×32	320 (0.18 μm, typical) MHz	3.3, 2.5, 1.8, 1.5
Toshiba TLCS900/H2	**Toshiba** www.toshiba.com/taec Enter No. 473	Yes	TLCS 900/H2	24/8, 16 or 32	No	No	8, 16, 32	8×8, 16×16	0.032 to 20 MHz	1.8 to 5.5

* Published scores available.

Typical power at maximum frequency	Power-down modes	Instruction cache	Data cache	Non-volatile memory type and size	SRAM	Memory controller	Timers	Additional features	Price (10,000)
4W at 200 MHz	Doze: 1.5W, nap: 150 mW, sleep: 120 mW	16-kbyte	16-kbyte				Two	Debugging support	$18 to $37
4W at 300 MHz	Doze, nap, and sleep; dynamic power management	16-kbyte	16-kbyte					Superscalar with as many as three instructions per clock into five independent execution units	N/A
5.8W at 400 MHz	Doze, nap, and sleep; dynamic power management; selectively activate functional units as needed	32-kbyte	32-kbyte			MPC750 and 755: backside L2 cache support for 256 kbytes, 512 kbytes, 1 Mbytes			N/A
5W at 400 MHz	Doze, nap, and sleep; thermal-assist unit and instruction-cache throttling under software control	32-kbyte	32-kbyte			Backside L2 cache support for 512 kbytes, 1 Mbyte, or 2 Mbytes		AltiVec Technology, MPX bus mode, SMP	N/A
2.5W at 133 MHz, 3W at 200 MHz	8240: dynamic power management	16-kbyte	16-kbyte			8240 memory controller with as much as 1-Gbyte SDRAM support to 100 MHz, 8260 memory controller with as much as 4 Gbytes SDRAM support	Four programmable	8240-PCI, DMA, I2O, I^2C, interrupt controller; 8260: time-processing unit	8260: $105, 8255: $75
		MPC860P, MPC860DP: 16-kbyte; MPC860SR, MPC860EN, MPC850, MPC855T: 4-kbyte	MPC860P, MPC860DP: 8-kbyte; MPC860SR, MPC860EN, MPC850, MPC855T: 4-kbyte			DRAM controller, glueless interface to DRAM, SIMMs, SRAM, EPROMs, and other	Four programmable		N/A
Core only: 300 mW		2- to 4-kbyte	2- to 4-kbyte	N/A	4 to 8 kbytes	EMI peripheral provides glueless support of SDRAM and burst flash as fast as 100 MHz; 8, 16, or 32 bits wide	Two 32-bit CPU	16 levels of interrupts, DCU: extensive nonintrusive debugging support	ASSP core
2W at 3.3V		2-kbyte	2-kbyte	N/A	4 kbytes	100-MHz SDRAM interface; glueless support of 8-, 16-, and 32-bit-wide DRAM and flash; SRAM, ROM	Two 32-bit CPU, three 32-bi, three 32-bit capture	SOC for set-top-box applications, MPEG2 video decoder, PAL/NTSC encoder, hardware transport-stream demultiplexor, vectored interrupts with eight prioritized levels, DMA, two MPEG DMAs, MPEG L1/2 audio decoder	$25
0.4 mW/MHz at 1.8V, 0.18 µm; Xtensa processor generator estimates power for various configurations	Architectural and logic features for power-down. Sleep mode via wait	0- to 16-kbyte, four-way set associative)	0- to 16-kbyte, four-way set associative)	0- to 64-kbyte instruction and data ROM	0 to 64 kbytes, instruction and data RAM	Optional	Three 32-bit	Vectra DSP coprocessor unit, additional functions via designer-defined Tensilica Instruction Extension language	Intellectual property licensing
0.6W at 20 MHz	run, stop, idle 1 and idle 2 mode	No	No	No	As much as 2 kbytes	Yes	8- and 16-bit	LED, ADC, DAC, watchdog timer, µDMA	$10 to $35