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MC68060
MC68LC060
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Product Brief
Superscalar 32-Bit Microprocessors

The superscalar M68060 represents a new line of Motorola microprocessor products. The first generation of the M68060 product line consists of the MC68060, MC68LC060, and MC68EC060. All three microprocessors offer superscalar integer performance of over 100 MIPS at 66 MHz. The MC68060 comes fully equipped with both a floating-point unit (FPU) and a memory management unit (MMU) for high-performance embedded control and desktop applications. For cost-sensitive embedded control and desktop applications where an MMU is required, but the additional cost of a FPU is not justified, the MC68LC060 offers high performance at a low cost. Specifically designed for low-cost embedded control applications, the MC68EC060 eliminates both the FPU and MMU, permitting designers to leverage MC68060 performance while avoiding the cost of unnecessary features. Throughout this product brief, all references to the MC68060 also refer to the MC68LC060 and the MC68EC060, unless otherwise noted. Figure 1 illustrates a block diagram of the MC68060.

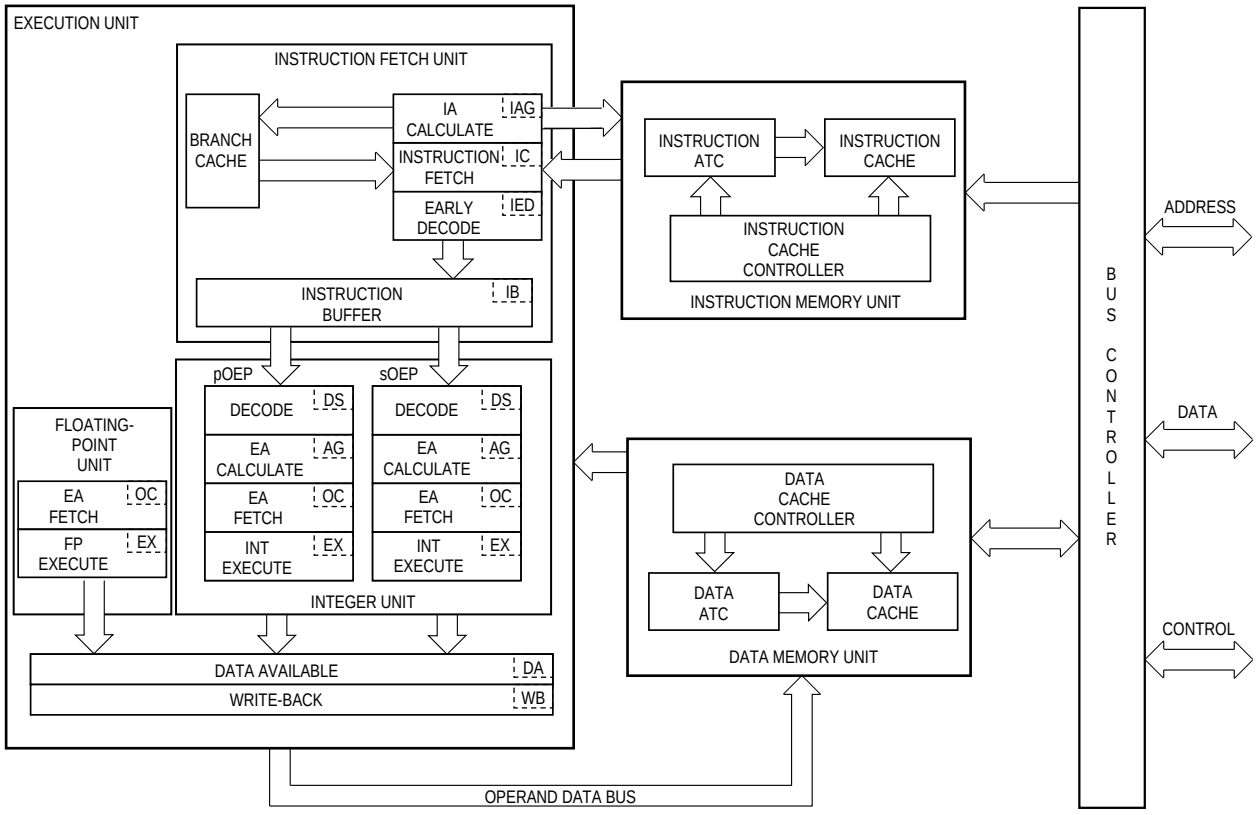

Figure 1. MC68060 Block Diagram

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SEMICONDUCTOR PRODUCT INFORMATION

Leveraging many of the same performance enhancements used by RISC designs as well as providing innovative architectural techniques, the MC68060 harnesses new levels of performance for the M68000 family. Incorporating 2.5 million transistors on a single piece of silicon, the MC68060 employs a deep pipeline, dual issue superscalar execution, a branch cache, a high-performance floating-point unit (MC68060 only), eight Kbytes each of on-chip instruction and data caches, and dual on-chip demand paging MMUs (MC68060 and MC68LC060 only). The MC68060 allows simultaneous execution of two integer instructions (or an integer and a floating-point instruction) and one branch instruction during each clock.

The MC68060 features a full internal Harvard architecture. The instruction and data caches are designed to support concurrent instruction fetch, operand read, and operand write references on every clock. Separate 8-Kbyte instruction and 8-Kbyte data caches can be frozen to prevent allocation over time-critical code or data. The independent nature of the caches allows instruction stream fetches, data-stream fetches, and external accesses to occur simultaneously with instruction execution. The operand data cache is four-way banked to permit simultaneous read and write access each clock.

A very high bandwidth internal memory system coupled with the compact nature of the M68000 family code allows the MC68060 to achieve extremely high levels of performance, even when operating from low-cost memory such as a 32-bit wide dynamic random access memory system.

Instructions are fetched from the internal cache or external memory by a four-stage instruction fetch pipeline. The MC68060 variable-length instruction system is internally decoded into a fixed-length representation and channeled into an instruction buffer. The instruction buffer acts as a FIFO which provides a decoupling mechanism between the instruction fetch unit and the operand execution units. Fixed format instructions are dispatched to dual four-stage pipelined RISC operand execution engines where they are then executed.

The branch cache also plays a major role in achieving the high performance levels of the MC68060. It has been implemented such that most branches are executed in zero cycles. Using a technique known as branch folding, the branch cache allows the instruction fetch pipeline to detect and change the instruction prefetch stream before the change of flow affects the instruction execution engines, minimizing the need for pipeline refill.

In addition to substantial cost and performance benefits, the MC68060 also offers advantages in power consumption and power management. The MC68060 automatically minimizes power dissipation by using a fully-static design, dynamic power management, and low-voltage operation. It automatically powers-down internal functional blocks that are not needed on a clock-by-clock basis. Explicitly, the MC68060 power consumption can be controlled from the operating system. Although the MC68060 operates at a lower operating voltage, it directly interfaces to both 3-V and 5-V peripherals and logic.

Complete code compatibility with the M68000 family allows the designer to draw on existing code and past experience to bring products to market quickly. There is also a broad base of established development tools, including real-time kernels, operating systems, languages, and applications, to assist in product design. The functionality provided by the MC68060 makes it the ideal choice for a range of high-performance embedded applications and computing applications. With M68000 family code compatibility, the MC68060 provides a range of upgrade opportunities to virtually any existing MC68040 application.

The following is a list of primary featuresof the MC68060:

- Fully User-Code Compatible with MC68040
- Superscalar Implementation of M68000 Architecture
  - — Dual Integer Instruction Execution Improves Performance
- Branch Cache Reduces Branches to Zero Cycles
- Executes Three Instructions per Clock
- Dual 8-Kbyte On-Chip Caches
  - — Separate Data and Instruction Caches
  - — Simultaneous Access
  - — Data Cache is Four-Way Banked to Allow Read and Write Access on Each Clock
- Bus Snooping
- Independent Instruction and Data Paged MMUs (MC68060 and MC68LC060 Only)
- Full 32-Bit Nonmultiplexed Address and Data Bus
  - — Optimized to Achieve Very High Performance Using 32-Bit Memory System
  - — Can Operate Bus at 1/2-or 1/4-Speed of Internal Clock
  - — 32-Bit Bus Maximizes Data Throughput
  - — Nonmultiplexed Bus Simplifies Design
  - — Four-Deep Store Buffer and One-Deep Push Buffer to Maximize Write Bandwidth
  - — MC68040-Compatible Bus Provides Simple Hardware Migration Path
- Power Management
  - — Automatic Power-Down of Unused Blocks of Logic on a Clock-by-Clock Basis
  - — Low-Voltage Operation at 3.3 V, with 3.3-V and 5-V I/O Capability
  - — LPSTOP Mode Provides an Idle State for Lowest Standby Current
  - — Static CMOS Technology Reduces Power in Normal Operation
- IEEE-Compatible On-Chip FPU (MC68060 Only)
- Available in 40-MHz (MC68EC060 only), 50-MHz, and 66-MHz Speeds
- Packaging
  - — Ceramic Pin Grid Array (PGA)
  - — Ceramic Quad Flat Pack (CQFP)

MC68060 SIGNALS

Figure 2 shows the MC68060 functional signal groups.

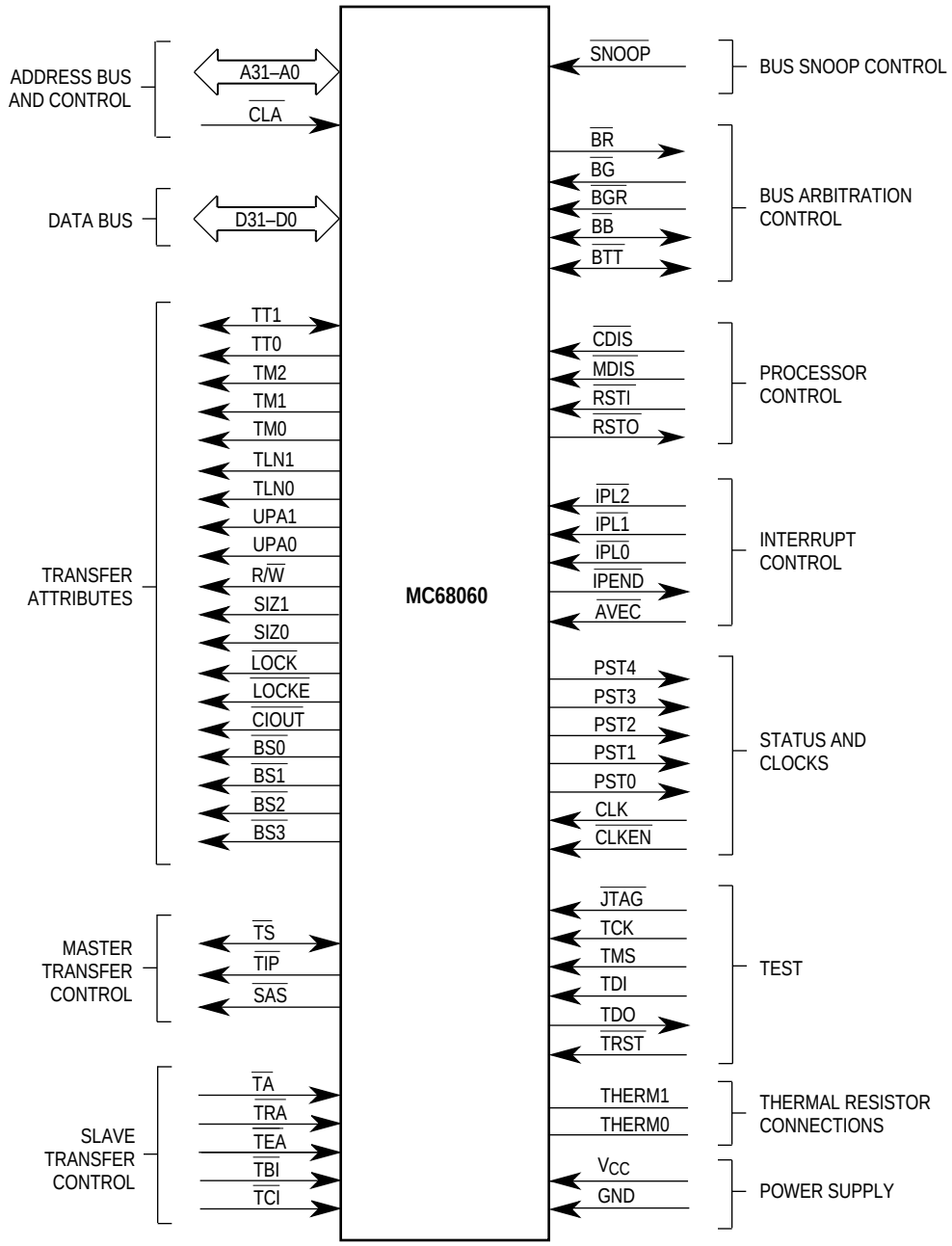

Figure 2. Functional Signal Groups

EXECUTION UNIT

The MC68060 execution unit carries out logical and arithmetic operations. The execution unit contains an instruction fetch unit, an integer unit, a branch cacheand a floating-point unit. The superscalar design of the MC68060 provides dual execution pipelines in the instruction integer unit, providing simultaneous instruction execution.

The superscalar operation of the execution unit can be disabled in software, turning off the second execution pipeline for debugging. Disabling the superscalar operation also lowers power consumption.

INSTRUCTION FETCH UNIT

The instruction fetch unit contains an instruction fetch pipeline and the logic that interfaces to the branch cache. The instruction fetch pipeline consists of four stages, providing the ability to prefetch instructions in advance of their actual use in the instruction execution controller. The continuous fetching of instructions keeps the instruction execution unit busy for the greatest possible performance. Every instruction passes through each of the four stages before entering the integer unit. The four stages in the instruction fetch pipeline are:

1) Instruction Address Calculation—The virtual address of the instruction is determined.
2) Instruction Fetch—The instruction is fetched from memory.
3) Early Decode—The instruction is pre-decoded into a fixed length format for pipeline control information.
4) Instruction Buffer—The instruction and its pipeline control information are buffered until the integer execution pipeline is ready to process the instruction.

BRANCH CACHE

The branch cache plays a major role in achieving the performance levels of the MC68060. The concept of the branch cache is to provide a mechanism that allows the instruction fetch pipeline to detect and change the instruction stream before the change of flow affects the integer unit.

The branch cache is examined for a valid branch entry after each instruction fetch address is generated in the instruction fetch pipeline. If a hit does not occur in the branch cache, the instruction fetch pipeline continues to fetch instructions sequentially. If a hit occurs in the branch cache, indicating a branch taken instruction, the current instruction stream is discarded and a new instruction stream is fetched starting at the location indicated by the branch cache.

INTEGER UNIT

The integer unit contains dual integer execution pipelines, interface logic to the FPU (MC68060 only), and control logic for data written to the data cache and MMU. The superscalar design of the dual integer execution pipelines provides for simultaneous instruction execution, which allows processing more than one instruction during each machine clock cycle. The net effect of this is a software-invisible pipeline capable of sustained execution rates of less than one machine clock cycle per instruction for the M68000 instruction set.

The integer unit control logic pulls an instruction pair from the instruction buffer every machine clock cycle, stopping only if the instruction information is not available or if an integer execution pipeline hold condition exists. The six stages in the dual integer execution pipelines are:

1) Instruction Decode—The instruction is fully decoded.
2) Effective Address Calculation—If the instruction calls for data from memory, the location of the data is calculated.
3) Effective Address Fetch—Data is fetched from the memory location.
4) Integer Execution—The data is manipulated during execution.
5) Data Available—The result is available.
6) Write-Back—The resulting data is written back to on-chip caches or external memory.

The MC68060 is optimized for most integer instructions to execute in one machine clock cycle. If during the instruction decode stage the instruction is determined to be a floating-point instruction, it will be passed to the FPU after the effective address fetch stage. If data is to be written to either the on-chip caches or external memory after instruction execution, the write-back stage holds the data until memory is ready to receive it. Temporarily holding data in the write-back stage adds to the overall performance of the MC68060 by not slowing down pipeline operations.

The MC68060 implements practically all of the MC68040 instructions and addressing modes in hardware for the highest performance. However, to optimize silicon usage, a very few infrequently used integer instructions are not fully implemented in hardware. These instructions are emulated in software using the M68060SP which is available free from Motorola. This software package assures full binary compatibility. Since these instructions appear very infrequently in the instruction stream, software emulation of the instructions provides no noticeable loss in performance.

FLOATING-POINT UNIT (MC68060 ONLY)

Floating-point math is distinguished from integer math, which deals only with whole numbers and fixed decimal point locations. The IEEE-compatible MC68060 FPU computes numeric calculations with a variable decimal point location. The MC68060 features a built-in FPU that is MC68040 and MC68881/882 compatible. Consolidating this important function on-chip speeds up overall processing and eliminates the interfacing overhead associated with external accelerators. The MC68060 FPU operates in parallel with the integer unit. The FPU performs numeric calculations while the integer unit continues integer processing.

The FPU has been optimized for the most frequently used instructions and data types to provide the highest possible performance. The FPU can also be disabled in software to reduce system power consumption.

The MC68060 implements the most frequently used M68000 family floating-point instructions, data types, and data formats in hardware for the highest performance. The remaining instructions are emulated in software with the M68060SP to provide complete IEEE compatibility. The M68060SP provides the following features:

- Arithmetic and Transcendental Instructions
- IEEE-Compliant Exception Handlers
- Unimplemented Data Type and Data Format Handlers

MEMORY MANAGEMENT UNITS
(MC68060 AND MC68LC060 ONLY)

The MC68060 contains independent instruction and data MMUs. Each MMU contains a cache memory called the address translation cache (ATC). The full addressing range of the MC68060 is four Gbytes (4,294,967,296 bytes). Even though most MC68060 systems implement a much smaller physical memory, by using virtual memory techniques, the system can appear to have a full four Gbytes of physical memory available to each user program. Each MMU fully supports demand-paged virtual-memory operating systems with either 4- or 8-Kbyte page sizes. Each MMU protects supervisor areas from accesses by user programs and provides write protection on a page-by-page basis. For maximum efficiency, each MMU operates in parallel with other processor activities. The MMUs can be disabled for emulator and debugging support.

The 64-entry, four-way, set-associative ATCs store recently used logical-to-physical address translation information as page descriptors for instruction and data accesses. Each MMU initiates address translation by searching for a descriptor containing the address translation information in the ATC. If the descriptor does not reside in the ATC, the MMU performs external bus cycles through the bus controller to search the translation tables in physical memory. After being located, the page descriptor is loaded into the ATC, and the address is correctly translated for the access.

INSTRUCTION AND DATA CACHES

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the M68000 family took advantage of this locality-of-reference phenomenon to varying degrees. The MC68060 takes further advantage of cache technology with its two, independent, on-chip physical caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of the MC68060 yield a very high hit rate, providing a substantial increase in system performance.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and external accesses to occur simultaneously with instruction execution. For example, if the MC68060 requires both an instruction access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and it is resident in the data cache, it can be accessed without hindering either the instruction access or the external peripheral access. The parallelism inherent in the MC68060 also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

Each MC68060 cache is eight Kbytes and is accessed by physical addresses. The data cache can be configured as write-through or deferred copyback on a page basis. This choice allows for optimizing the system design for high performance when deferred copyback is used.

Cachability of data in each memory page is controlled by two bits in the page descriptor. Cachable pages can be either write-through or copyback, with no write-allocate for misses to write-through pages.

The MC68060 implements a four-entry write buffer that maximizes system performance by decoupling the integer pipeline from the external system bus. When needed, the write buffer allows the pipeline to generate writes every clock cycle, even if the system bus runs at a slower speed than the processor.

CACHE ORGANIZATION

The instruction and data caches are each organized as four-way set associative, with 16-byte lines. Each line of data has associated with it an address tag and state information that shows the line's validity. In the data cache, the state information indicates whether the line is invalid, valid, or dirty.

CACHE COHERENCY

The MC68060 has the ability to watch, or snoop, the external bus during accesses by other bus masters, maintaining coherency between the MC68060 caches and external memory systems. External bus cycles can be flagged on the bus as snoopable or nonsnoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches and invalidates the matching data. Although the execution unit and the bus snooper circuit have access to the on-chip caches, the snooper has priority over the execution unit.

BUS CONTROLLER

The bus is implemented as a nonmultiplexed, fully synchronous protocol that is clocked off the rising edge of the input clock. It is compatible with an MC68040 bus. The bus controller operates concurrently with all other functional units of the MC68060 to maximize system throughput. The timing of the bus is fully configurable to match external memory requirements.

The $\overline{\text{CLKEN}}$ input is used on the MC68060 to enable to the clock edges on which the bus controller will respond. By toggling the $\overline{\text{CLKEN}}$ pin, it is possible to operate the MC68060 on an external bus at 1/2 or 1/4 the speed of the processor clock.

Although the MC68060 bus is compatible with the MC68040, additional signals and protocols have been added to simplify designs requiring very high bus speeds.

IEEE 1149.1 TEST

To aid in system diagnostics, the MC68060 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as Joint Test Action Group (JTAG).

POWER MANAGEMENT

The MC68060 is very power efficient due to the static logic and power management designed into the basic architecture. Each stage of the integer unit pipelines and the FPU pipeline draws power only when an instruction is executing, and the cache arrays draw power only when an access is made. The FPU, secondary integer execution pipeline, branch cache, and instruction and data caches can be disabled to reduce overall power usage. The 3.3-V power supply reduces current consumption by 40–60% over that of microprocessors using a 5-V power supply.

The MC68060 has additional methods for dynamically controlling power consumption during operation. Running a special LPSTOP instruction shuts down the active circuits in the processor, halting instruction execution. Power consumption in this standby mode is greatly reduced. Processing can be resumed by resetting the processor or by generating an interrupt. The frequency of operation can be lowered to reduce current consumption while the device is in LPSTOP mode.

PHYSICAL

The MC68060 is available in ceramic PGA and CQFP packaging configurations. All parts operate from a 3.3 V 5% power supply but directly interface to 3.3 V or 5 V peripherals and logic. The following table identifies the operating frequencies available for the various M68060 microprocessors.

Processor	40 MHz	50 MHz	66 MHz
MC68060		X	X
MC68LC060		X	X
MC68EC060	X	X	X

The documents listed in the following table contain detailed information on the MC68060. These documents may be obtained from the Literature Distribution Centers at the addresses listed on the back page.

Document Title	Order Number	Contents
M68060 User's Manual	M68060UM/AD	Detailed information for design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
The 68K Source	BR729/D	Independent vendor listing supporting software and development tools
3.3 Volt Logic and Interface Circuits	BR1407/D	Low voltage interface components

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION