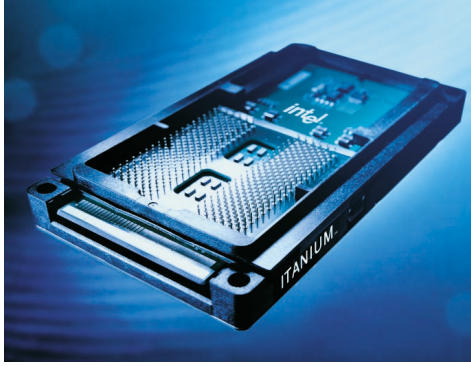

Intel® Itanium™ Processor

Product Brief

The Intel® Itanium™ processor is the first in a family of processors based on the new Itanium architecture. The Itanium processor was designed from the ground up to meet the increasing demands for high availability, scalability and performance needed for high-end enterprise and technical computing applications.

The Itanium processor uses Explicitly Parallel Instruction Computing (EPIC) technology to enable breakthrough levels of performance in targeted application segments. EPIC's explicit parallelism provides the capability to execute multiple instructions simultaneously. EPIC also delivers new features such as predication and speculation to overcome legacy performance limitations such as instruction branches and memory latency.

The Itanium processor family extends open-standards-based computing to the enterprise and brings flexibility, choice and value over proprietary solutions. A broad range of Itanium-based software offerings from industry-leading vendors combined with IA-32 instruction binary compatibility in hardware providing an increased level of investment protection.

PRODUCT HIGHLIGHTS

- Explicitly Parallel Instruction Computing (EPIC) technology enables up to 20 operations/clock.
- Three levels of cache reduce memory latency: 2MB or 4MB Level 3 cache, 96K Level 2 cache, and 32K Level 1 cache.
- Operating frequencies of 733MHz and 800MHz.
- 266MHz data bus enables fast system bus transactions with 2.1 GB/sec bandwidth.
- Advanced error detection, correction and containment provided by Machine Check Architecture (MCA), comprehensive error logging, and Error Correcting Code (ECC) on caches and the system bus.
- System management features such as a thermal sensing device.
- IA-32 instruction binary compatibility in hardware.
- Transistor Count (25 million transistors in CPU/300 million in cache.)

PERFORMANCE

ITANIUM™ PROCESSOR FEATURES

- Unified 2MB or 4MB on-cartridge L3 cache. Runs at full processor frequency and is organized as 4-way set-associative with 64-byte cache line size. Fully pipelined and optimized to provide fast access to data at a bandwidth of 12.8GB/sec using a 128-bit wide cache bus.
- Unified L2 cache is 96KB, 6-way set-associative, and fully pipelined with 64-byte cache line size.
- L1 cache, with separate instruction and data caches, is 32KB (16KB data/16KB instruction), 4-way set-associative, and fully pipelined with 32-byte cache line size.
- Highly parallel, pipelined hardware with 10-stage pipeline.
- Two integers units and two memory units, able to execute four ALU instructions per clock.
- Floating-point (FP) unit containing two FMAC (Floating-Point Multiply Accumulate) units operates on 82-bit operands. Each FMAC unit can execute two floating-point operations per clock with single, double and double-extended precision.
- Two additional FP multimedia units are capable of executing two single-precision FP operations each. Combined with the regular FMACs, a total of eight single precision FP operations can be executed every cycle resulting in 6.4 GFLOPS maximum.
- 44 bits of physical memory addressing.
- Integrated system management features provide temperature monitoring and cartridge identification information.
- Advanced Load Address Table (ALAT) containing 32 entries and organized as a 2-way set-associative cache provides support for speculation, minimizing memory latency and improving performance.
- Data Translation-Lookaside-Buffer (DTLB) has two-level hierarchy with 32 entries in DTLB1 (fully associative) and 96 entries in DTLB2 (fully associative). In addition, 48 Translation Registers (TRs) can be used exclusively by the system software (OS) to store critical virtual-to-physical address translations.
- Instruction Translation-Lookaside-Buffer (ITLB) contains 64 entries and is fully associative.

ITANIUM™ ARCHITECTURE

- Explicitly Parallel Instruction Set Computing (EPIC) technology increases Instruction Level Parallelism (ILP) by maximizing hardware-software synergy. The Itanium architecture provides mechanisms such as branch and cache hints for the compiler to communicate compiler time information to the processor. In addition, the architecture allows compiled code to manage the processor hardware more efficiently through an innovative instruction format. These communication mechanisms minimize the cost of branches and reduce cache misses while enabling more parallelism than is otherwise inherent in the code.
  - Speculation: Improves performance by allowing the compiler to schedule load instructions ahead of branches and stores to reduce memory latency.
  - Predication: Improves performance by eliminating branches and associated branch misprediction penalties.
  - Parallelism: Delivers higher performance and scalability by enabling the compiler to provide more information to the processor allowing it to execute multiple operations simultaneously on a sustained basis.
  - Register Stacking: Reduces call/return procedure overhead via the flexible integer register model managed by the Register Stack Engine (RSE).
  - Register Rotation: Automatically renames registers in hardware to improve software loop performance without the additional overhead required in traditional methods.
  - Branch/Memory Hints: Improves branch prediction rate and reduces memory latency.
  - SIMD instructions: Significantly improves multimedia application performance by operating on multiple integer or floating-point operands per single instruction.
- Massive register resources: 128 integer registers, 128 floating point registers, 8 branch registers, 64 predicate registers.

SYSTEM BUS ARCHITECTURE

- Increased bus efficiency through enhanced deferred transactions.
- 266MHz data bus (bus fraction 2:11 and 2:12).
- System data bus throughput up to 2.1GB/sec.
- Enhanced version of low-voltage AGTL+ (Advanced Gunning Transceiver Logic) signal technology.
- 64-bit wide data bus (plus 8 bits of ECC).

PHYSICAL CHARACTERISTICS

- ~3" x 5" cartridge contains the Itanium processor and up to 4MB of on-cartridge L3 cache.
- Dedicated edge power connector delivers separate voltages for the processor and cache devices to improve signal integrity.
- Integrated heat pipe lid improves thermal performance of heat sink and enables passive cooling.

AVAILABILITY

- Enhanced Machine Check Architecture enables processor, firmware and OS to cooperate to contain and fix errors, reducing downtime.
- Notification of corrected errors allows the OS/platform to maintain error statistics allowing proactive preventative actions and system maintenance decisions to be made.
- Error Checking & Correction (ECC) provides increased availability, enabling detection and correction of data errors in L2 data cache, L3 tag and data cache, and processor data bus.
- Parity checking on L1 cache provides increased reliability by enabling detection of errors.
- Server Management features provide for increased system availability.
  - Thermal sensor provides increased thermal management.
  - Processor information ROM includes key processor information and built-in programmable EEPROM for special-purpose software (e.g., inventory management).
  - Known SMBus implementation simplifies system design.
- Processor watchdog timer detects system hang conditions.

SCALABILITY

- Scalability features enable large systems to scale to 32 processors and beyond with increased throughput.
- Optimized memory utilization.
  - 64-bit flat address space (no copy overhead for >4GB.)
  - Flexible page sizes up to 256MB reduces paging overhead.
  - Innovative three-level cache hierarchy reduces bus traffic.
  - Speculation allows processor to hide memory latency.
- Highly efficient system bus.
  - Enhanced deferred transaction support makes bus transactions more efficient.
  - 5-load shared bus with 2.1GB/sec bandwidth.
  - Dedicated, full-speed L3 bus frees system bus for MP traffic.
- Increased resources more effectively manage large data sets and high-volume workloads: 17 execution units, up to 4MB of cache, 256 on-die registers.

INVESTMENT PROTECTION AND CHOICE

- Industry-leading vendors are providing a broad range of Itanium-based software offerings for enterprise server, workstation and technical computing solutions.
- Itanium-based software is compatible across current and future Itanium architecture processors.
- IA-32 instruction binary compatibility in hardware.

For more information, visit our Web site at http://www.developer.intel.com/design/ia-64.

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