Rev 1.3

Summary of Differences Between Engineering Sample and Production Release revisions of SX48/52

The following table will assist customers in understanding the differences between SX48/52 (engineering sample silicon revision) and the production release SX48/52. There are numerous additional internal differences, but these do not affect customer applications.

	SX48/52BD (Engineering Sample)	SX48/52BD (Production Release)
Compatibility Features	Following features can be enabled for compatibility To PIC 16C5x: -1:4 or 1:1 instruction to clock ratio -2 or 8 level stack -6 or 8-bit OPTION register	Compatibility features removed (fixed 1:1 instruction to clock ratio, 8 level stack, and 8-bit OPTION register)
Interrupt Stack	Single level stack, which buffers the contents of the PC, FSR, STATUS, and W registers.	Same, but also buffers the contents of the MODE register.
Supply Voltage	4.5 – 5.5V (0 – 70C)	3.0 – 5.5V @ 50MHz (0 - 70C) 4.75 – 5.25V @ 100MHz (0 – 70C)
Analog Blocks	IRC, WDT, POR, BOR, and RC circuits similar to previous designs.	All blocks reviewed and modified as required.
Comparator	On-board CMP features: -Common-mode voltage range from 0.4 to Vdd-1.3V -typ +/-1V input offset (should be max +/-25mV) -250nS response	On-board CMP features: -Common-mode voltage range from 0V to Vdd -typ +/-10mV input offset (max +/-25mV) -250nS response -Operation across 0 - 70 deg C
Oscillator Circuit	Similar OSC circuitry SX18/20/28AC (old datecode)	-OSC circuitry updated to new robust OSC circuits based on SX18/20/28AC (new datecode) -ability to disable clock driver
FUSE Word	Same as SX18/20/28AC (old datecode)	Same as to SX18/20/28AC (new datecode), with the exception of: -bit 11 is unused -bit 7 enables IRC or enables XTL -bit 4 used for crystal buffer enable (XTLBUF_EN)
FUSEX Word Register	-bit 11 used for sleep clock disable (SLPCLK) -bits 8,9,10 used for Delay Reset Timer (DRT) timeout period -bit 7 used for Carry Flag enable (CF) -bits 4, 5, 6 are used for IRC trimming -bits 2,3 unused -bits 0 and 1 are used for Brown Out Reset level select	Same as to SX18/20/28AC (new datecode), with the exception of: -bit 10 is used for sleep clock disable (SLPCLK) -bit 7 is unused -bits 0,1 used for Delay Reset Timer (DRT) timeout period

Delay Reset Timer (DRT) Timeout Period	A 3-bit field (WDRT2: WDRT0, bits 10, 9, 8) in the FUSEX Word register can be used to specify the DRT timeout period that results in an automatic wake-up from the power down mode.	A 2-bit field (WDRT1: WDRT0, bits 0, 1) in the FUSEX Word register to be used to specify the DRT timeout period.
Bank Instruction	Modifies bits 5, 6, and 7 of the FSR. Bit 4 is cleared by default. After every BANK instruction, FSR bit 4 must be set if an odd bank ($10, $30, $50, $70, $90, $B0, $D0 and $F0) is to be accessed. A single BANK instruction can only be used to switch between even banks.	Modifies bits 4, 5, and 6 of the FSR. Bit 7 is left to the user to modify. After use of the BANK instruction, FSR bit 7 must be set (or cleared) only if moving between upper ($80, $90, $A0, $B0, $C0, $D0, $E0 and $F0) or lower ($00, $10, $20, $30, $40, $50, $60 and $70) banks of data memory. A single BANK instruction can only be used to switch between upper banks (if FSR.7 is set) or between lower banks (if FSR.7 is clear).
Device ID	$001	$002
MODE register shadow	No MODE register shadow on interrupts.	MODE register shadowed on interrupt.