SX52BD EMI Evaluation: EMI Results and Board Design Recommendations

SCENIX

Application Note 34
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1.0 INTRODUCTION

This report provides a summary of the EMI results for the SX52BD. An independent EMI lab that specializes in EMI testing has taken all the measurements. Based on the results obtained, an analysis of the data is provided and overall PCB design guidelines are given so that the designer can minimize EMI before it becomes a problem.

1.1 Test Type

- Radiate Emissions

1.2 Package Types

- 52-pin PQFP

1.3 Device Operating Frequency

Measurements were taken using a 50 MHz crystal oscillator.

1.4 Test Board

The SX28AC/52BD Evaluation Board was used as the hardware platform for EMI measurements.The board contains the following:

- SX52BD/PQFP preprogrammed with following integrated Virtual Peripheral modules:
  - UART (with provision for RTS/CTS handshake lines)
  - I2C
  - 8-bit ADC
  - 8-bit PWM/PPM
- DB-9 serial port connector and RS-232 transceiver for connection to a terminal
- External serial EEPROM
- Four user pushbuttons and four user input DIP switches
- Eight active-high LEDs
- All on-board resources are jumpered to allow I/O relocation
- RESET button
- DC power-in plug e voltage source of 2.5V to 5.5V
- prototype area (1.5”x 3”)

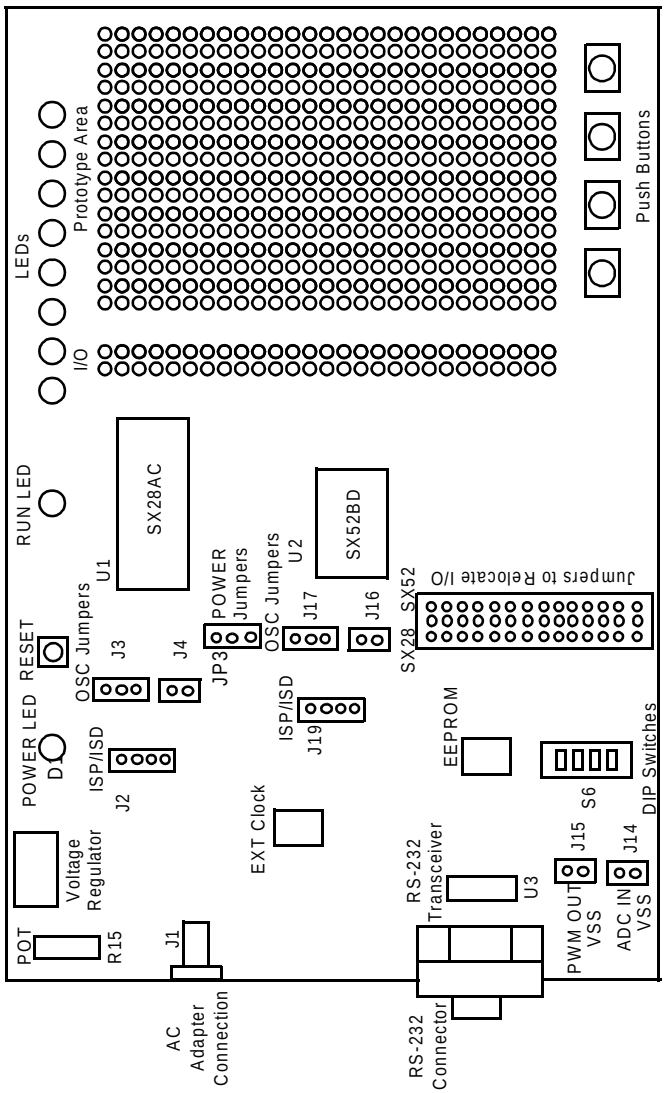

Figure 1-1. SX Evaluation Board

1.5 EMI Test Code

Several demonstration routines are integrated and programmed into the SX52BD device.The program performs the following functions:

- 16-bit timer - flashes the “RUN” LED to show program execution.
- PWM - The default value for the PWM is $bf (75% duty cycle). Pressing ‘P’ allows the entry of a new PWM high duty cycle value
- I2C EEPROM Interface - Upon power-up or reset, a test routine erases the first two locations at address $A0, writes to those location, and read the contents back. If the read value matches the value being written, “EEPROM OK” message will be displayed on the terminal. Otherwise, “Test Failed” will be displayed.
- DIP Switch - Upon power-up or reset, a routine reads the status of a 4-bit DIP switch and the result is displayed on the terminal.

1.6 Test Equipment

Semi-anechoic chamber, HP8591EM spectrum analyzer, and oscilloscope.

2.0 MEASUREMENT METHOD AND RESULTS

2.1 Measurement of Noise on the SX52BD

This report presents measurements of two forms of noise from the SX52BD device. The first is noise in the form of radiated emissions from the device and support circuitry on the evaluation circuit board. The board has an attached serial cable and a DC power cable. The test was conducted at the semi-anechoic chamber EMC test facility at Compaq Computer Corporation in Marlboro, Massachusetts. The test limit is the FCC Part 15 Class A and Class B limits. The test was conducted at the 3 meter distance and the measurement antenna was at a fixed height. The experience of the laboratory shows good correlation between results in the chamber versus open field measurements at the 10 meter distance. The graphs in Figures 2-1 and 2-2 show the emissions levels relative to the FCC Class A and Class B limits

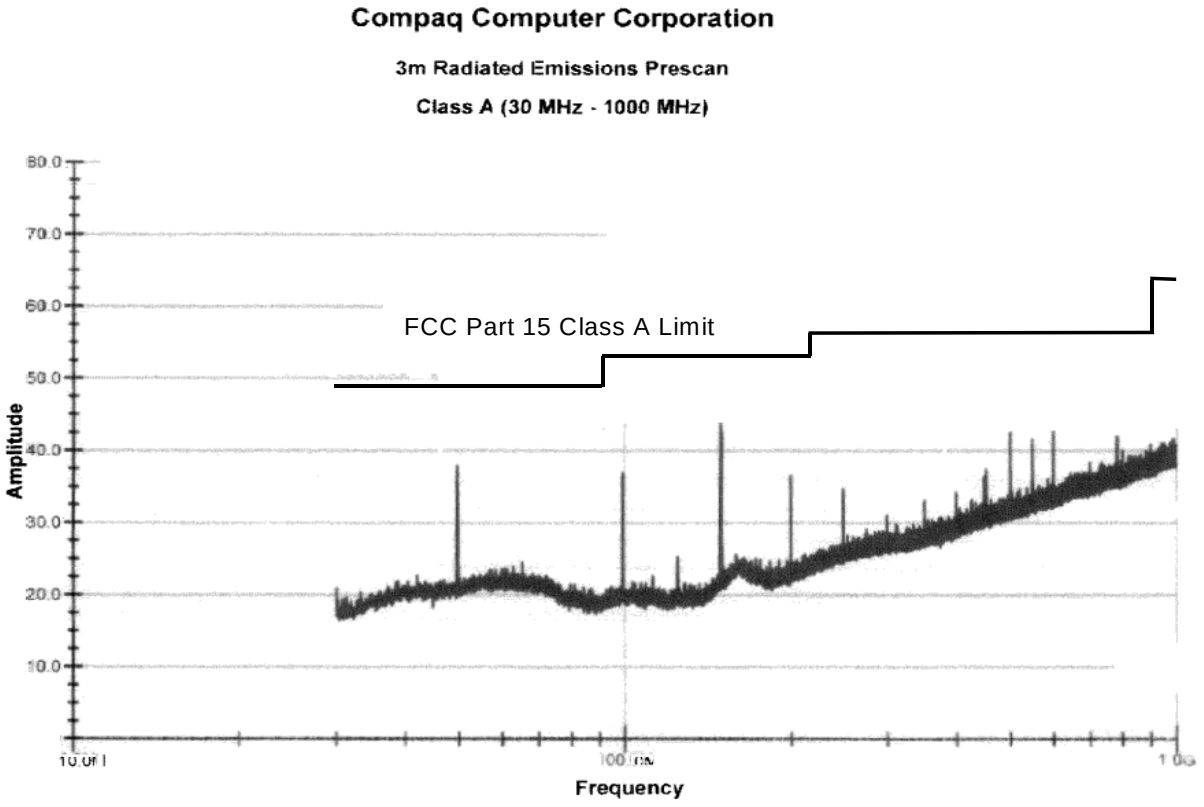

Figure 2-1. Radiated Emissions Relative to FCC Class A Limit

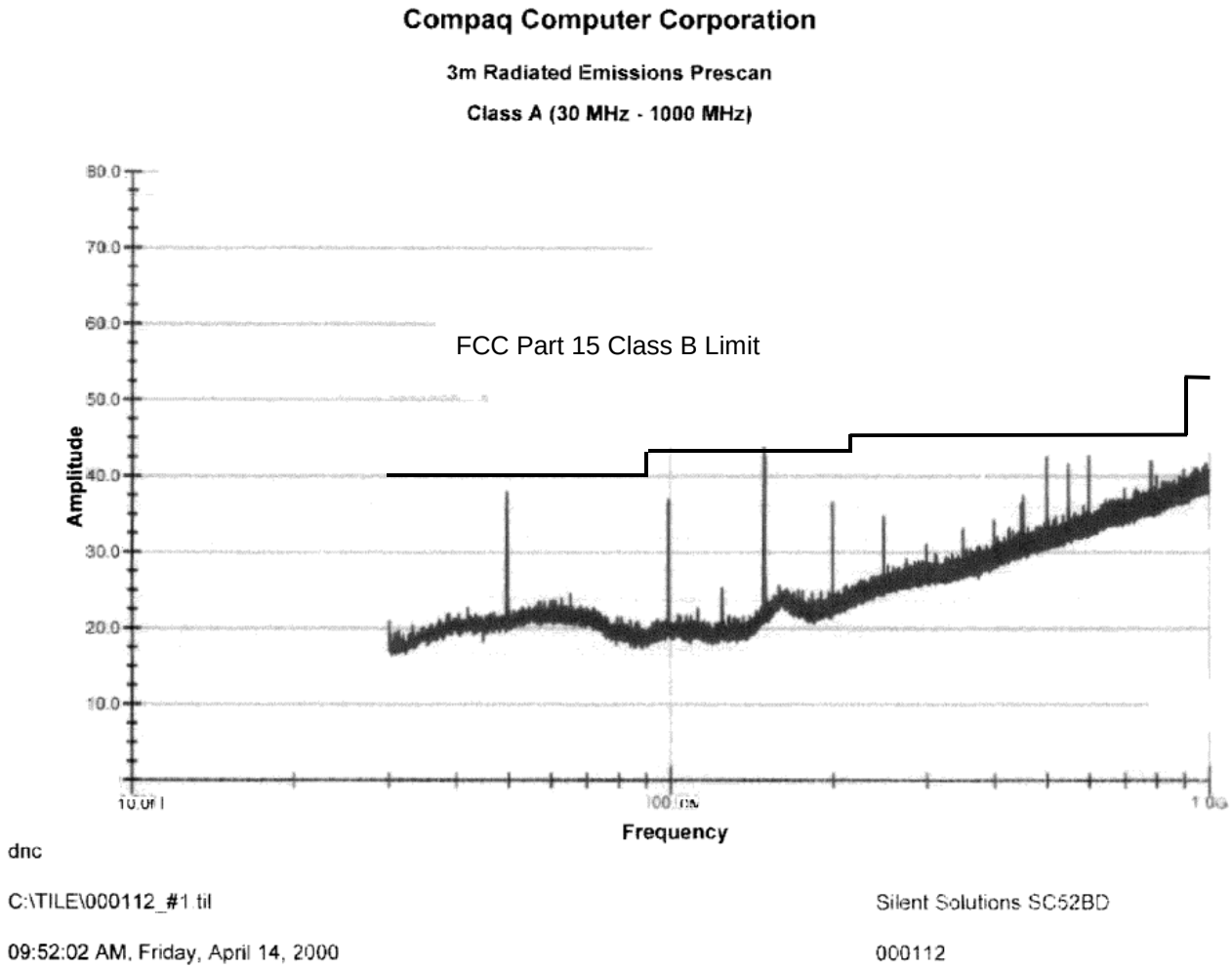

Figure 2-2. Radiated Emissions Relative to FCC Class B Limit

The second form of noise relates to circuit functionality. Low level analog or RF circuits associated with the SX52BD device can benefit functionally by having the device introduce to them as little noise as possible. Measurements were taken of noise on the power net of the device and the signal pins. Most of the signal pins were static. Most of the noise was due to the 50 MHz clock circuit. A low capacitance 10:1 FET probe with approximately 1.5 pF of loading was used to make noise voltage measurements. Noise measurements were taken in the frequency and time domains. An HP8591EM spectrum analyzer was used to measure a frequency range of 10 kHz to 500 MHz. Since a 10:1 probe is used a correction factor of 20*log(10:1) = 20dB is added to the values read in the following graphs. For example a measured value of 70 dBuVrms is actually 90 dBuVrms. The time domain measurements were made with a 350 MHz bandwidth oscilloscope. In correlating the time domain and frequency domain measurements, the frequency domain readings should be converted to peak-to-peak measurements.

The following example illustrates the process:

Assume the value from the graph is 70 dBuVrms. Adding the 20 dB probe correction factor yields 90 dBuVrms. Insert that value into the equation.

$$mVpp = 2.8 * 10^{-3} * 10^{dBuVrms/20}$$

$$mVpp = 2.8 * 10^{-3} * 10^{90/20}$$

$$mVpp = 88.5$$

Note that the time domain noise voltage is typically larger than the frequency domain measurement of a single spectral line. However, if all the spectral lines are combined with the appropriate phase information (which is not captured in these measurements) then both measurement methods would converge to the same result. If one spectral line dominates, then an approximation can be done which uses the one dominant line and ignores the rest.

The measurement flatness across the band is +/- 2 dB.

2.2 Frequency Domain Noise Measurements

Figure 2-3 shows the noise voltage on the SX52BD side of the power ferrite, FB4. Figure 2-4 shows the much lower noise on the power supply side of the ferrite bead. This demonstrates that noise produced by the SX52BD is being significantly attenuated by the ferrite bead and capacitor filter. The reduction is typically 10 dB and greater than 15 dB at the 50 MHz fundamental frequency.

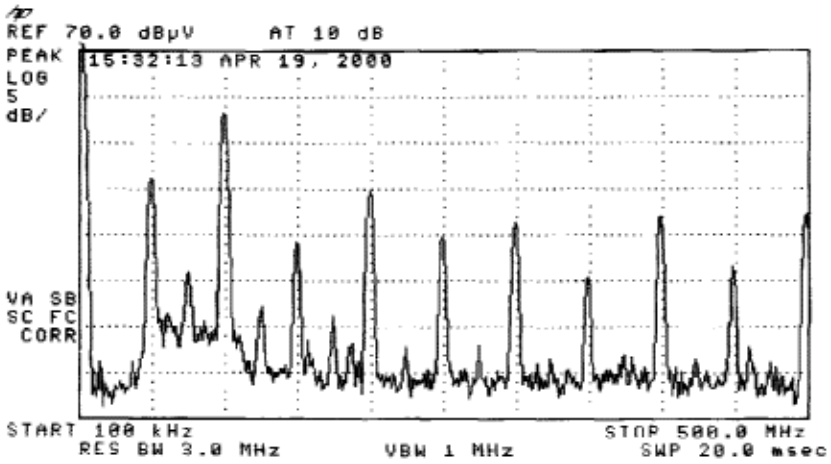

Figure 2-3. Noise on the SX52BD Side of the Vdd Ferrite Bead

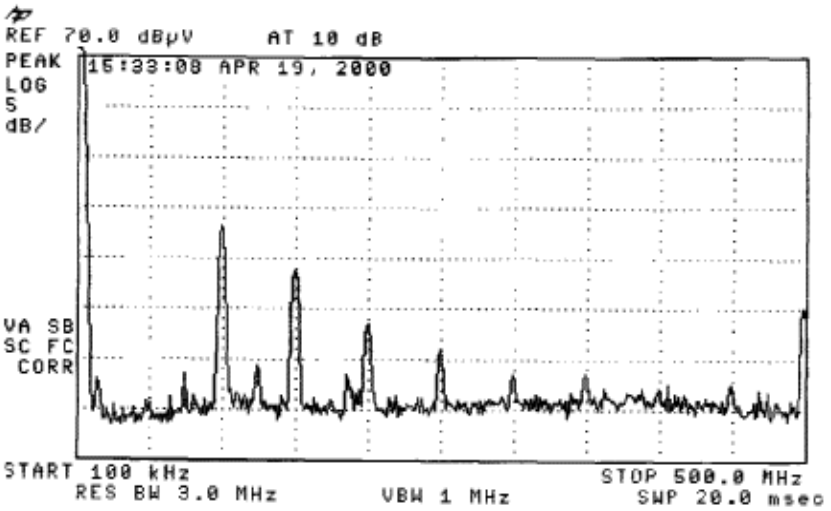

Figure 2-4. Noise on the Power Supply Side of the SX52BD Vdd Ferrite Bead

Figure 2-5 is a measurement of the noise voltage on power pin 20 of the SX52BD. It is a representative of all four power pins.

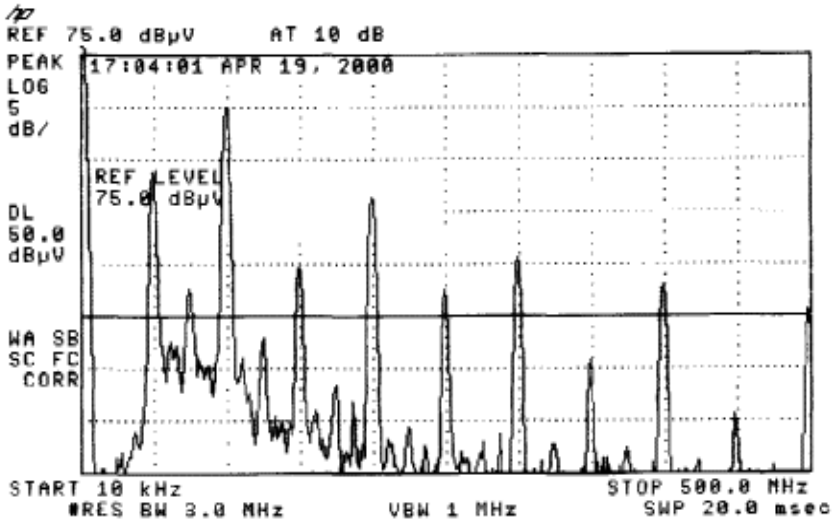

Figure 2-5. Typical Noise Voltage on SX52BD Power Pins

Figure 2-6 shows the noise on a typical non-toggling pin. This is for reference to upcoming plots of other static (non-toggling) pins that are more noisier.

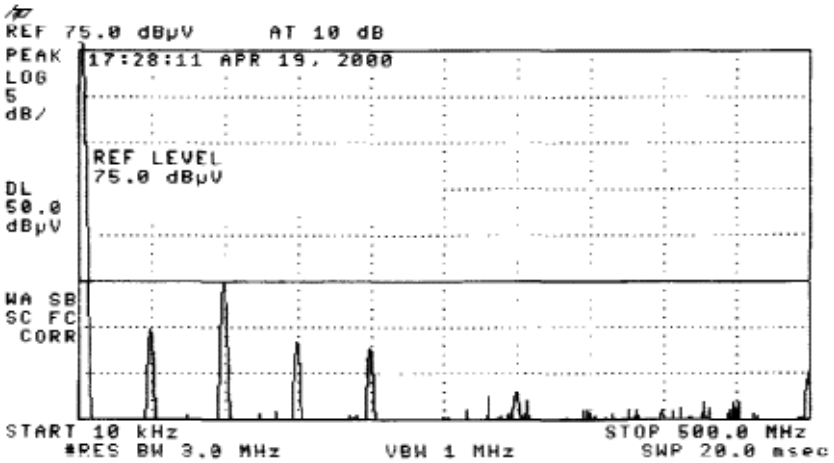

Figure 2-6. Noise Voltage on A Typical Non-Toggling Pin

Figure 2-7 shows the noise voltage on pin 11. The pin is at a logic high. It is noticeably noisier than other static pins.

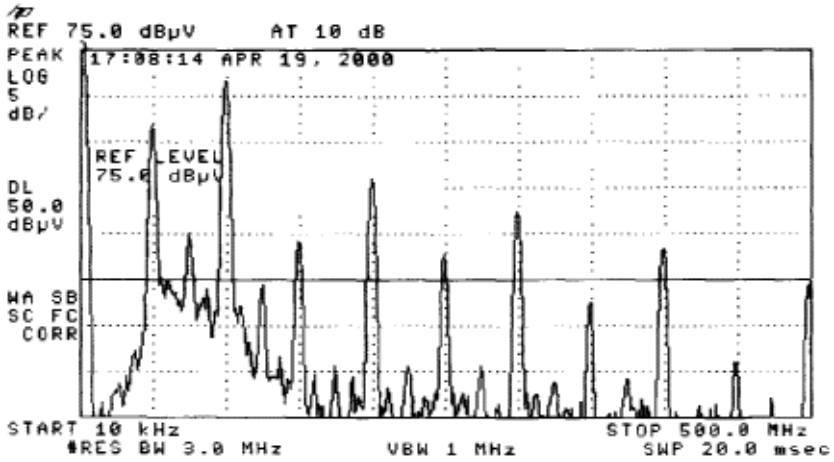

Figure 2-7. Pin 11 at Logic High

Figure 2-8 shows the noise on pin 26. It is similar to the noise on pins 27 and 29 which are not shown. All three pins are at a logic low and noisier than typical non-toggling pins.

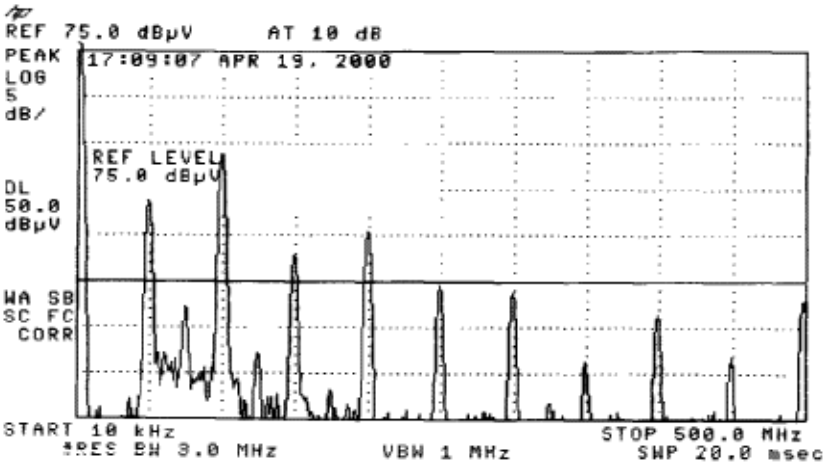

Figure 2-8. Pins 26/27/29 at Logic Low

Figures 2-9 and 2-10 show the noise on pins 44 and 45 which are toggling at rates of approximately 1 kHz and 100 kHz respectively.

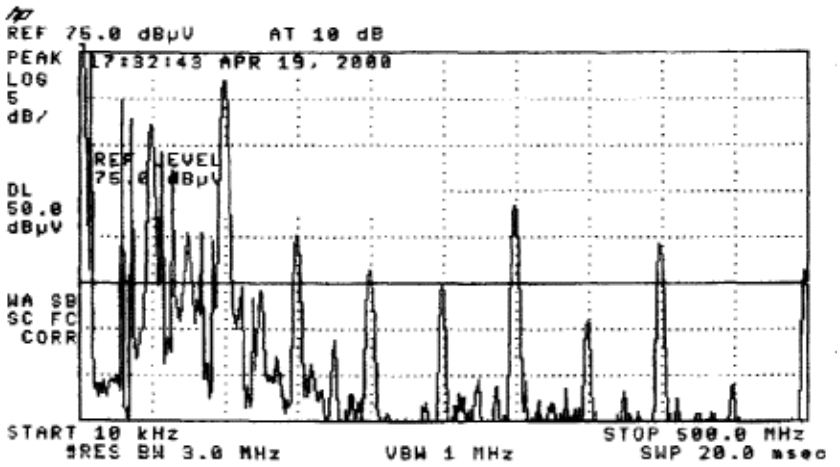

Figure 2-9. Pin 44 Toggling at 1 kHz

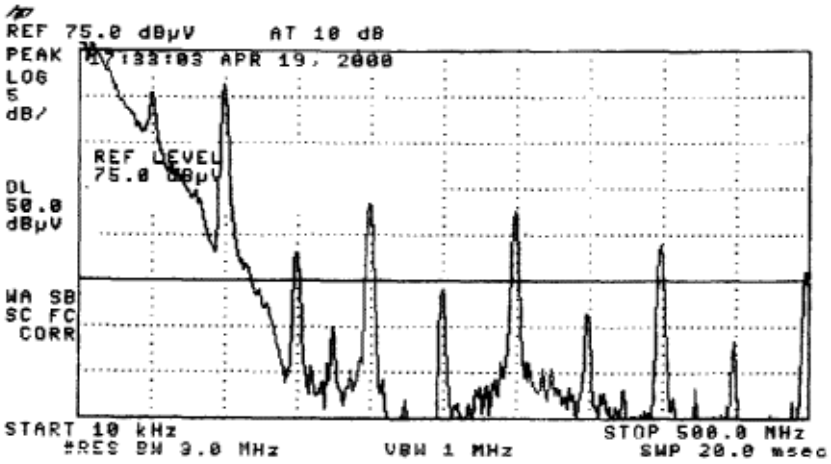

Figure 2-10. Pin 45 Toggling at 100 kHz

Figures 2-11 and 2-12 show the noise on pins 46 and 47. The signals are 2.5 volt DC and an approximately 5 Hz squarewave respectively.

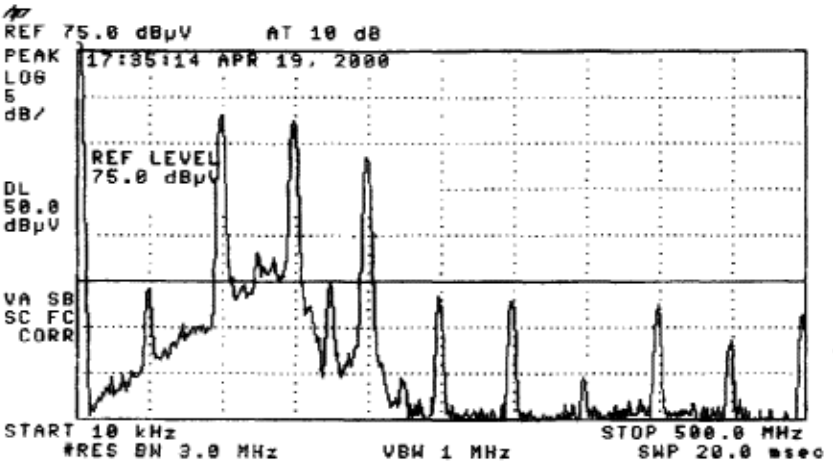

Figure 2-11. Noise Voltage on Pin 46 (static at 2.5V DC)

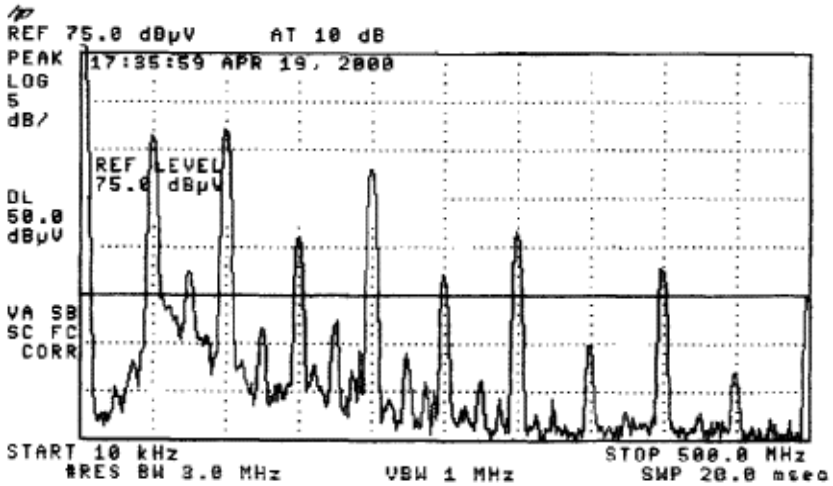

Figure 2-12. Noise Voltage on Pin 47 Toggling at 5 Hz

Figures 2-13 and 2-14 show the noise voltage on pins 51 and 52. They are at logic low.

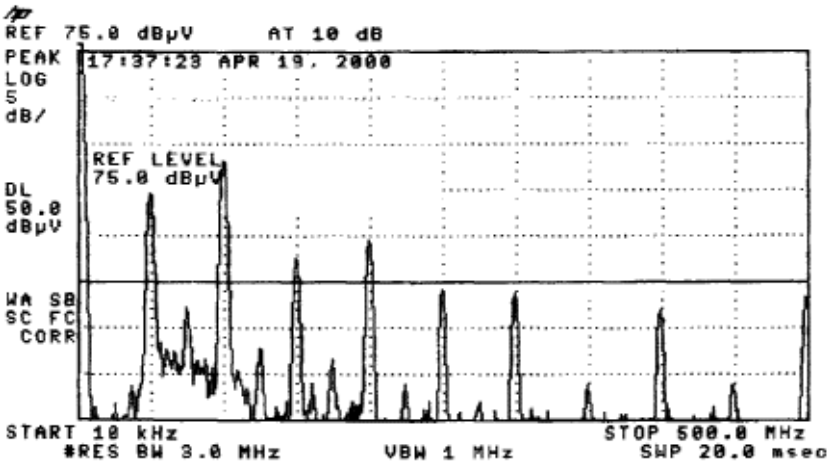

Figure 2-13. Pin 51 at Logic Low

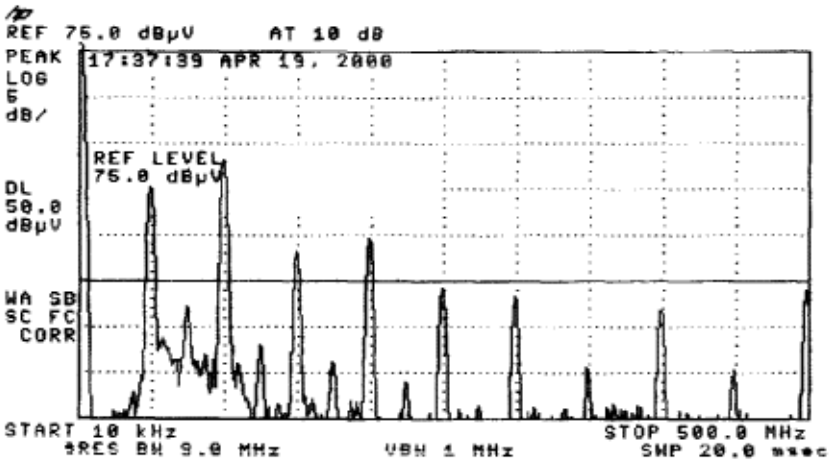

Figure 2-14. Pin 52 at Logic Low

Figure 2-15 is the clock signal on pin 5. The scale of the graph has been changed to 10 dB per division and the fundamental peak is approximately 123dBuVrms (includes 20 dB probe correction factor). This is nominally a sinewave signal and thus the harmonics are relatively low with respect to the fundamental.

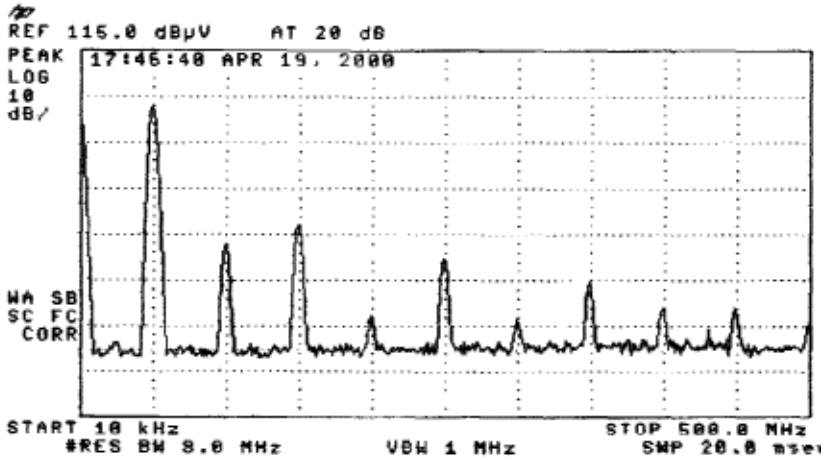

Figure 2-15. Pin 5 Sinewave Oscillator (10 dB/division)

2.3 Time Domain Noise Measurements

Table 2-1 indicates the peak to peak noise voltage on the pins as measured with a wideband oscilloscope and low capacitance FET probe.

Table 2-1. Noise Voltage at Various Pins

Pin	Signal	Noise Voltage (mVpp)
Typical non-toggling	Logic low or high	25
5	5 Vpp sinewave	N/A
11	High	270
26 (27 and 29)	Low	110
44	1 kHz	250
45	100 kHz	500
46	2.5 DC	175
47	5 Hz	200
51	Low	100
52	Low	100

3.0 ANALYSIS OF THE RESULTS

1. Near field probing indicates that modulation of the power supply lines by high frequency switching in the SX device is reduced due to placement of Vdd and Vss pins close to each other and on one side of the package. This leads to a small trace length to the decoupling capacitor and also the smallest radiating area.
2. The rise and fall times of the port drivers seem to be low enough to keep the radiated interference at reduced level due to port switching. Measurements were taken with the device being held in RESET and the results were compared with emission levels obtained during output switching. No significant difference was observed. Typically CMOS output stages may cause “shoot through” current to be drawn when switching, if the high-side and low-side drivers are both on at the same time. The SX I/O ports have slew rate control (gradual turn on) circuitry that helps control the “shoot through” effect.
3. The maximum emission levels are observed at the harmonics of the operating frequency. For example, for an operating frequency of 50 MHz, the peak emission level is at 100 MHz, 150 MHz, etc.

4.0 GENERAL GUIDELINES FOR PCB LAYOUT AND CONSTRUCTION

4.1 Suppression of Interference on the Supply Line

1. Current and voltage peaks are the most common causes of EMI. Use of proper decoupling capacitors between Power and Ground at the power source to the board as well as on the SX Vdd and Vss pins may help. It is also important to evaluate the proper capacitor type, frequency response, placement, output load effect, and size.
2. The decoupling capacitor by itself may not be able to significantly reduce the radiated interference. Because the inductance causing the interference has already been formed, to a large extent by the packages of the ICs and the connection to the capacitor, significant improvement cannot be achieved by simply connecting in parallel several capacitors of different values. Of greater concern is preventing the current causing the disturbance from reaching the other parts of the circuit. This can be achieved by introducing an inductor behind the decoupling capacitor, which represents a sufficiently high resistance at high frequencies. The impedance of the inductor could be limited at high frequencies by a resistor of 50 Ohm connected in parallel to the inductor. A more cost effective approach is to run a small trace from Vdd to a capacitor, and a larger trace from the capacitor to the SX device.
3. Experiments during measurements indicate that using small ferrite beads at the power source to the board and/or at the point where power is supplied to the SX52BD, may significantly reduce excessive emissions.

4.2 Reducing the Power and Ground Loop Area

The long supply lines with the relatively large areas that these lines surround may form an effective antenna. At the frequencies present, an unacceptable level of interference may be radiated. A grounded area under the SX device must be connected to the Vss pin. In addition, the ground area should be tied to the ground plain with multiple vias. This ground area ensures that the major part of the field lines emanating from the SX are concentrated between the SX and the ground level.

4.3 Oscillator Considerations

1. The oscillator circuit needs to be analyzed with respect to the flow of significant current to determine where the interference suppression is necessary.
2. Avoid large ground loop in the oscillator circuit area. This large loop will result in larger amount of current flow in the oscillator resonant circuit. The creation of a ground plane underneath the chip (mentioned above to reduce the power line loop) will help shorten the loop effect. In addition, it will be useful to run the capacitor ground connection close and in parallel to the clock input and output signals. If ground area underneath the chip is not available, the capacitor should be directly connected to the SX ground pin through a short and independent trace.
3. The shape of the oscillator signal should be observed with a low capacitance FET probe to identify any ringing. The oscillator signal should look smooth. Impedance matching techniques can be employed to smoothen the oscillator signal.

4.4 Handling I/O Signals

1. High speed signals should be close to the ground plane or ground signals. High speed signal wires and their returns should be as short as possible and put in the smallest possible area. As mentioned in Section 3.0, the SX output drivers have slew rate control (gradual turn on), it may still be beneficial to slow I/O pin transition further by adding capacitors on the I/O pins. This is useful in applications that involve large amount of data transfer into/out of the SX device. Filtering noise from output pins can be done effectively with a small value capacitor such as 10 - 47 pF to ground on the noisy pins. If additional filtering is required a series resistor in the range of 33 to 68 ohms followed by a capacitor to ground can be used. This provides a 3 dB cutoff frequency in the range of 50 MHz (68 ohms) to 100 MHz (33 ohms). Significantly lower cutoff frequencies can be achieved by increasing the capacitor value. For a simple RC filter the cutoff frequency is:

$$f = \frac{1}{2\pi RC}$$

   A 1 MHz logic signal will typically perform acceptably in logic circuits with a bandwidth of 10 MHz. In this case, a 68 ohm resistor followed by a 240 pF capacitor to ground provides a 10 MHz filter. The digital circuit functionality should be verified to insure that logic timing is acceptable.
2. High speed signals should be shielded and kept away from other signals, in order to avoid crosstalk, particularly on high resistance and level sensitive tracks. The tracks should be routed sufficiently far apart or run parallel to a track connected to the system reference voltage, usually ground, to provide shielding.

4.5 General Considerations

1. If the PCB contains both analog and digital circuits, there should be separate analog and digital power supplies and grounds.
2. Single point connection of tracks for analog ground and power supply. In order to avoid different potentials a galvanic connection at only one point is desirable. Track loops should be avoided (also less susceptible to interference).
3. Large ground plane. If the size of the ground plane is increased, the radiating area due to current loops will be reduced. Additionally, the capacitance to ground of the digital lines is increased which could lead to an increase in the interference caused by switching currents.
4. Low inductance connections. The use of short connecting wires results in a reduction of any inductive voltage spikes as Vi = L*di/dt at constant di/dt when switching.
5. If the board physical layout permits, it is beneficial to keep the power connector (power source to the board) and other connectors (such RS-232) on the same side of the board.
6. On a two-sided board, if the back side is copper poured, try to keep this side free of components, traces, and “cuts” as much as possible to leave more ground metal area.
7. Using a multi-layer board can lead to reduction in emitted interference. The improvement is due to the reduction in track length and the reduction of Vdd to ground impedance, for example if Vdd/Ground grid is used.

Lit #: SXL-AN34-01

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