SX18/20/28AC to SX48/52BD Conversion

SCENIX

Application Note 15
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1.0 Overview

Although the SX18/28AC and SX48/52BD share the same basic architecture, there are numerous minor changes which the designer should be aware of. This document will help the designer to understand the differences between these variants of the SX family, and the software changes that may need to be implemented.

1.1 SX48/52 MODIFICATIONS

The SX48/52 expands on the same basic architecture as the SX18/28, sharing an identical instruction set and feature set, with the following additional features and modifications:

- 4Kx 12 bits EE/Flash program memory rated for 10000 rewrite cycles
- 262 x 8 bits SRAM
- 5 8-bit ports on SX52; 1 4-bit, 4 8-bit ports on SX48
- Two 16-bit timers with 8-bit prescalers supporting:
  - Software Timer mode
  - PWM mode
  - Simultaneous PWM/Capture mode
  - External Event mode
- Port LVL, PLP, ST, and Direction registers are read/write
- RTCC interrupt flag
- Ability to disable clock during SLEEP mode
- Selectable delay reset timeout period (DRT)

Please consult the SX48/52 datasheet for more details on all the SX48/52 features.

Note:There are some additional features which will be made available in the production released revision of SX48/52. Please see section 3.0 for more details on these improvements.

1.2 CONVERSION

Almost all software written for the SX18/28 can be converted for use on the SX48/52 with only minor modifications. Please be advised that object code compiled specifically for the SX18/28 will not operate on the SX48/52, as the FUSE and FUSEX registers do not have a compatible arrangement.

1.3 MODE REGISTER

The MODE register value on the SX48/52 has been expanded to use 5 bits. This provided the additional address pointers to include read capability for the port ST, LVL, PLP, and direction registers. In the SX18/28, the MODE register address pointer only required 4 bits and the following instruction alone could be used to modify the MODE register:

```
mov M,#
```

With SX48/52 however, this instruction will not modify all 5 bits of the MODE register to correctly point to entire range of registers pointed to by MODE, as the mov M,# instruction only has a 4-bit operand. When all 5-bits of the MODE register need to be modified, the following instructions should instead be used:

```
mov W,#
mov M,W
```

This will ensure that all 5-bits of the MODE address pointer are written.

1.4 DEVICE CONFIGURATION REGISTERS

The SX device has 2 registers (FUSE and FUSEX) that are used to configure various optional modes of operation.

The SX48/52 have different FUSE and FUSEX bit assignments from SX18/28. Depending on the assembler or tool used, the directives, device configuration or FUSE/FUSEX assignment will need to be modified. For this reason, all object targeted for SX18/28 will need to be re-compiled with SX48/52 as the target device.

Note:The FUSE and FUSEX assignment directives vary depending on the tool vendor, and assembler being used. Please consult your assembler software manual for details on the different directives for each SX device.

1.4.1 SX48/52 FUSE Word (Read/Program at 1FFFh in main memory map)

$\overline{\text{TURBO}}$	$\overline{\text{SYNC}}$	$\overline{\text{OPTIONX}}$	$\overline{\text{STACKX}}$	$\overline{\text{IRC}}$	DIV2	DIV1	DIV0	$\overline{\text{CP}}$	WDTE	FOSC1	FOSC0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

$\overline{\text{TURBO}}$ Turbo mode enable:
- 0 = turbo mode (instruction clock = osc/1)
- 1 = compatible mode (instruction clock = osc/4)

$\overline{\text{SYNC}}$ Synchronous input enable (for turbo mode):
- 0 = enabled
- 1 = disabled

$\overline{\text{OPTIONX}}$ OPTION register extension enable:
- 0 = OPTION register increased from six to eight bits for RTW and RTW_IE
- 1 = OPTION register is six bits (two most significant bits forced to 1)

$\overline{\text{STACKX}}$ Stack extension enable:
- 0 = 8 levels (stack extension enabled)
- 1 = 2 levels (stack extension disabled)

$\overline{\text{IRC}}$ Internal RC oscillator enable:
- 0 = enabled - OSC1 weakly pulled low, OSC2 weakly pulled high
- 1 = disabled - OSC1 and OSC2 behave according to FOSC1: FOSC0

DIV2: DIV0 Internal RC oscillator divider:
- 000b = 4 MHz
- 001b = 2 MHz
- 010b = 1 MHz
- 011b = 500 KHz
- 100b = 250 KHz
- 101b = 125 KHz
- 110b = 62.5 KHz
- 111b = 31.25 KHz

$\overline{\text{CP}}$ Code protect enable:
- 0 = enabled (FUSE, code, and ID memories read back as garbled data)
- 1 = disabled (FUSE, code, and ID memories can be read normally)

WDTE Watchdog timer enable:
- 0 = disabled
- 1 = enabled

FOSC1: FOSC0 External oscillator configuration (valid when IRC = 1):
- 00b = LP – low power crystal
- 10b = HS – high speed crystal
- 01b = XT – normal crystal
- 11b = RC network - OSC2 is pulled high by a weak pullup(no CLKOUT output)

1.4.2 SX48/52 FUSEX Word (Read/Program via Programming Command)

SLEEPCLK	WDRT2 : WDRT0			$\overline{CF}$	IRCTRIM2 : IRCTRIM0			Unused		BOR0:BOR0	
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

SLEEPCLK — Sleep Clock Disable. Clear this bit to 0 to enable operation of the clock during power down mode (to allow fast start-up). Set this bit to 1 to disable clock operation during power down mode (to reduce power consumption).

WDRT2: WDRT0 — Delay Reset Timer (DRT) timeout period. This 3-bit field can be used to specify the DRT timeout period that results in an automatic wake-up from the power down mode:

100 = 0 msec (no delay)
101 = 0.06 msec
110 = 7.68 msec
111 = 18.4 msec (default)
000 = 60 msec
001 = 480 msec
010 = 960 msec
011 = 1920 msec

For fast start-up from the power down mode, clear the SLEEPCLK bit and set the WDRT2:WDRT0 field to 100. This will keep the clock operating during the power down mode and allow a zero start-up delay.

$\overline{CF}$ — active low – makes the carry flag an input to ADD and SUB instructions.

IRCTRIM2: IRCTRIM0 — Internal RC Oscillator Trim. This 3-bit field adjusts the operation of the internal RC oscillator to make it operate within the target frequency range of 4.0 MHz plus or minus 8%. Parts are shipped from the factory untrimmed. The device relies on the programming tool to provide trimming.

000b = minimum frequency

111b = maximum frequency

each step approx. 3%

BOR1: BOR0 — Brown-Out Reset; factory preset values. Bits should not be changed unless brown-out feature is to be disabled.

00b = brown-out enabled

01b = (reserved)

10b = (reserved)

11b = brown-out disabled

1.4.3 FUSE/FUSEX changes

There are some additional features which will be made available in the production released revision of SX48/52, including a change to the arrangement of the FUSE and FUSEX bit assignments. Please see section 3.0 for more details on these improvements.

1.5 DATA MEMORY

The data memory is a RAM-based register set consisting of 262 general-purpose registers and nine special-purpose registers. All of these registers are eight bits wide.

The data memory is organized into 16 banks, designated Bank 0 through Bank F, each containing 16 registers, plus an additional bank of 16 “global” registers. Because the registers are organized into banks or “files,” these memory-mapped registers are called “file registers.”

1.5.1 Addressing Modes

Each SX instruction that accesses a data memory register contains a 5-bit field in the instruction opcode that specifies the register to be accessed. The abbreviation “fr” represents the 5-bit register address designator. For example, the instruction description “mov fr,W” means that a 5-bit value or label must be substituted for “fr” in the instruction, such as “mov $0F,W” (to move the contents of the working register W into file register 0Fh).

There are three different addressing modes, called the indirect, direct, and semi-direct modes. The addressing mode used for register access depends on the 5-bit “fr” value used in the instruction:

- indirect mode: fr = 00h
- direct mode: fr = 01h through 0Fh
- semi-direct mode: fr = 10h through 1Fh

For indirect addressing (fr=00), the File Select Register (FSR) specifies the register to be accessed. FSR is an 8-bit, memory-mapped register (at address 04h) which serves as an 8-bit pointer into data memory for indirect addressing. In this mode, the global register bank and Bank 1 through Bank F are accessible. Bank 0 is not accessible.

For direct addressing (fr=01-0F), the value of “fr” itself specifies the register to be accessed, and the FSR register is ignored. For this addressing mode, only the global register bank is accessible. To gain access to any other bank, you must use either indirect or semi-direct addressing.

For semi-direct addressing (fr=10-1F), the bank number is selected by the four high-order bits of FSR, and the register within that bank is selected by the four low-order bits of “fr.” In other words, the register address is obtained by combining the four high-order bits of FSR with the four low-order bits of “fr”. In this addressing mode, the low-order bits of FSR are ignored. Bank 0 through Bank F are accessible, but the global register bank is not accessible.

Figure 1-1 shows how register addressing works in the indirect, direct, and semi-direct modes. The 16 global registers are always accessible by direct addressing, regardless of what is contained in the FSR register. The global registers are also accessible with indirect addressing, but they are not accessible with semi-direct addressing. Of the 16 global registers, nine are special-purpose registers (RTCC, PC, STATUS, and so on), and six are general-purpose registers. Location 00 is used for indirect addressing (INDF). All of the registers in Bank 0 though Bank F are general-purpose registers.

1.5.2 SFRs and Globals

The SX48/52 have all the same special-function registers as the SX18/28 devices. The SX48/52 however, feature two additional I/O ports, RD and RE, which correspond to addresses $08 and $09 respectively. For this reason, user-assignable global memory starts from address $0A, instead of $08 on the SX18/28. Therefore, there are only 6 user-assignable global data memory locations available instead of the 8 locations available on SX18/28 - some code may need to be rewritten to limit the use of global memory locations.

1.5.3 BANK switching

In order to access data memory locations across other banks, the upper 4-bits of the FSR serve as a pointer to the current bank being accessed. To change the contents of the FSR register, the program can either write an eight-bit value to the FSR register or use the “bank” instruction. The BANK instruction writes the three high-order bits in the FSR register, and clears bit 4 of the FSR. Thus, the BANK instruction alone,

```
bank $20
```

lets you quickly change from one even-numbered bank to another (banks $00, $20, $40, $60, $80, $A0, $C0, $D0 and $F0). To change from one odd-numbered bank to another, FSR bit 4 must be set immediately following the BANK instruction as below.

```
bank $10
sb FSR.4
```

Careful consideration must always be paid to the correct handling of bit 4 in the FSR to ensure that you are pointing to the correct data memory bank.

Note:The BANK instruction will be modified in the production released revision of SX48/52 to help alleviate some of difficulty surrounding bank switching. Please see section 3.0 for more details on these improvements.

1.5.4 BANK 0 Considerations

BANK 0 (data memory address $00 - $0F) shares the same physical addresses as the SFR registers so deserves special attention. BANK 0 can only be accessed via semi-direct addressing, where bit 4 of the operand address must be set, so the operand address created on assembly should be in the range $10 - $1F. The upper 4-bits of the FSR would also need to be cleared.

Since BANK 0 cannot be accessed via direct or indirect addressing modes, some tool vendors may choose not to support this register bank in debug mode. Please consult your tool vendors documentation for more information on this limitation.

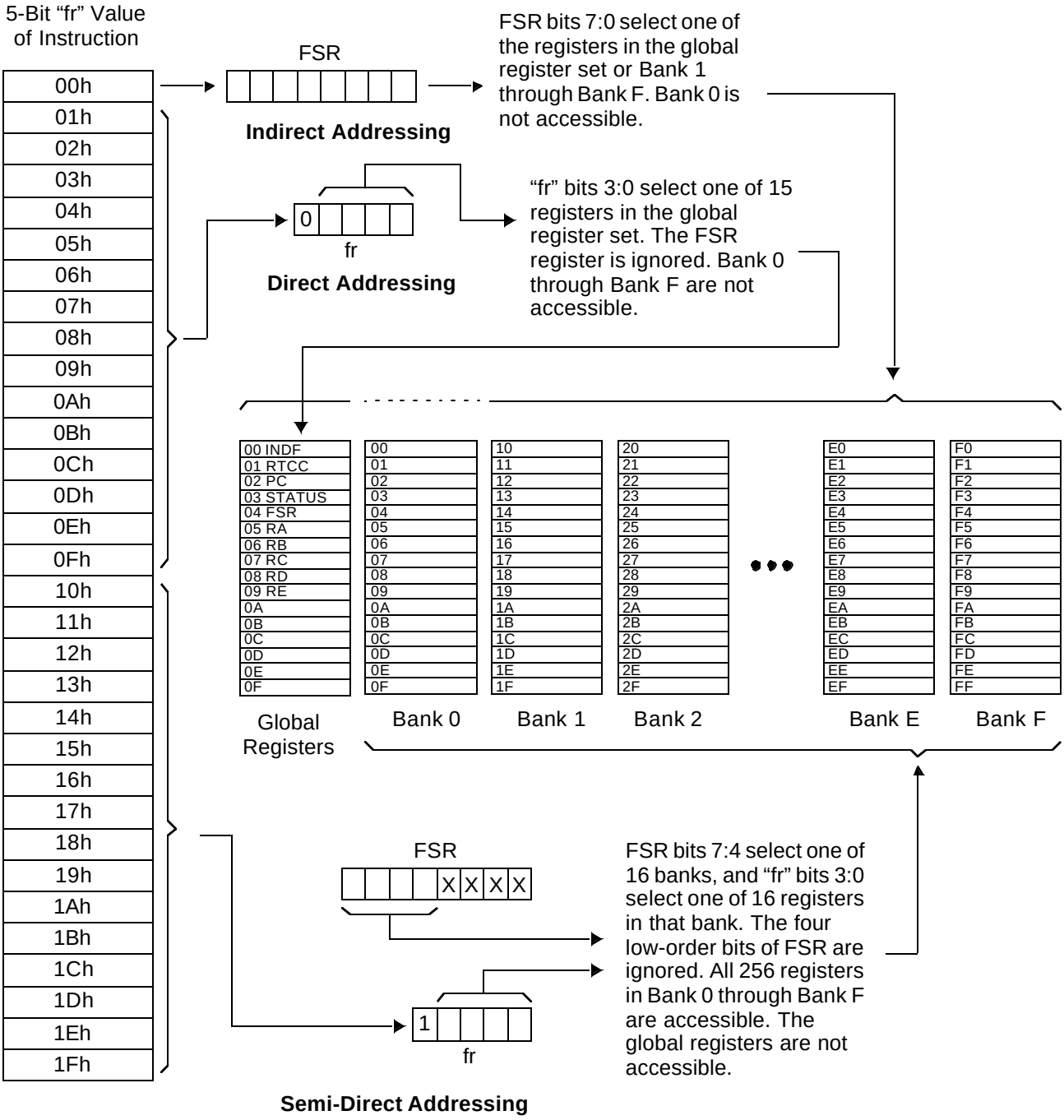

Figure 1-1. Register Access Modes

2.0 SX48/52BD Additional Features

There are several new features specific to the SX48/52 that were not available in previous members of the SX family.

2.1 MULTI-FUNCTION TIMERS

Two additional 16-bit timers with 8-bit prescalers with the following operating modes have been implemented:

- Software Timer mode
- PWM mode
- Simultaneous PWM/Capture mode
- External Event mode

Please consult the SX48/52 datasheet for more details on all the SX48/52 features.

2.2 INTERRUPT SOURCES

In addition to the internal Real-Time Clock/Counter (RTCC) interrupt and the external PORT B interrupts, timers T1 and T2 each has three interrupt sources associated with counter overflow, compare match, and input capture. As there is still only one interrupt vector, special attention must be paid to determining the source of interrupt at the beginning of the interrupt service routine (ISR) if multiple sources are enabled. The handling of these interrupts may induce jitter in the timing of Virtual Peripheral™ modules if the RTCC interrupt is enabled along with other interrupt sources.

An RTCC Overflow Flag bit (RTCCOV) has also been added, and contained in the T1CNTB register. This flag is automatically set to 1 when the RTCC overflows from FFh to 00h. This flag stays set until it is cleared by the software. Note that this flag is not related to multi-function timers T1 and T2.

2.3 PORT READ FEATURE

Reading from a data register reads either the voltage levels of the corresponding port pins or the data contained in the port data register depending on the status PORTRD bit contained in the T2CNTB register.

2.4 DELAY RESET TIMER (DRT)

The FUSEX register contains this 3-bit field which can be used to specify the DRT timeout period that results in an automatic wake-up from the power down mode. Timeout periods of 0, 0.06, 7.68, 18.4, 60, 480, 960 or 1920 msec can be selected.

Note:The DRT timeout period is based on the internal watchdog oscillator clock, so these timeout periods are fixed regardless of the external oscillator clock speed.

2.5 SLEEP CLOCK DISABLE

This FUSEX bit allows the ability to enable the operation of the clock during power down mode to allow fast start-up. Set this bit to 1 to disable clock operation during power down mode (to reduce power consumption).

3.0 SX48/52 Production Release

The production release of SX48/52 will have some features modified either for compatibility with existing SX18/28 devices or as enhancements.

These include:

- Modification of FUSE and FUSEX bit arrangement and features for maximum compatibility with existing SX18/28 devices or enhanced features
- Removal of PIC 'compatible' features:
  - fixed 1:1 instruction:clock ratio
  - fixed 8-level stack
  - full 8-bit OPTION register
- Same OSC circuitry and settings as existing SX18/28 devices
- Selectable BOR threshold
- Modification of DRT timeout period setting for compatibility with existing SX18/28 devices
- Improved BANK instruction operation

3.1 SX48/52 FUSE WORD (READ/PROGRAM AT 1FFFH IN MAIN MEMORY MAP)

Unused	$\overline{\text{SYNC}}$	Unused	$\overline{\text{IRC}}$/XTL	DIV1/$\overline{\text{IFBD}}$	DIV0/FOSC2	$\overline{\text{XTLBUF\_EN}}$	$\overline{\text{CP}}$	WDTE	FOSC1	FOSC0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

$\overline{\text{SYNC}}$ Synchronous output enable (output transition only on clock edge)
- 0 = enabled
- 1 = disabled

$\overline{\text{IRC}}$ Internal RC oscillator enable
- 0 = enabled - OSC1 weakly pulled low, OSC2 weakly pulled high
- 1 = disabled - OSC1 and OSC2 behave according to FOSC2:FOSC0

DIV1:DIV0 Internal RC oscillator divider
- 00b = 4 MHz
- 01b = 1 MHz
- 10b = 128 KHz
- 11b = 32 KHz

$\overline{\text{IFBD}}$ Internal crystal/resonator oscillator feedback resistor
- 0 = Internal feedback resistor disable (external feedback required for crystal operation)
- 1 = Internal feedback resistor enabled (valid when IRC = 1)

$\overline{\text{XTLBUF\_EN}}$ Crystal Buffer enable (disable when not using a crystal to reduce Idd)
- 0 = Crystal Buffer enabled
- 1 = Crystal Buffer disabled

$\overline{\text{CP}}$ Code protect enable
- 0 = enabled (FUSE, code, and ID memories read back as scrambled data)
- 1 = disabled (FUSE, code, and ID memories can be read normally)

WDTE Watchdog timer enable
- 0 = disabled
- 1 = enabled

FOSC2:FOSC0 External oscillator configuration (valid when $\overline{\text{IRC}}$ = 1):
- 000b = LP1 – low power crystal (32KHz)
- 001b = LP2 – low power crystal (32KHz - 1MHz)
- 010b = XT1 – normal crystal (32KHz - 10MHz)
- 011b = XT2 – normal crystal (1MHz - 24MHz)
- 100b = HS1 – high speed crystal (1MHz - 30MHz)
- 101b = HS2 – high speed crystal (1MHz - 50MHz)
- 110b = HS3 – high speed crystal (1MHz - 50MHz)
- 111b = External RC network - OSC2 is pulled high by a weak pullup(no CLKOUT output)

3.2 SX48/52 FUSEX WORD (READ/PROGRAM VIA PROGRAMMING COMMAND)

IRCTRIM2	SLEEPCLK	IRCTRIM1:IRCTRIM0	Unused	$\overline{CF}$	BOR1:BOR0	BORTR1:BORTR0	DRT1:DRT0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

IRCTRIM2: IRCTRIM0 — Internal RC Oscillator Trim. This 3-bit field adjusts the operation of the internal RC oscillator to make it operate within the target frequency range of 4.0 MHz plus or minus 8%. Parts are shipped from the factory untrimmed. The device relies on the programming tool to provide trimming.

000b = minimum frequency

111b = maximum frequency

$\overline{SLEEPCLK}$ — Sleep Clock Disable.

0 = enable operation of the clock during power down mode (to allow fast start-up).

1 = disable clock operation during power down mode (to reduce power consumption).

$\overline{CF}$ — Carry Flag ADD/SUB enable

0 = carry bit input to ADD and SUB instructions.

1 = ADD and SUB without carry

BOR1: BOR0 — Sets the Brown Out Reset threshold voltage

00b = 4.2V

10b = 2.6V

01b = 2.2V

11b = BOR disabled

BORTR1: BORTR0 — Brown-Out trim bits (parts are shipped out of factory untrimmed).

00b = minimum threshold voltage

11b = maximum threshold voltage

DRT1:DRT0 — Delay Reset Timer (DRT) timeout period

10b = 0.06 msec

11b = 18.4 msec

00b = 60 msec

01b = 960 msec

3.3 BANK SWITCHING

The BANK instruction will be modified to provide better access to all 16 data memory banks with maximum software efficiency.

In the production release revision of SX48/52, the upper 4-bits of the FSR will still serve as a pointer to the current bank being accessed. The BANK instruction however, will only modify FSR bits 4, 5 and 6, without affecting the other bits in the register. This will break up the data memory banks into upper and lower blocks, with a single BANK instruction allowing you quickly change from one upper bank to another, or from lower bank to another. FSR bit 7 will need to be modified by the user to switch from an upper to a lower bank (or vice-versa). This allows the maximum number of register banks to be available with a single BANK instruction, while using the FSR to indirectly address another block of addresses, as well as a more ‘intuitive’ data memory arrangement.

Lit #: SXL-AN15-03

Sales and Tech Support Contact Information

For the latest contact and support information on SX devices, please visit the Scenix Semiconductor website at www.scenix.com. The site contains technical literature, local sales contacts, tech support and many other features.

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