Cypress MicroSystems
M8C Instruction Set Summary

Program Flow Instructions

				Flags	Cycles
CALL		**Call (relative)**			
9xh	CALL addr	LSB Address Byte (MSN in opcode, x)			11
HALT		**Halt**			NA
30h	HALT				
JACC		**Jump Accumulator (relative)**			
Exh	JACC addr	LSB Address Byte (MSN in opcode, x)			7
JC		**Jump if Carry (relative)**			
Cxh	JC addr	LSB Address Byte (MSN in opcode, x)			5/4
JMP		**Jump (relative)**			
8xh	JMP addr	LSB Address Byte (MSN in opcode, x)			5
JNC		**Jump if No Carry (relative)**			
Dxh	JNC addr	LSB Address Byte (MSN in opcode, x)			5/4
JNZ		**Jump if Not Zero (relative)**			
Bxh	JNZ addr	LSB Address Byte (MSN in opcode, x)			5/4
JZ		**Jump if Zero (relative)**			
Axh	JZ addr	LSB Address Byte (MSN in opcode, x)			5/4
LCALL		**Long Call**			
7Ch	LCALL addrl	addr MSB	addr LSB		13
LJMP		**Long Jump**			
7Dh	LJMP addrl	addr MSB	addr LSB		7
NOP		**No Operation**			
40h	NOP				4
RET		**Return from Call**			
7Fh	RET				8
RETI		**Return from Interrupt**			
7Eh	RETI				10
SSC		**System Supervisor Call**			NA
00h	SSC				

Non Destructive Test Instructions

				Flags	Cycles
CMP		**Non Destructive Compare**			
39h	CMP A,expr	Immediate		c z	5
3Ah	CMP A,[expr]	Direct Address		c z	7
3Bh	CMP A,[X+exr]	Index		c z	8
3Ch	CMP [expr],expr	Direct Address	Immediate	c z	8
3Dh	CMP [X+expr],expr	Index	Immediate	c z	9
TST		**Test with Mask**			
47h	TST [expr],expr	Direct Address	Bit Mask	z	8
48h	TST [X+expr],expr	Index	Bit Mask	z	9
49h	TST REG[expr],expr	Reg Direct Address	Bit Mask	z	8
4Ah	TST REG[X+expr],expr	Reg Index	Bit Mask	z	9

Arithmetic Instructions

				Flags	Cycles
ADC		**Add with Carry**			
09h	ADC A,expr	Immediate		c z	4
0Ah	ADC A,[expr]	Direct Address		c z	6
0Bh	ADC A,[X+expr]	Index		c z	7
0Ch	ADC [expr],A	Direct Address		c z	7
0Dh	ADC [X+expr],A	Index		c z	8
0Eh	ADC [expr],expr	Direct Address	Immediate	c z	9
0Fh	ADC [X+expr],expr	Index	Immediate	c z	10
ADD		**Add without Carry**			
01h	ADD A,expr	Immediate		c z	4
02h	ADD A,[expr]	Direct Address		c z	6
03h	ADD A,[X+expr]	Index		c z	7
04h	ADD [expr],A	Direct Address		c z	7
05h	ADD [X+expr],A	Index		c z	8
06h	ADD [expr],expr	Direct Address	Immediate	c z	9
07h	ADD [X+expr],expr	Index	Immediate	c z	10
38h	ADD SP,expr	Immediate		c z	5
SBB		**Subtract with Borrow**			
19h	SBB A,expr	Immediate		c z	4
1Ah	SBB A,[expr]	Direct Address		c z	6
1Bh	SBB A,[X+expr]	Index		c z	7
1Ch	SBB [expr],A	Direct Address		c z	7
1Dh	SBB [X+expr],A	Index		c z	8
1Eh	SBB [expr],expr	Direct Address	Immediate	c z	9
1Fh	SBB [X+expr],expr	Index	Immediate	c z	10
SUB		**Subtract without Borrow**			
11h	SUB A,expr	Immediate		c z	4
12h	SUB A,[expr]	Direct Address		c z	6
13h	SUB A,[X+expr]	Index		c z	7
14h	SUB [expr],A	Direct Address		c z	7
15h	SUB [X+expr],A	Index		c z	8
16h	SUB [expr],expr	Direct Address	Immediate	c z	9
17h	SUB [X+expr],expr	Index	Immediate	c z	10
DEC		**Decrement**			
78h	DEC A			c z	4
79h	DEC X			c z	4
7Ah	DEC [expr]	Direct Address		c z	7
7Bh	DEC [X+expr]	Index		c z	8
INC		**Increment**			
74h	INC A			c z	4
75h	INC X			c z	4
76h	INC [expr]	Direct Address		c z	7
77h	INC [X+expr]	Index		c z	8
ASL		**Arithmetic Shift Left**			
64h	ASL A			c z	4
65h	ASL [expr]	Direct Address		c z	7
66h	ASL [X+expr]	Index		c z	8
ASR		**Arithmetic Shift Right**			
67h	ASR A			c z	4
68h	ASR [expr]	Direct Address		c z	7
69h	ASR [X+expr]	Index		c z	8

Movement Instructions

					Flags	Cycles
INDEX		**Table Read (relative)**				
Fxh	INDEX addr	LSB Address Byte (MSN in opcode, x)			z	13
MOV		**Move**				
4Fh	MOV X,SP					4
50h	MOV A,expr	Immediate			z	4
51h	MOV A,[expr]	Direct Address			z	5
52h	MOV A,[X+expr]	Index			z	6
53h	MOV [expr],A	Direct Address				5
54h	MOV [X+expr],A	Index				6
55h	MOV [expr],expr	Direct Address	Immediate			8
56h	MOV [X+expr],expr	Index	Immediate			9
57h	MOV X,expr	Immediate				4
58h	MOV X,[expr]	Direct Address				6
59h	MOV X,[X+expr]	Index				7
5Ah	MOV [expr],X	Direct Address				5
5Bh	MOV A,X				z	4
5Ch	MOV X,A					4
5Dh	MOV A,REG[expr]	Reg Direct Address			z	6
5Eh	MOV A,REG[X+expr]	Reg Index			z	7
5Fh	MOV [expr],[expr]	Direct Address	Direct Address			10
60h	MOV REG[expr],A	Reg Direct Address				5
61h	MOV REG[X+expr],A	Reg Index				6
62h	MOV REG[expr],expr	Reg Direct Address	Immediate			8
63h	MOV REG[X+expr],expr	Reg Index	Immediate			9
MVI		**Move Indirect, Post Increment to Memory**				
3Eh	MVI A,[expr]	Direct Address (Page 0)			z	10
3Fh	MVI [expr],A	Direct Address (Page 0)				10
POP		**Pop Stack into Register**				
18h	POP A				z	5
20h	POP X					5
PUSH		**Push Register onto Stack**				
08h	PUSH A					4
10h	PUSH X					4
ROMX		**Table Read**				
28h	ROMX				z	11
SWAP		**Swap**				
4Bh	SWAP A,X				z	5
4Ch	SWAP A,[expr]	Direct Address			z	7
4Dh	SWAP X,[expr]	Direct Address			z	7
4Eh	SWAP A,SP				z	5

Logical Instructions

					Flags	Cycles
AND		**Bitwise AND**				
21h	AND A,expr	Immediate			z	4
22h	AND A,[expr]	Direct Address			z	6
23h	AND A,[X+expr]	Index			z	7
24h	AND [expr],A	Direct Address			z	7
25h	AND [X+expr],A	Index			z	8
26h	AND [expr],expr	Direct Address	Immediate		z	9
27h	AND [X+expr],expr	Index	Immediate		z	10
41h	AND REG[expr],expr	Reg Direct Address	Immediate		z	9
42h	AND REG[X+expr],expr	Reg Index	Immediate		z	10
70h	AND F,expr	Immediate			c z	4
OR		**Bitwise OR**				
29h	OR A,expr	Immediate			z	4
2Ah	OR A,[expr]	Direct Address			z	6
2Bh	OR A,[X+expr]	Index			z	7
2Ch	OR [expr],A	Direct Address			z	7
2Dh	OR [X+expr],A	Index			z	8
2Eh	OR [expr],expr	Direct Address	Immediate		z	**9**
2Fh	OR [X+expr],expr	Index	Immediate		z	10
43h	OR REG[expr],expr	Reg Direct Address	Immediate		z	9
44h	OR REG[X+expr],expr	Reg Index	Immediate		z	10
71h	OR F,expr	Immediate			c z	4
XOR		**Bitwise XOR**				
31h	XOR A,expr	Immediate			z	4
32h	XOR A,[expr]	Direct Address			z	**6**
33h	XOR A,[X+expr]	Index			z	7
34h	XOR [expr],A	Direct Address			z	7
35h	XOR [X+expr],A	Index			z	8
36h	XOR [expr],expr	Direct Address	Immediate		z	9
37h	XOR [X+expr],expr	Index	Immediate		z	10
45h	XOR REG[expr],expr	Reg Direct Address	Immediate		z	9
46h	XOR REG[X+expr],expr	Reg Index	Immediate		z	10
72h	XOR F,expr	Immediate			c z	4
CPL		**Complement Accumulator**				
73h	CPL A				z	4
RLC		**Rotate Left through Carry**				
6Ah	RLC A				c z	4
6Bh	RLC [expr]	Direct Address			c z	7
6Ch	RLC [X+expr]	Index			c z	8
RRC		**Rotate Right through Carry**				
6Dh	RRC A				c z	4
6Eh	RRC [expr]	Direct Address			c z	7
6Fh	RRC [X+expr]	Index			c z	8

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