Pin Definitions

Pad Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock buffers or DLL inputs. These pins become user inputs when not needed for clocks.
DLL	No	Input	Clock input pins that connect to DLL input or feedback clocks. Differential clock input (N input of pair) when paired with adjacent GCK input. Becomes a user I/O when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for Slave Parallel and Slave Serial modes, and output in Master Serial mode. After configuration, it is an input only with Don't Care logic levels.
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. Goes High to indicate the end of initialization. Goes back Low to indicate a CRC error. This pin becomes a user I/O after configuration.
DOUT/BUSY	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data can be loaded. It is not needed below 50 MHz. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	1.8V power supply pins for the internal core logic.

Pin Definitions *(Continued)*

Pad Name	Dedicated Pin	Direction	Description
V_{CCO}	Yes	Input	Power supply pins for output drivers (1.5V, 1.8V, 2.5V, or 3.3V subject to banking rules in module 2).
V_{REF}	No	Input	Input threshold reference voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules in module 2).
GND	Yes	Input	Ground. All must be connected.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx PCI cores. If the cores are not used, these pins are available as user I/Os.
L#[P/N] (e.g., L0P)	No	Bidirectional	Differential I/O with synchronous output. P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_Y (e.g., L0P_Y)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (asynchronous output not compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
L#[P/N]_YY (e.g., L0P_YY)	No	Bidirectional	Differential I/O with asynchronous or synchronous output (compatible for all densities in a package). P = positive, N = negative. The number (#) is used to associate the two pins of a differential pair. Becomes a general user I/O when not needed for differential signals.
I/O	No	Bidirectional	These pins can be configured to be input and/or output after configuration is completed. Unused I/Os are disabled with a weak pull-down resistor. After power-on and before configuration is completed, these pins are either pulled up or left floating according to the Mode pin values. See module 3 for power-on characteristics.

Spartan-IIE Package Pinouts

The Spartan-IIE family of FPGAs is available in five popular, low-cost packages, including plastic quad flat packs and fine-pitch ball grid arrays. Package drawings can be found at **http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Package+Drawings**. Family members have footprint compatibility across devices provided in the same package, with minor exceptions due to the smaller number of I/O in smaller devices or due to LVDS/LVPECL pin pairing. The Spartan-IIE family is not footprint compatible with any other FPGA family. The following package-specific pinout tables indicate function, pin, and bank information for all devices available in that package. The pinouts follow the pad locations around the die, starting from pin 1 on the QFP packages.

Low Voltage Differential Signals (LVDS and LVPECL)

The Spartan-IIE family features low-voltage differential signaling (LVDS and LVPECL). Each signal utilizes two pins on the Spartan-IIE device, known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

I/O, L#[P/N][-/_Y/_YY]

where

L = LVDS or LVPECL pin

= Pin pair number

P = Positive

N = Negative

_Y = Asynchronous output allowed (device-dependent)

_YY = Asynchronous output allowed (all devices)

Available Differential Pairs According to Package Type

Device	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	28	50	83	-	-
XC2S100E	28	50	83	86	-
XC2S150E	-	50	83	114	-
XC2S200E	-	50	83	120	-
XC2S300E	-	50	83	120	-
XC2S400E	-	-	83	120	172
XC2S600E	-	-	-	120	205

Synchronous or Asynchronous

I/O pins for differential signals can either be synchronous or asynchronous, input or output. Differential signaling requires the pins of each pair to switch simultaneously. If the output signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous, and therefore more care must be taken that they are simultaneous. Any differential pairs can be used for synchronous input and output signals as well as asynchronous input signals.

However, only the differential pairs with the _Y or _YY suffix can be used for asynchronous output signals.

Asynchronous Output Pad Name Designation

Because of differences between densities, the differential pairs that can be used for asynchronous outputs vary by device. The pairs that are available in all densities for a given package have the _YY suffix. These pins should be used for differential asynchronous outputs if the design may later move to a different density. All other differential pairs that can be used for asynchronous outputs have the _Y suffix.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. The "Pad Name" column leaves out the _Y suffix and the "LVDS Asynchronous Output Option" column indicates the densities that allow asynchronous outputs for LVDS or LVPECL on the given pin.

DLL Pins

Pins labeled "I/O (DLL)" can be used as general-purpose I/O or as inputs to the DLL. Adjacent DLL pins form a differential pair. They reside in two different banks, so if they are outputs the V_{CCO} level must be the same for both banks. Each DLL pin can also be paired with the adjacent GCK clock pin for a differential clock input. The "I/O (DLL)" pin always becomes the N terminal when paired with GCK, even if it is labeled "P" for its pairing with the adjacent DLL pin.

VREF Pins

Pins labeled "I/O, VREF" can be used as either an I/O or a VREF pin. If any I/O pin within the bank requires a VREF input, all the VREF pins in the bank must be connected to the same voltage. See the I/O banking rules in module 2 for more detail. If no pin in a given bank requires VREF, then that bank's VREF pins can be used as general I/O.

To simplify the following tables, the "Pad Name" column shows the part of the name that is common across densities. When VREF is only available in limited densities, the "Pad Name" column leaves out the VREF designation and the "VREF Option" column indicates the densities that provide VREF on the given pin.

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan-IIE device. They follow the pad locations around the die. In the TQ144 package, all VCCO pins must be connected to the same voltage.

TQ144 Pinouts (XC2S50E and XC2S100E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	-
I/O, VREF Bank 7	7	P5	-	All
I/O	7	P6	-	-
I/O, L27P	7	P7	XC2S50E	XC2S100E
I/O, L27N	7	P8	XC2S50E	-
GND	-	P9	-	-
I/O, L26P_YY	7	P10	All	-
I/O, L26N_YY	7	P11	All	-
I/O, VREF Bank 7, L25P	7	P12	XC2S50E	All
I/O, L25N	7	P13	XC2S50E	-
I/O	7	P14	-	-
I/O (IRDY)	7	P15	-	-
GND	-	P16	-	-
VCCO	-	P17	-	-
I/O (TRDY)	6	P18	-	-
VCCINT	-	P19	-	-
I/O	6	P20	-	-
I/O, L24P	6	P21	XC2S50E	-
I/O, VREF Bank 6, L24N	6	P22	XC2S50E	All
I/O, L23P_YY	6	P23	All	-
I/O, L23N_YY	6	P24	All	-
GND	-	P25	-	-
I/O, L22P	6	P26	XC2S50E	-
I/O, L22N	6	P27	XC2S50E	XC2S100E

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	6	P28	-	-
I/O, VREF Bank 6	6	P29	-	All
I/O	6	P30	-	-
I/O, L21P_YY	6	P31	All	-
I/O, L21N_YY	6	P32	All	-
M1	-	P33	-	-
GND	-	P34	-	-
M0	-	P35	-	-
VCCO	-	P36	-	-
M2	-	P37	-	-
I/O, L20N_YY	5	P38	All	-
I/O, L20P_YY	5	P39	All	-
I/O	5	P40	-	-
I/O, VREF Bank 5	5	P41	-	All
I/O	5	P42	-	-
I/O, L19N_YY	5	P43	All	XC2S100E
I/O, L19P_YY	5	P44	All	-
GND	-	P45	-	-
VCCINT	-	P46	-	-
I/O, L18N_YY	5	P47	All	-
I/O, L18P_YY	5	P48	All	-
I/O, VREF Bank 5	5	P49	-	All
I/O (DLL), L17N	5	P50	-	-
VCCINT	-	P51	-	-
GCK1, I	5	P52	-	-
VCCO	5	P53	-	-
GND	-	P54	-	-
GCK0, I	4	P55	-	-
I/O (DLL), L17P	4	P56	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	4	P57	-	-
I/O, VREF Bank 4	4	P58	-	All
I/O, L16N_YY	4	P59	All	-
I/O, L16P_YY	4	P60	All	-
VCCINT	-	P61	-	-
GND	-	P62	-	-
I/O, L15N_YY	4	P63	All	-
I/O, L15P_YY	4	P64	All	XC2S100E
I/O	4	P65	-	-
I/O, VREF Bank 4	4	P66	-	All
I/O	4	P67	-	-
I/O, L14N_YY	4	P68	All	-
I/O, L14P_YY	4	P69	All	-
GND	-	P70	-	-
DONE	3	P71	-	-
VCCO	-	P72	-	-
$\overline{\text{PROGRAM}}$	-	P73	-	-
I/O ($\overline{\text{INIT}}$), L13N_YY	3	P74	All	-
I/O (D7), L13P_YY	3	P75	All	-
I/O	3	P76	-	-
I/O, VREF Bank 3	3	P77	-	All
I/O	3	P78	-	-
I/O, L12N	3	P79	XC2S50E	XC2S100E
I/O (D6), L12P	3	P80	XC2S50E	-
GND	-	P81	-	-
I/O (D5), L11N_YY	3	P82	All	-
I/O, L11P_YY	3	P83	All	-
I/O	3	P84	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L10N	3	P85	XC2S50E	All
I/O (D4), L10P	3	P86	XC2S50E	-
I/O	3	P87	-	-
VCCINT	-	P88	-	-
I/O (TRDY)	3	P89	-	-
VCCO	-	P90	-	-
GND	-	P91	-	-
I/O (IRDY)	2	P92	-	-
I/O	2	P93	-	-
I/O (D3), L9N	2	P94	XC2S50E	-
I/O, VREF Bank 2, L9P	2	P95	XC2S50E	All
I/O	2	P96	-	-
I/O, L8N_YY	2	P97	All	-
I/O (D2), L8P_YY	2	P98	All	-
GND	-	P99	-	-
I/O (D1), L7N	2	P100	XC2S50E	-
I/O, L7P	2	P101	XC2S50E	XC2S100E
I/O	2	P102	-	-
I/O, VREF Bank 2	2	P103	-	All
I/O	2	P104	-	-
I/O (DIN, D0), L6N_YY	2	P105	All	-
I/O (DOUT, BUSY), L6P_YY	2	P106	All	-
CCLK	2	P107	-	-
VCCO	-	P108	-	-
TDO	2	P109	-	-
GND	-	P110	-	-
TDI	-	P111	-	-

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O ($\overline{CS}$), L5P_YY	1	P112	All	-
I/O ($\overline{WRITE}$), L5N_YY	1	P113	All	-
I/O	1	P114	-	-
I/O, VREF Bank 1	1	P115	-	All
I/O	1	P116	-	-
I/O, L4P_YY	1	P117	All	XC2S100E
I/O, L4N_YY	1	P118	All	-
GND	-	P119	-	-
VCCINT	-	P120	-	-
I/O, L3P_YY	1	P121	All	-
I/O, L3N_YY	1	P122	All	-
I/O, VREF Bank 1	1	P123	-	All
I/O	1	P124	-	-
I/O (DLL), L2P	1	P125	-	-
GCK2, I	1	P126	-	-
GND	-	P127	-	-
VCCO	-	P128	-	-
GCK3, I	0	P129	-	-
VCCINT	-	P130	-	-
I/O (DLL), L2N	0	P131	-	-
I/O, VREF Bank 0	0	P132	-	All
I/O, L1P_YY	0	P133	All	-
I/O, L1N_YY	0	P134	All	-
VCCINT	-	P135	-	-
GND	-	P136	-	-
I/O, L0P_YY	0	P137	All	-
I/O, L0N_YY	0	P138	All	XC2S100E

TQ144 Pinouts (XC2S50E and XC2S100E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P139	-	-
I/O, VREF Bank 0	0	P140	-	All
I/O	0	P141	-	-
I/O	0	P142	-	-
TCK	-	P143	-	-
VCCO	-	P144	-	-

TQ144 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P55	GCK0, I	P56	I/O (DLL), L17P
GCK1	5	P52	GCK1, I	P50	I/O (DLL), L17N
GCK2	1	P126	GCK2, I	P125	I/O (DLL), L2P
GCK3	0	P129	GCK3, I	P131	I/O (DLL), L2N

In the PQ208 package, all VCCO pins must be connected to the same voltage.

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
GND	-	P1	-	-
TMS	-	P2	-	-
I/O	7	P3	-	-
I/O	7	P4	-	XC2S200E, 300E
I/O	7	P5	-	-
I/O, VREF Bank 7, L49P	7	P6	XC2S50E, 150E, 200E, 300E	All
I/O, L49N	7	P7	XC2S50E, 150E, 200E, 300E	-
I/O	7	P8	-	-
I/O	7	P9	-	-
I/O, L48P	7	P10	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L48N	7	P11	XC2S50E, 300E	-
GND	-	P12	-	-
VCCO	-	P13	-	-
VCCINT	-	P14	-	-
I/O, L47P_YY	7	P15	All	-
I/O, L47N_YY	7	P16	All	-
I/O, L46P_YY	7	P17	All	-
I/O, L46N_YY	7	P18	All	-
GND	-	P19	-	-
I/O, VREF Bank 7, L45P	7	P20	XC2S50E, 300E	All
I/O, L45N	7	P21	XC2S50E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	7	P22	-	-
I/O, L44P_YY	7	P23	All	-
I/O (IRDY), L44N_YY	7	P24	All	-
GND	-	P25	-	-
VCCO	-	P26	-	-
I/O (TRDY)	6	P27	-	-
VCCINT	-	P28	-	-
I/O	6	P29	-	-
I/O, L43P	6	P30	XC2S50E, 300E	-
I/O, VREF Bank 6, L43N	6	P31	XC2S50E, 300E	All
GND	-	P32	-	-
I/O, L42P_YY	6	P33	All	-
I/O, L42N_YY	6	P34	All	-
I/O, L41P_YY	6	P35	All	-
I/O, L41N_YY	6	P36	All	-
VCCINT	-	P37	-	-
VCCO	-	P38	-	-
GND	-	P39	-	-
I/O, L40P	6	P40	XC2S50E, 300E	-
I/O, L40N	6	P41	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	6	P42	-	-
I/O	6	P43	-	-
I/O	6	P44	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 6, L39P	6	P45	XC2S100E, 150E	All
I/O, L39N	6	P46	XC2S100E, 150E	-
I/O	6	P47	-	XC2S200E, 300E
I/O, L38P_YY	6	P48	All	-
I/O, L38N_YY	6	P49	All	-
M1	-	P50	-	-
GND	-	P51	-	-
M0	-	P52	-	-
VCCO	-	P53	-	-
M2	-	P54	-	-
I/O, L37N_YY	5	P55	All	-
I/O, L37P_YY	5	P56	All	-
I/O	5	P57	-	XC2S200E, 300E
I/O	5	P58	-	-
I/O, VREF Bank 5, L36N_YY	5	P59	All	All
I/O, L36P_YY	5	P60	All	-
I/O, L35N	5	P61	XC2S50E, 100E, 300E	-
I/O, L35P	5	P62	XC2S50E, 100E, 300E	-
I/O, L34N	5	P63	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L34P	5	P64	XC2S50E, 100E, 200E, 300E	-
GND	-	P65	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P66	-	-
VCCINT	-	P67	-	-
I/O, L33N	5	P68	XC2S50E, 100E, 200E, 300E	-
I/O, L33P	5	P69	XC2S50E, 100E, 200E, 300E	-
I/O	5	P70	-	-
I/O, L32N	5	P71	XC2S100E, 150E	-
GND	-	P72	-	-
I/O, VREF Bank 5, L32P	5	P73	XC2S100E, 150E	All
I/O	5	P74	-	-
I/O (DLL), L31N	5	P75	-	-
VCCINT	-	P76	-	-
GCK1, I	5	P77	-	-
VCCO	-	P78	-	-
GND	-	P79	-	-
GCK0, I	4	P80	-	-
I/O (DLL), L31P	4	P81	-	-
I/O	4	P82	-	-
I/O, L30N	4	P83	XC2S50E, 200E, 300E	-
I/O, VREF Bank 4, L30P	4	P84	XC2S50E, 200E, 300E	All
GND	-	P85	-	-
I/O, L29N	4	P86	XC2S50E, 200E, 300E	-
I/O, L29P	4	P87	XC2S50E, 200E, 300E	-
I/O, L28N	4	P88	XC2S50E, 100E, 200E, 300E	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L28P	4	P89	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P90	-	-
VCCO	-	P91	-	-
GND	-	P92	-	-
I/O, L27N	4	P93	XC2S50E, 100E, 200E, 300E	-
I/O, L27P	4	P94	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	4	P95	-	-
I/O	4	P96	-	-
I/O, L26N_YY	4	P97	All	-
I/O, VREF Bank 4, L26P_YY	4	P98	All	All
I/O	4	P99	-	-
I/O	4	P100	-	XC2S200E, 300E
I/O, L25N_YY	4	P101	All	-
I/O, L25P_YY	4	P102	All	-
GND	-	P103	-	-
DONE	3	P104	-	-
VCCO	-	P105	-	-
$\overline{\text{PROGRAM}}$	-	P106	-	-
I/O ($\overline{\text{INIT}}$), L24N_YY	3	P107	All	-
I/O (D7), L24P_YY	3	P108	All	-
I/O	3	P109	-	XC2S200E, 300E
I/O	3	P110	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 3, L23N	3	P111	XC2S50E, 150E, 200E, 300E	All
I/O, L23P	3	P112	XC2S50E, 150E, 200E, 300E	-
I/O	3	P113	-	-
I/O	3	P114	-	-
I/O, L22N	3	P115	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O (D6), L22P	3	P116	XC2S50E, 300E	-
GND	-	P117	-	-
VCCO	-	P118	-	-
VCCINT	-	P119	-	-
I/O (D5), L21N_YY	3	P120	All	-
I/O, L21P_YY	3	P121	All	-
I/O, L20N_YY	3	P122	All	-
I/O, L20P_YY	3	P123	All	-
GND	-	P124	-	-
I/O, VREF Bank 3, L19N	3	P125	XC2S50E, 300E	All
I/O (D4), L19P	3	P126	XC2S50E, 300E	-
I/O	3	P127	-	-
VCCINT	-	P128	-	-
I/O (TRDY)	3	P129	-	-
VCCO	-	P130	-	-
GND	-	P131	-	-
I/O (IRDY), L18N_YY	2	P132	All	-
I/O, L18P_YY	2	P133	All	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	2	P134	-	-
I/O (D3), L17N	2	P135	XC2S50E, 300E	-
I/O, VREF Bank 2, L17P	2	P136	XC2S50E, 300E	All
GND	-	P137	-	-
I/O, L16N_YY	2	P138	All	-
I/O, L16P_YY	2	P139	All	-
I/O, L15N_YY	2	P140	All	-
I/O (D2), L15P_YY	2	P141	All	-
VCCINT	-	P142	-	-
VCCO	-	P143	-	-
GND	-	P144	-	-
I/O (D1), L14N	2	P145	XC2S50E, 300E	-
I/O, L14P	2	P146	XC2S50E, 300E	XC2S100E, 150E, 200E, 300E
I/O	2	P147	-	-
I/O	2	P148	-	-
I/O	2	P149	-	-
I/O, VREF Bank 2, L13N	2	P150	XC2S100E, 150E	All
I/O, L13P	2	P151	XC2S100E, 150E	-
I/O	2	P152	-	XC2S200E, 300E
I/O (DIN, D0), L12N_YY	2	P153	All	-
I/O (DOUT, BUSY), L12P_YY	2	P154	All	-
CCLK	2	P155	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
VCCO	-	P156	-	-
TDO	2	P157	-	-
GND	-	P158	-	-
TDI	-	P159	-	-
I/O ($\overline{CS}$), L11P_YY	1	P160	All	-
I/O ($\overline{WRITE}$), L11N_YY	1	P161	All	-
I/O	1	P162	-	XC2S200E, 300E
I/O	1	P163	-	-
I/O, VREF Bank 1, L10P_YY	1	P164	All	All
I/O, L10N_YY	1	P165	All	-
I/O	1	P166	-	-
I/O	1	P167	-	-
I/O, L9P	1	P168	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O, L9N	1	P169	XC2S50E, 100E, 200E, 300E	-
GND	-	P170	-	-
VCCO	-	P171	-	-
VCCINT	-	P172	-	-
I/O, L8P	1	P173	XC2S50E, 100E, 200E, 300E	-
I/O, L8N	1	P174	XC2S50E, 100E, 200E, 300E	-
I/O, L7P	1	P175	XC2S50E, 200E, 300E	-
I/O, L7N	1	P176	XC2S50E, 200E, 300E	-
GND	-	P177	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 1, L6P	1	P178	XC2S50E, 200E, 300E	All
I/O, L6N	1	P179	XC2S50E, 200E, 300E	-
I/O	1	P180	-	-
I/O (DLL), L5P	1	P181	-	-
GCK2, I	1	P182	-	-
GND	-	P183	-	-
VCCO	-	P184	-	-
GCK3, I	0	P185	-	-
VCCINT	-	P186	-	-
I/O (DLL), L5N	0	P187	-	-
I/O, L4P	0	P188	XC2S50E, 200E, 300E	-
I/O, VREF Bank 0, L4N	0	P189	XC2S50E, 200E, 300E	All
GND	-	P190	-	-
I/O, L3P	0	P191	XC2S50E, 200E, 300E	-
I/O, L3N	0	P192	XC2S50E, 200E, 300E	-
I/O, L2P	0	P193	XC2S50E, 100E, 200E, 300E	-
I/O, L2N	0	P194	XC2S50E, 100E, 200E, 300E	-
VCCINT	-	P195	-	-
VCCO	-	P196	-	-
GND	-	P197	-	-
I/O, L1P	0	P198	XC2S50E, 100E, 200E, 300E	-
I/O, L1N	0	P199	XC2S50E, 100E, 200E, 300E	XC2S100E, 150E, 200E, 300E
I/O	0	P200	-	-

PQ208 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O	0	P201	-	-
I/O, L0P_YY	0	P202	All	-
I/O, VREF Bank 0, L0N_YY	0	P203	All	All
I/O	0	P204	-	-
I/O	0	P205	-	XC2S200E, 300E
I/O	0	P206	-	-
TCK	-	P207	-	-
VCCO	-	P208	-	-

PQ208 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	P80	GCK0, I	P81	I/O (DLL), L31P
GCK1	5	P77	GCK1, I	P75	I/O (DLL), L31N
GCK2	1	P182	GCK2, I	P181	I/O (DLL), L5P
GCK3	0	P185	GCK3, I	P187	I/O (DLL), L5N

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
TMS	-	B1	-	-
I/O	7	D3	-	-
I/O, L83P	7	C2	XC2S100E, 150E	-
I/O, L83N	7	C1	XC2S100E, 150E	XC2S200E, 300E, 400E
I/O, L82P_YY	7	D2	All	-
I/O, L82N_YY	7	D1	All	-
I/O, VREF Bank 7, L81P	7	E3	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L81N	7	E4	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, L80P	7	E2	XC2S200E, 400E	-
I/O, L80N	7	E1	XC2S200E, 400E	-
I/O, L79P	7	F4	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L79N	7	F3	XC2S50E, 300E, 400E	-
I/O, L78P_YY	7	F2	All	-
I/O, L78N_YY	7	F1	All	-
I/O, L77P	7	F5	XC2S100E, 150E	-
I/O, L77N	7	G5	XC2S100E, 150E	-
I/O, L76P_YY	7	G3	All	-
I/O, L76N_YY	7	G4	All	-
I/O, VREF Bank 7, L75P	7	G2	XC2S50E, 300E, 400E	All
I/O, L75N	7	G1	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L74P	7	H4	XC2S100E, 150E, 200E	-
I/O, L74N	7	H3	XC2S100E, 150E, 200E	XC2S400E
I/O, L73P_YY	7	H2	All	-
I/O (IRDY), L73N_YY	7	H1	All	-
I/O (TRDY)	6	J4	-	-
I/O, L72P	6	J2	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L72N	6	J3	XC2S100E, 150E, 200E, 400E	-
I/O, L71P	6	J1	XC2S50E, 300E, 400E	-
I/O, VREF Bank 6, L71N	6	K1	XC2S50E, 300E, 400E	All
I/O, L70P_YY	6	K2	All	-
I/O, L70N_YY	6	K3	All	-
I/O, L69P	6	L1	XC2S100E, 150E, 400E	-
I/O, L69N	6	L2	XC2S100E, 150E, 400E	-
I/O, L68P_YY	6	K4	All	-
I/O, L68N_YY	6	K5	All	-
I/O, L67P	6	L3	XC2S50E, 300E, 400E	-
I/O, L67N	6	M2	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L66P	6	M1	XC2S150E, 200E, 400E	-
I/O, L66N	6	N1	XC2S150E, 200E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L65P	6	L4	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 6, L65N	6	L5	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L64P_YY	6	M3	All	-
I/O, L64N_YY	6	M4	All	-
I/O, L63P	6	N2	XC2S100E, 200E, 300E	-
I/O, L63N	6	N3	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O, L62P_YY	6	P1	All	-
I/O, L62N_YY	6	P2	All	-
M1	-	R1	-	-
M0	-	T2	-	-
M2	-	R3	-	-
I/O, L61N_YY	5	P4	All	-
I/O, L61P_YY	5	R4	All	-
I/O, L60N	5	T3	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L60P	5	T4	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L59N_YY	5	N5	All	-
I/O, L59P_YY	5	P5	All	-
I/O, VREF Bank 5, L58N_YY	5	R5	All	All
I/O, L58P_YY	5	T5	All	-
I/O, L57N	5	N6	XC2S50E, 100E, 150E, 300E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L57P	5	P6	XC2S50E, 100E, 150E, 300E	-
I/O, L56N	5	R6	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L56P	5	T6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L55N	5	M6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L55P	5	N7	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	5	P7	-	-
I/O, L54N	5	R7	XC2S50E, 200E, 300E, 400E	-
I/O, L54P	5	T7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 5, L53N	5	M7	XC2S50E, 200E, 300E, 400E	All
I/O, L53P	5	N8	XC2S50E, 200E, 300E, 400E	-
I/O	5	P8	-	XC2S400E
I/O (DLL), L52N	5	R8	-	-
GCK1, I	5	T8	-	-
GCK0, I	4	T9	-	-
I/O (DLL), L52P	4	R9	-	-
I/O, L51N	4	P9	XC2S50E, 150E, 200E, 400E	XC2S400E

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L51P	4	N9	XC2S50E, 150E, 200E, 400E	-
I/O, L50N	4	T10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 4, L50P	4	R10	XC2S50E, 200E, 300E, 400E	All
I/O, L49N	4	P10	XC2S50E, 200E, 300E, 400E	-
I/O, L49P	4	R11	XC2S50E, 200E, 300E, 400E	-
I/O	4	T11	-	-
I/O, L48N	4	N10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L48P	4	M10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47N	4	P11	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L47P	4	R12	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L46N	4	T12	XC2S50E, 100E, 150E, 300E	-
I/O, L46P	4	T13	XC2S50E, 100E, 150E, 300E	-
I/O, L45N_YY	4	N11	All	-
I/O, VREF Bank 4, L45P_YY	4	M11	All	All
I/O, L44N_YY	4	P12	All	-
I/O, L44P_YY	4	N12	All	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L43N	4	R13	XC2S50E, 150E	XC2S200E, 300E, 400E
I/O, L43P	4	P13	XC2S50E, 150E	-
I/O, L42N_YY	4	T14	All	-
I/O, L42P_YY	4	R14	All	-
DONE	3	T15	-	-
$\overline{\text{PROGRAM}}$	-	R16	-	-
I/O ($\overline{\text{INIT}}$), L41N_YY	3	P15	All	-
I/O (D7), L41P_YY	3	P16	All	-
I/O, L40N	3	N15	XC2S100E, 150E, 400E	-
I/O, L40P	3	N16	XC2S100E, 150E, 400E	XC2S200E, 300E, 400E
I/O, L39N	3	N14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L39P	3	M14	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L38N	3	M15	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L38P	3	M16	XC2S50E, 150E, 200E, 300E, 400E	-
I/O(2)	3	M13	-	-
I/O(2)	3	L14	-	-
I/O, L36N	3	L15	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O (D6), L36P	3	L16	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O (D5), L35N_YY	3	L13	All	-
I/O, L35P_YY	3	K14	All	-
I/O, L34N	3	K15	XC2S100E, 150E, 400E	-
I/O, L34P	3	K16	XC2S100E, 150E, 400E	-
I/O, L33N	3	L12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L33P	3	K12	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, VREF Bank 3, L32N	3	K13	XC2S50E, 300E, 400E	All
I/O (D4), L32P	3	J14	XC2S50E, 300E, 400E	-
I/O, L31N	3	J15	XC2S100E, 150E, 200E, 400E	-
I/O, L31P	3	J16	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O (TRDY)	3	J13	-	-
I/O (IRDY), L30N_YY	2	H16	All	-
I/O, L30P_YY	2	G16	All	-
I/O, L29N	2	H14	XC2S100E, 150E, 200E, 400E	XC2S400E
I/O, L29P	2	H15	XC2S100E, 150E, 200E, 400E	-
I/O (D3), L28N	2	G15	XC2S50E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, VREF Bank 2, L28P	2	F16	XC2S50E, 300E, 400E	All
I/O, L27N	2	H13	XC2S50E, 100E, 150E, 200E, 300E(1)	-
I/O, L27P	2	G14	XC2S50E, 100E, 150E, 200E, 300E(2)	-
I/O, L26N	2	F15	XC2S100E, 150E, 400E	-
I/O, L26P	2	E16	XC2S100E, 150E, 400E	-
I/O, L25N_YY	2	G13	All	-
I/O (D2), L25P_YY	2	F14	All	-
I/O (D1), L24N	2	E15	XC2S50E, 300E, 400E	-
I/O, L24P	2	D16	XC2S50E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L23N	2	F13	XC2S150E, 200E, 400E	-
I/O, L23P	2	E14	XC2S150E, 200E, 400E	-
I/O, L22N	2	D15	XC2S50E, 150E, 200E, 300E, 400E	-
I/O, VREF Bank 2, L22P	2	C16	XC2S50E, 150E, 200E, 300E, 400E	All
I/O, L21N	2	G12	XC2S50E, 100E, 200E, 300E	-
I/O, L21P	2	F12	XC2S50E, 100E, 200E, 300E	-
I/O, L20N	2	E13	XC2S100E, 200E, 300E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L20P	2	D14	XC2S100E, 200E, 300E	XC2S200E, 300E, 400E
I/O (DIN, D0), L19N_YY	2	B16	All	-
I/O (DOUT, BUSY), L19P_YY	2	C15	All	-
CCLK	2	A15	-	-
TDO	2	B14	-	-
TDI	-	C13	-	-
I/O ($\overline{CS}$), L18P_YY	1	A14	All	-
I/O ($\overline{WRITE}$), L18N_YY	1	A13	All	-
I/O, L17P	1	B13	XC2S50E, 100E, 200E, 300E, 400E	XC2S200E, 300E, 400E
I/O, L17N	1	C12	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L16P_YY	1	B12	All	-
I/O, L16N_YY	1	A12	All	-
I/O, VREF Bank 1, L15P_YY	1	D12	All	All
I/O, L15N_YY	1	E11	All	-
I/O, L14P	1	D11	XC2S50E, 100E, 150E, 300E	-
I/O, L14N	1	C11	XC2S50E, 100E, 150E, 300E	-
I/O, L13P	1	B11	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L13N	1	A11	XC2S50E, 100E, 200E, 300E, 400E	-

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L12P	1	E10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L12N	1	D10	XC2S50E, 100E, 200E, 300E, 400E	-
I/O	1	C10	-	-
I/O, L11P	1	B10	XC2S50E, 200E, 300E, 400E	-
I/O, L11N	1	A10	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 1, L10P	1	D9	XC2S50E, 200E, 300E, 400E	All
I/O, L10N	1	C9	XC2S50E, 200E, 300E, 400E	-
I/O, L9P	1	B9	XC2S50E, 150E, 200E, 400E	-
I/O, L9N	1	A9	XC2S50E, 150E, 200E, 400E	XC2S400E
I/O (DLL), L8P	1	A8	-	-
GCK2, I	1	B8	-	-
GCK3, I	0	C8	-	-
I/O (DLL), L8N	0	D8	-	-
I/O	0	A7	-	XC2S400E
I/O, L7P	0	E7	XC2S50E, 200E, 300E, 400E	-
I/O, VREF Bank 0, L7N	0	D7	XC2S50E, 200E, 300E, 400E	All

FT256 Pinouts (XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option
Function	Bank			
I/O, L6P	0	C7	XC2S50E, 200E, 300E, 400E	-
I/O, L6N	0	B7	XC2S50E, 200E, 300E, 400E	-
I/O	0	A6	-	-
I/O, L5P	0	B6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L5N	0	C6	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4P	0	A5	XC2S50E, 100E, 200E, 300E, 400E	-
I/O, L4N	0	B5	XC2S50E, 100E, 200E, 300E, 400E	XC2S100E, 150E, 200E, 300E, 400E
I/O, L3P	0	D6	XC2S50E, 100E, 300E	-
I/O, L3N	0	E6	XC2S50E, 100E, 300E	-
I/O, L2P_YY	0	D5	All	-
I/O, VREF Bank 0, L2N_YY	0	C5	All	All
I/O, L1P_YY	0	B4	All	-
I/O, L1N_YY	0	C4	All	-
I/O, L0P_YY	0	A4	All	-
I/O, L0N_YY	0	A3	All	XC2S200E, 300E, 400E
I/O	0	B3	-	-
TCK	-	A2	-	-

Notes:
1. Although designated with the _YY suffix in the XC2S50E, XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.
2. There is no pair L37.

FT256 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	T9	GCK0, I	R9	I/O (DLL), L52P
GCK1	5	T8	GCK1, I	R8	I/O (DLL), L52N
GCK2	1	B8	GCK2, I	A8	I/O (DLL), L8P
GCK3	0	C8	GCK3, I	D8	I/O (DLL), L8N

Additional FT256 Package Pins

VCCINT Pins				
C3	C14	D4	D13	E5
E12	M5	M12	N4	N13
P3	P14	-	-	-
VCCO Bank 0 Pins				
E8	F7	F8	-	-
VCCO Bank 1 Pins				
E9	F9	F10	-	-
VCCO Bank 2 Pins				
G11	H11	H12	-	-
VCCO Bank 3 Pins				
J11	J12	K11	-	-
VCCO Bank 4 Pins				
L9	L10	M9	-	-
VCCO Bank 5 Pins				
L7	L8	M8	-	-
VCCO Bank 6 Pins				
J5	J6	K6	-	-
VCCO Bank 7 Pins				
G6	H5	H6	-	-
GND Pins				
A1	A16	B2	B15	F6
F11	G7	G8	G9	G10
H7	H8	H9	H10	J7
J8	J9	J10	K7	K8
K9	K10	L6	L11	R2
R15	T1	T16	-	-

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
TMS	-	E4	-	-	TMS	TMS	TMS	TMS	TMS	TMS
I/O	7	D3	XC2S150E	-	I/O	I/O, L113P_Y	I/O	I/O	I/O	I/O
I/O	7	C2	-	-	-	-	-	I/O	I/O	I/O
I/O	7	C1	XC2S150E	-	-	I/O, L113N_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	D2	XC2S150E, 200E, 300E, 400E	-	-	I/O, L112P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P_Y	I/O, L119P
I/O, L#N_Y	7	D1	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L112N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N_Y	I/O, L119N
I/O, L#P_Y	7	E2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L85P_Y	I/O, L111P	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P_Y	I/O, VREF Bank 7, L118P	I/O, VREF Bank 7, L118P_Y
I/O, L#N_Y	7	E3	XC2S100E, 200E, 300E, 600E	-	I/O, L85N_Y	I/O, L111N	I/O, L118N_Y	I/O, L118N_Y	I/O, L118N	I/O, L118N_Y
I/O	7	E1	-	-	-	-	-	I/O	I/O	I/O
I/O	7	F5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	F4	XC2S100E, 200E, 300E, 600E	-	I/O, L84P_Y	I/O, L110P	I/O, L117P_Y	I/O, L117P_Y	I/O, L117P	I/O, L117P_Y
I/O, L#N_Y	7	F3	XC2S100E, 200E, 300E, 600E	-	I/O, L84N_Y	I/O, L110N	I/O, L117N_Y	I/O, L117N_Y	I/O, L117N	I/O, L117N_Y
I/O, VREF Bank 7, L#P_Y	7	F2	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 7, L83P	I/O, VREF Bank 7, L109P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y	I/O, VREF Bank 7, L116P_Y
I/O, L#N_Y	7	F1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L83N	I/O, L109N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y	I/O, L116N_Y
I/O	7	G5	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	G4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L108P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P_Y	I/O, L115P
I/O, L#N_Y	7	G3	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L108N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N_Y	I/O, L115N
I/O, L#P_Y	7	G2	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L82P_Y	I/O, L107P_Y	I/O, L114P	I/O, L114P_Y	I/O, L114P	I/O, VREF Bank 7, L114P_Y
I/O, L#N_Y	7	G1	XC2S100E, 150E, 300E, 600E	-	I/O, L82N_Y	I/O, L107N_Y	I/O, L114N	I/O, L114N_Y	I/O, L114N	I/O, L114N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O	7	H5	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 7, L#P_Y	7	H3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L81P	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L113P	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y	I/O, VREF Bank 7, L113P_Y
I/O, L#N_Y	7	H4	XC2S300E, 400E, 600E	-	I/O, L81N	I/O, L106N	I/O, L113N	I/O, L113N_Y	I/O, L113N_Y	I/O, L113N_Y
I/O, L#P_YY	7	H2	All	-	I/O, L80P_YY	I/O, L105P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY	I/O, L112P_YY
I/O, L#N_YY	7	H1	All	-	I/O, L80N_YY	I/O, L105N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY	I/O, L112N_YY
I/O	7	J6	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P_Y	7	J4	XC2S150E, 200E, 300E, 400E	-	-	I/O, L104P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P_Y	I/O, L111P
I/O, L#N_Y	7	J5	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L79P_Y	I/O, L104N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N_Y	I/O, L111N
I/O, L#P_Y	7	J3	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L79N_Y	I/O, L103P_Y	I/O, L110P_Y	I/O, L110P_Y	I/O, L110P	I/O, L110P_Y
I/O, L#N_Y	7	J2	XC2S150E, 200E, 300E, 600E	-	-	I/O, L103N_Y	I/O, L110N_Y	I/O, L110N_Y	I/O, L110N	I/O, L110N_Y
I/O	7	J1	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	7	K5	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L78P_YY	I/O, L102P_YY	I/O, L109P_YY	I/O, L109P_YY	I/O, L109P	I/O, L109P_Y
I/O, L#N	7	K6	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L78N_YY	I/O, L102N_YY	I/O, L109N_YY	I/O, L109N_YY	I/O, L109N	I/O, L109N_Y
I/O, VREF Bank 7, L#P_Y	7	K3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 7, L77P	I/O, VREF Bank 7, L101P	I/O, VREF Bank 7, L108P	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y	I/O, VREF Bank 7, L108P_Y
I/O, L#N_Y	7	K4	XC2S300E, 400E, 600E	-	I/O, L77N	I/O, L101N	I/O, L108N	I/O, L108N_Y	I/O, L108N_Y	I/O, L108N_Y
I/O	7	K2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	7	K1	XC2S300E, 400E	-	-	-	I/O, L107P	I/O, L107P_Y	I/O, L107P_Y	I/O, L107P
I/O, L#N_Y	7	L1	XC2S100E, 150E, 300E, 400E	-	I/O, L76P_Y	I/O, L100P_Y	I/O, L107N	I/O, L107N_Y	I/O, L107N_Y	I/O, L107N
I/O, L#P_Y	7	L3	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L76N_Y	I/O, L100N_Y	I/O, L106P_Y	I/O, L106P_Y	I/O, VREF Bank 7, L106P	I/O, VREF Bank 7, L106P_Y
I/O, L#N_Y	7	L2	XC2S200E, 300E, 600E	-	-	I/O	I/O, L106N_Y	I/O, L106N_Y	I/O, L106N	I/O, L106N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O	7	L4	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_YY	7	L5	All	-	I/O, L75P_YY	I/O, L99P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY	I/O, L105P_YY
I/O (IRDY), L#N_YY	7	L6	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L99N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY	I/O (IRDY), L105N_YY
I/O (TRDY)	6	M1	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)
I/O	6	M2	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	M3	XC2S200E, 300E, 600E	-	-	I/O	I/O, L104P_Y	I/O, L104P_Y	I/O, L104P	I/O, L104P_Y
I/O, L#N_Y	6	M4	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L74P_Y	I/O, L98P_Y	I/O, L104N_Y	I/O, L104N_Y	I/O, VREF Bank 6, L104N	I/O, VREF Bank 6, L104N_Y
I/O, L#P_Y	6	M5	XC2S100E, 150E, 300E, 400E	-	I/O, L74N_Y	I/O, L98N_Y	I/O, L103P	I/O, L103P_Y	I/O, L103P_Y	I/O, L103P
I/O, L#N_Y	6	M6	XC2S300E, 400E	-	-	-	I/O, L103N	I/O, L103N_Y	I/O, L103N_Y	I/O, L103N
I/O	6	N1	-	-	-	-	-	I/O	I/O	I/O
I/O	6	N2	-	-	I/O, L73P	I/O, L97P	I/O	I/O	I/O	I/O
I/O, VREF Bank 6, L#P	6	N3	XC2S200E, 400E	All	I/O, VREF Bank 6, L73N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P	I/O, VREF Bank 6, L102P_Y	I/O, VREF Bank 6, L102P
I/O, L#N	6	N4	XC2S100E, 150E, 200E, 400E	-	I/O, L72P_Y	I/O, L96P_Y	I/O, L102N_Y	I/O, L102N	I/O, L102N_Y	I/O, L102N
I/O, L#P_Y	6	N5	XC2S100E, 150E, 300E, 600E	-	I/O, L72N_Y	I/O, L96N_Y	I/O, L101P	I/O, L101P_Y	I/O, L101P	I/O, L101P_Y
I/O, L#N_Y	6	N6	XC2S300E, 600E	-	-	-	I/O, L101N	I/O, L101N_Y	I/O, L101N	I/O, L101N_Y
I/O, L#P_Y	6	P1	XC2S150E, 200E, 300E, 600E	-	-	I/O, L95P_Y	I/O, L100P_Y	I/O, L100P_Y	I/O, L100P	I/O, L100P_Y
I/O, L#N_Y	6	P2	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L71P_Y	I/O, L95N_Y	I/O, L100N_Y	I/O, L100N_Y	I/O, L100N	I/O, L100N_Y
I/O	6	R1	XC2S100E, 150E	-	I/O, L71N_Y	I/O, L94P_Y	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	P3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L94N_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y	I/O, L99P_Y
I/O, L#N_Y	6	P4	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y	I/O, L99N_Y
I/O, L#P_YY	6	P5	All	-	I/O, L70P_YY	I/O, L93P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY	I/O, L98P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N_YY	6	P6	All	-	I/O, L70N_YY	I/O, L93N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY	I/O, L98N_YY
I/O, L#P_Y	6	R2	XC2S300E, 400E, 600E	-	I/O, L69P	I/O, L92P	I/O, L97P	I/O, L97P_Y	I/O, L97P_Y	I/O, L97P_Y
I/O, VREF Bank 6, L#N_Y	6	R3	XC2S300E, 400E, 600E	All	I/O, VREF Bank 6, L69N	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L97N	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y	I/O, VREF Bank 6, L97N_Y
I/O	6	R4	-	-	-	-	-	I/O	I/O	I/O
I/O	6	R5	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	6	T2	XC2S200E, 400E, 600E	XC2S600E	I/O, L68P	I/O, L91P	I/O, L96P_Y	I/O, L96P	I/O, L96P_Y	I/O, VREF Bank 6, L96P_Y
I/O, L#N	6	T3	XC2S200E, 400E, 600E	-	I/O, L68N	I/O, L91N	I/O, L96N_Y	I/O, L96N	I/O, L96N_Y	I/O, L96N_Y
I/O, L#P_Y	6	T4	XC2S150E, 300E, 400E	-	-	I/O, L90P_Y	I/O, L95P	I/O, L95P_Y	I/O, L95P_Y	I/O, L95P
I/O, L#N_Y	6	T5	XC2S150E, 300E, 400E	-	-	I/O, L90N_Y	I/O, L95N	I/O, L95N_Y	I/O, L95N_Y	I/O, L95N
I/O, L#P_Y	6	T1	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L67P	I/O, L89P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y	I/O, L94P_Y
I/O, VREF Bank 6, L#N_Y	6	U1	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 6, L67N	I/O, VREF Bank 6, L89N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y	I/O, VREF Bank 6, L94N_Y
I/O	6	U2	XC2S100E	-	I/O, L66P_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	U3	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L66N_Y	I/O, L88P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y	I/O, L93P_Y
I/O, L#N_Y	6	U4	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L88N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y	I/O, L93N_Y
I/O	6	V1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_Y	6	W1	XC2S100E, 200E, 300E, 600E	-	I/O, L65P_Y	I/O, L87P	I/O, L92P_Y	I/O, L92P_Y	I/O, L92P	I/O, L92P_Y
I/O, L#N_Y	6	V2	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L65N_Y	I/O, L87N	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N_Y	I/O, VREF Bank 6, L92N	I/O, VREF Bank 6, L92N_Y
I/O	6	W2	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P_Y	6	V3	XC2S200E, 300E, 400E	-	-	I/O, L86P	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P_Y	I/O, L91P
I/O, L#N_Y	6	V4	XC2S200E, 300E, 400E	-	-	I/O, L86N	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N_Y	I/O, L91N
I/O	6	Y1	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P_YY	6	Y2	All	-	I/O, L64P_YY	I/O, L85P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY	I/O, L90P_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N_YY	6	W3	All	-	I/O, L64N_YY	I/O, L85N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY	I/O, L90N_YY
M1	-	U5	-	-	M1	M1	M1	M1	M1	M1
M0	-	AA1	-	-	M0	M0	M0	M0	M0	M0
M2	-	AB2	-	-	M2	M2	M2	M2	M2	M2
I/O, L#N_Y	5	AA3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y	I/O, L89N_Y
I/O, L#P_Y	5	AB3	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L84P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y	I/O, L89P_Y
I/O	5	AB4	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA5	XC2S100E, 150E	-	I/O, L63N_Y	I/O, L83N_Y	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W5	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L63P_Y	I/O, L83P_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y	I/O, L88N_Y
I/O, L#P_Y	5	Y5	XC2S200E, 300E, 400E, 600E	-	I/O	I/O	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y	I/O, L88P_Y
I/O, L#N_Y	5	AB5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L62N_Y	I/O, L82N	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y	I/O, VREF Bank 5, L87N_Y
I/O, L#P_Y	5	AB6	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L62P_Y	I/O, L82P	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y	I/O, L87P_Y
I/O	5	Y6	-	-	-	-	-	I/O	I/O	I/O
I/O	5	AA6	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_YY	5	V6	All	-	I/O, L61N_YY	I/O, L81N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY	I/O, L86N_YY
I/O, L#P_YY	5	W6	All	-	I/O, L61P_YY	I/O, L81P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY	I/O, L86P_YY
I/O, VREF Bank 5, L#N_YY	5	AB7	All	All	I/O, VREF Bank 5, L60N_YY	I/O, VREF Bank 5, L80N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY	I/O, VREF Bank 5, L85N_YY
I/O, L#P_YY	5	AA7	All	-	I/O, L60P_YY	I/O, L80P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY	I/O, L85P_YY
I/O	5	Y7	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	V7	XC2S300E, 600E	-	-	I/O, L79N	I/O, L84N	I/O, L84N_Y	I/O, L84N	I/O, L84N_Y
I/O, L#P_Y	5	W7	XC2S300E, 600E	-	I/O	I/O, L79P	I/O, L84P	I/O, L84P_Y	I/O, L84P	I/O, L84P_Y
I/O, L#N_Y	5	AB8	XC2S100E, 300E, 600E	XC2S600E	I/O, L59N_Y	I/O, L78N	I/O, L83N	I/O, L83N_Y	I/O, L83N	I/O, VREF Bank 5, L83N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P_Y	5	AA8	XC2S100E, 300E, 600E	-	I/O, L59P_Y	I/O, L78P	I/O, L83P	I/O, L83P_Y	I/O, L83P	I/O, L83P_Y
I/O	5	Y8	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 5, L#N_Y	5	V8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L58N_Y	I/O, VREF Bank 5, L77N	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y	I/O, VREF Bank 5, L82N_Y
I/O, L#P_Y	5	W8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L58P_Y	I/O, L77P	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y	I/O, L82P_Y
I/O, L#N_Y	5	AB9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57N_Y	I/O, L76N	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y	I/O, L81N_Y
I/O, L#P_Y	5	AA9	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L57P_Y	I/O, L76P	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y	I/O, L81P_Y
I/O	5	AB10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L75N_Y	I/O, L80N	I/O, L80N_Y	I/O, L80N_Y	I/O, L80N_Y
I/O, L#P_Y	5	Y9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56N_Y	I/O, L75P_Y	I/O, L80P	I/O, L80P_Y	I/O, L80P_Y	I/O, L80P_Y
I/O, L#N_Y	5	V9	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L56P_Y	I/O, L74N_Y	I/O, L79N	I/O, L79N_Y	I/O, L79N_Y	I/O, L79N_Y
I/O, L#P_Y	5	U9	XC2S150E, 300E, 400E, 600E	-	-	I/O, L74P_Y	I/O, L79P	I/O, L79P_Y	I/O, L79P_Y	I/O, L79P_Y
I/O	5	AA10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N_Y	5	W10	XC2S200E, 300E, 400E, 600E	-	I/O, L55N	I/O, L73N	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y	I/O, L78N_Y
I/O, L#P_Y	5	Y10	XC2S200E, 300E, 400E, 600E	-	I/O, L55P	I/O, L73P	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y	I/O, L78P_Y
I/O, VREF Bank 5, L#N_Y	5	V10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 5, L54N	I/O, VREF Bank 5, L72N	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y	I/O, VREF Bank 5, L77N_Y
I/O, L#P_Y	5	U10	XC2S200E, 300E, 400E, 600E	-	I/O, L54P	I/O, L72P	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y	I/O, L77P_Y
I/O	5	U11	-	-	-	-	-	I/O	I/O	I/O
I/O	5	V11	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	5	W11	XC2S200E, 400E	-	I/O	I/O, L71N	I/O, L76N_Y	I/O, L76N	I/O, L76N_Y	I/O, L76N
I/O, L#P	5	Y11	XC2S200E, 400E	XC2S400E, 600E	-	I/O, L71P	I/O, L76P_Y	I/O, L76P	I/O, VREF Bank 5, L76P_Y	I/O, VREF Bank 5, L76P

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O	5	AA11	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#N	5	AB11	-	-	I/O (DLL), L53N	I/O (DLL), L70N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N	I/O (DLL), L75N
GCK1, I	5	AB12	-	-	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I	GCK1, I
GCK0, I	4	AA12	-	-	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I	GCK0, I
I/O (DLL), L#P	4	Y12	-	-	I/O (DLL), L53P	I/O (DLL), L70P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P	I/O (DLL), L75P
I/O	4	W12	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	V12	XC2S150E, 300E, 600E	-	-	I/O, L69N_Y	I/O, L74N	I/O, L74N_Y	I/O, L74N	I/O, L74N_Y
I/O, L#P	4	U12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L52N	I/O, L69P_Y	I/O, L74P	I/O, L74P_Y	I/O, VREF Bank 4, L74P	I/O, VREF Bank 4, L74P_Y
I/O, L#N	4	AB13	XC2S300E, 600E	-	I/O, L52P	I/O	I/O, L73N	I/O, L73N_Y	I/O, L73N	I/O, L73N_Y
I/O, L#P	4	AA13	XC2S300E, 600E	-	-	-	I/O, L73P	I/O, L73P_Y	I/O, L73P	I/O, L73P_Y
I/O	4	Y13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	W13	XC2S200E, 300E, 400E, 600E	-	I/O, L51N	I/O, L68N	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y	I/O, L72N_Y
I/O, VREF Bank 4, L#P	4	V13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L51P	I/O, VREF Bank 4, L68P	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y	I/O, VREF Bank 4, L72P_Y
I/O	4	U13	-	-	I/O, L50N	I/O, L67N	I/O	I/O	I/O	I/O
I/O, L#N	4	AB14	-	-	I/O, L50P	I/O, L67P	I/O, L71N	I/O, L71N	I/O, L71N	I/O, L71N
I/O, L#P	4	AA14	-	-	-	-	I/O, L71P	I/O, L71P	I/O, L71P	I/O, L71P
I/O	4	AB15	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	4	Y14	XC2S100E, 150E, 200E	-	I/O, L49N_Y	I/O, L66N_Y	I/O, L70N_Y	I/O, L70N	I/O, L70N	I/O, L70N
I/O, L#P	4	W14	XC2S100E, 150E, 200E	-	I/O, L49P_Y	I/O, L66P_Y	I/O, L70P_Y	I/O, L70P	I/O, L70P	I/O, L70P
I/O, L#N	4	U14	XC2S150E, 200E	-	-	I/O, L65N_Y	I/O, L69N_Y	I/O, L69N	I/O, L69N	I/O, L69N
I/O, L#P	4	V14	XC2S150E, 200E	-	-	I/O, L65P_Y	I/O, L69P_Y	I/O, L69P	I/O, L69P	I/O, L69P
I/O, L#N	4	AA15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48N_Y	I/O, L64N	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y	I/O, L68N_Y
I/O, L#P	4	Y15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L48P_Y	I/O, L64P	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y	I/O, L68P_Y
I/O, L#N	4	W15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L47N_Y	I/O, L63N	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y	I/O, L67N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, VREF Bank 4, L#P	4	V15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 4, L47P_Y	I/O, VREF Bank 4, L63P	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y	I/O, VREF Bank 4, L67P_Y
I/O	4	AB16	-	-	-	-	-	I/O	I/O	I/O
I/O	4	AB17	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#N	4	AA16	XC2S150E, 200E, 400E	XC2S600E	I/O, L46N	I/O, L62N_Y	I/O, L66N_Y	I/O, L66N	I/O, L66N_Y	I/O, VREF Bank 4, L66N
I/O, L#P	4	Y16	XC2S150E, 200E, 400E	-	I/O, L46P	I/O, L62P_Y	I/O, L66P_Y	I/O, L66P	I/O, L66P_Y	I/O, L66P
I/O, L#N	4	W16	XC2S150E, 200E	-	-	I/O, L61N_Y	I/O, L65N_Y	I/O, L65N	I/O, L65N	I/O, L65N
I/O, L#P	4	V16	XC2S150E, 200E	-	-	I/O, L61P_Y	I/O, L65P_Y	I/O, L65P	I/O, L65P	I/O, L65P
I/O, L#N_YY	4	AA17	All	-	I/O, L45N_YY	I/O, L60N_YY	I/O, L64N_YY	I/O, L64N_YY	I/O, L64N_YY	I/O, L64N_YY
I/O, VREF Bank 4, L#P_YY	4	Y17	All	All	I/O, VREF Bank 4, L45P_YY	I/O, VREF Bank 4, L60P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY	I/O, VREF Bank 4, L64P_YY
I/O	4	AB18	XC2S100E	-	I/O, L44N_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#N	4	W17	XC2S100E, 400E, 600E	-	I/O, L44P_Y	I/O, L59N	I/O, L63N	I/O, L63N	I/O, L63N_Y	I/O, L63N_Y
I/O, L#P	4	V17	XC2S400E, 600E	-	-	I/O, L59P	I/O, L63P	I/O, L63P	I/O, L63P_Y	I/O, L63P_Y
I/O	4	AA18	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	4	Y18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L43N_Y	I/O, L58N	I/O, L62N_Y	I/O, L62N_Y	I/O, L62N_Y	I/O, L62N_Y
I/O, L#P	4	W18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L43P_Y	I/O, L58P	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y	I/O, VREF Bank 4, L62P_Y
I/O	4	AB19	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#N	4	AA19	XC2S150E, 400E	-	-	I/O, L57N_Y	I/O, L61N	I/O, L61N	I/O, L61N_Y	I/O, L61N
I/O, L#P	4	Y19	XC2S150E, 400E	-	-	I/O, L57P_Y	I/O, L61P	I/O, L61P	I/O, L61P_Y	I/O, L61P
I/O	4	AB21	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N_YY	4	AB20	All	-	I/O, L42N_YY	I/O, L56N_YY	I/O, L60N_YY	I/O, L60N_YY	I/O, L60N_YY	I/O, L60N_YY
I/O, L#P_YY	4	AA20	All	-	I/O, L42P_YY	I/O, L56P_YY	I/O, L60P_YY	I/O, L60P_YY	I/O, L60P_YY	I/O, L60P_YY
DONE	3	W20	-	-	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$	-	Y21	-	-	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
I/O ($\overline{\text{INIT}}$), L#N_YY	3	W21	All	-	I/O ($\overline{\text{INIT}}$), L41N_YY	I/O ($\overline{\text{INIT}}$), L55N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY	I/O ($\overline{\text{INIT}}$), L59N_YY

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O (D7), L#P_YY	3	Y22	All	-	I/O (D7), L41P_YY	I/O (D7), L55P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY	I/O (D7), L59P_YY
I/O	3	W22	-	-	-	-	-	I/O	I/O	I/O
I/O	3	V21	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	V19	XC2S150E, 200E, 300E, 400E	-	-	I/O, L54N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N_Y	I/O, L58N
I/O, L#P	3	V20	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L54P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P_Y	I/O, L58P
I/O, L#N	3	V22	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L40N_Y	I/O, L53N	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N_Y	I/O, VREF Bank 3, L57N	I/O, VREF Bank 3, L57N_Y
I/O, L#P	3	U22	XC2S100E, 200E, 300E, 600E	-	I/O, L40P_Y	I/O, L53P	I/O, L57P_Y	I/O, L57P_Y	I/O, L57P	I/O, L57P_Y
I/O	3	U21	-	-	-	-	-	I/O	I/O	I/O
I/O	3	U20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	U18	XC2S100E, 200E, 300E, 600E	-	I/O, L39N_Y	I/O, L52N	I/O, L56N_Y	I/O, L56N_Y	I/O, L56N	I/O, L56N_Y
I/O, L#P	3	U19	XC2S100E, 200E, 300E, 600E	-	I/O, L39P_Y	I/O, L52P	I/O, L56P_Y	I/O, L56P_Y	I/O, L56P	I/O, L56P_Y
I/O, VREF Bank 3, L#N	3	T21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 3, L38N	I/O, VREF Bank 3, L51N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y	I/O, VREF Bank 3, L55N_Y
I/O, L#P	3	T22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L38P	I/O, L51P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y	I/O, L55P_Y
I/O	3	T20	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#N	3	T18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L50N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N_Y	I/O, L54N
I/O, L#P	3	T19	XC2S150E, 200E, 300E, 400E	-	I/O	I/O, L50P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P_Y	I/O, L54P
I/O, L#N	3	R21	XC2S100E, 150E, 300E, 600E	XC2S600E	I/O, L37N_Y	I/O, L49N_Y	I/O, L53N	I/O, L53N_Y	I/O, L53N	I/O, VREF Bank 3, L53N_Y
I/O, L#P	3	R22	XC2S100E, 150E, 300E, 600E	-	I/O, L37P_Y	I/O, L49P_Y	I/O, L53P	I/O, L53P_Y	I/O, L53P	I/O, L53P_Y
I/O	3	R20	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 3, L#N	3	R18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L36N	I/O, VREF Bank 3, L48N	I/O, VREF Bank 3, L52N	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y	I/O, VREF Bank 3, L52N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O (D6), L#P	3	R19	XC2S300E, 400E, 600E	-	I/O (D6), L36P	I/O (D6), L48P	I/O (D6), L52P	I/O (D6), L52P_Y	I/O (D6), L52P_Y	I/O (D6), L52P_Y
I/O (D5), L#N_YY	3	P22	All	-	I/O (D5), L35N_YY	I/O (D5), L47N_YY	I/O (D5), L51N_YY	I/O (D5), L51N_YY	I/O (D5) L51N_YY	I/O (D5), L51N_YY
I/O, L#P_YY	3	P21	All	-	I/O, L35P_YY	I/O, L47P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY	I/O, L51P_YY
I/O	3	P20	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	P18	XC2S150E, 200E, 300E, 400E	-	-	I/O, L46N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N_Y	I/O, L50N
I/O, L#P	3	P19	XC2S100E, 150E, 200E, 300E, 400E	-	I/O, L34N_Y	I/O, L46P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P_Y	I/O, L50P
I/O, L#N	3	N22	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L34P_Y	I/O, L45N_Y	I/O, L49N_Y	I/O, L49N_Y	I/O, L49N	I/O, L49N_Y
I/O, L#P	3	N21	XC2S150E, 200E, 300E, 600E	-	-	I/O, L45P_Y	I/O, L49P_Y	I/O, L49P_Y	I/O, L49P	I/O, L49P_Y
I/O	3	P17	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#N	3	N19	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33N_YY	I/O, L44N_YY	I/O, L48N_YY	I/O, L48N_YY	I/O, L48N	I/O, L48N_Y
I/O, L#P	3	N20	XC2S100E, 150E, 200E, 300E, 600E(1)	-	I/O, L33P_YY	I/O, L44P_YY	I/O, L48P_YY	I/O, L48P_YY	I/O, L48P	I/O, L48P_Y
I/O, VREF Bank 3, L#N	3	N18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 3, L32N	I/O, VREF Bank 3, L43N	I/O, VREF Bank 3, L47N	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y	I/O, VREF Bank 3, L47N_Y
I/O (D4), L#P	3	N17	XC2S300E, 400E, 600E	-	I/O (D4), L32P	I/O (D4), L43P	I/O (D4), L47P	I/O (D4), L47P_Y	I/O (D4), L47P_Y	I/O (D4), L47P_Y
I/O	3	M22	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	3	M20	XC2S300E, 400E	-	-	-	I/O, L46N	I/O, L46N_Y	I/O, L46N_Y	I/O, L46N
I/O, L#P	3	M21	XC2S100E, 150E, 300E, 400E	-	I/O, L31N_Y	I/O, L42N_Y	I/O, L46P	I/O, L46P_Y	I/O, L46P_Y	I/O, L46P
I/O, L#N	3	M18	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L31P_Y	I/O, L42P_Y	I/O, L45N_Y	I/O, L45N_Y	I/O, VREF Bank 3, L45N	I/O, VREF Bank 3, L45N_Y
I/O, L#P	3	M19	XC2S200E, 300E, 600E	-	-	I/O	I/O, L45P_Y	I/O, L45P_Y	I/O, L45P	I/O, L45P_Y
I/O	3	M17	-	-	-	-	-	I/O	I/O	I/O
I/O (TRDY)	3	L22	-	-	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)	I/O (TRDY)

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O (IRDY), L#N_YY	2	L21	All	-	I/O (IRDY), L30N_YY	I/O (IRDY), L41N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY	I/O (IRDY), L44N_YY
I/O, L#P_YY	2	L20	All	-	I/O, L30P_YY	I/O, L41P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY	I/O, L44P_YY
I/O	2	L19	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	2	L18	XC2S200E, 300E, 600E	-	-	I/O	I/O, L43N_Y	I/O, L43N_Y	I/O, L43N	I/O, L43N_Y
I/O, L#P	2	L17	XC2S100E, 150E, 200E, 300E, 600E	XC2S400E, 600E	I/O, L29N_Y	I/O, L40N_Y	I/O, L43P_Y	I/O, L43P_Y	I/O, VREF Bank 2, L43P	I/O, VREF Bank 2, L43P_Y
I/O, L#N	2	K22	XC2S100E, 150E, 300E, 400E	-	I/O, L29P_Y	I/O, L40P_Y	I/O, L42N	I/O, L42N_Y	I/O, L42N_Y	I/O, L42N
I/O, L#P	2	K21	XC2S300E, 400E	-	-	-	I/O, L42P	I/O, L42P_Y	I/O, L42P_Y	I/O, L42P
I/O	2	K20	-	-	-	-	-	I/O	I/O	I/O
I/O (D3)	2	K19	-	-	I/O (D3)	I/O (D3), L39N	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
I/O, VREF Bank 2, L#N	2	K18	XC2S100E, 200E, 400E	All	I/O, VREF Bank 2, L28N_Y	I/O, VREF Bank 2, L39P	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N	I/O, VREF Bank 2, L41N_Y	I/O, VREF Bank 2, L41N
I/O, L#P	2	K17	XC2S100, 150E, 200E, 400E	-	I/O, L28P_Y	I/O, L38N_Y	I/O, L41P_Y	I/O, L41P	I/O, L41P_Y	I/O, L41P
I/O, L#N	2	J22	XC2S150E, 300E, 600E	-	I/O	I/O, L38P_Y	I/O, L40N	I/O, L40N_Y	I/O, L40N	I/O, L40N_Y
I/O, L#P	2	J21	XC2S300E, 600E	-	-	-	I/O, L40P	I/O, L40P_Y	I/O, L40P	I/O, L40P_Y
I/O, L#N	2	J20	XC2S150E, 200E, 300E, 600E	-	-	I/O, L37N_Y	I/O, L39N_Y	I/O, L39N_Y	I/O, L39N	I/O, L39N_Y
I/O, L#P	2	J19	XC2S100E, 150E, 200E, 300E, 600E	-	I/O, L27N_Y	I/O, L37P_Y	I/O, L39P_Y	I/O, L39P_Y	I/O, L39P	I/O, L39P_Y
I/O	2	H22	XC2S100E, 150E	-	I/O, L27P_Y	I/O, L36N_Y	I/O	I/O	I/O	I/O
I/O, L#N	2	J18	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L36P_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y	I/O, L38N_Y
I/O, L#P	2	J17	XC2S200E, 300E, 400E, 600E	-	-	-	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y	I/O, L38P_Y
I/O, L#N	2	H21	XC2S150E, 200E, 300E, 400E, 600E	-	I/O	I/O, L35N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y	I/O, L37N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O (D2), L#P	2	H20	XC2S150E, 200E, 300E, 400E, 600E	-	I/O (D2)	I/O (D2), L35P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y	I/O (D2), L37P_Y
I/O (D1), L#N	2	H19	XC2S300E, 400E, 600E	-	I/O (D1), L26N	I/O (D1), L34N	I/O (D1), L36N	I/O (D1), L36N_Y	I/O (D1), L36N_Y	I/O (D1), L36N_Y
I/O, VREF Bank 2, L#P	2	H18	XC2S300E, 400E, 600E	All	I/O, VREF Bank 2, L26P	I/O, VREF Bank 2, L34P	I/O, VREF Bank 2, L36P	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y	I/O, VREF Bank 2, L36P_Y
I/O	2	G22	-	-	-	-	-	I/O	I/O	I/O
I/O	2	F22	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#N	2	G21	XC2S200E, 400E, 600E	XC2S600E	I/O, L25N	I/O, L33N	I/O, L35N_Y	I/O, L35N	I/O, L35N_Y	I/O, VREF Bank 2, L35N_Y
I/O, L#P	2	G20	XC2S200E, 400E, 600E	-	I/O, L25P	I/O, L33P	I/O, L35P_Y	I/O, L35P	I/O, L35P_Y	I/O, L35P_Y
I/O, L#N	2	G19	XC2S150E, 300E	-	-	I/O, L32N_Y	I/O, L34N	I/O, L34N_Y	I/O, L34N	I/O, L34N
I/O, L#P	2	G18	XC2S150E, 300E	-	-	I/O, L32P_Y	I/O, L34P	I/O, L34P_Y	I/O, L34P	I/O, L34P
I/O, L#N	2	E22	XC2S150E, 200E, 300E, 400E, 600E	-	I/O, L24N	I/O, L31N_Y	I/O, L33N_Y	I/O, L33N_Y	I/O, L33N_Y	I/O, L33N_Y
I/O, VREF Bank 2, L#P	2	F21	XC2S150E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 2, L24P	I/O, VREF Bank 2, L31P_Y	I/O, VREF Bank 2, L33P_Y	I/O, VREF Bank 2, L33P_Y	I/O, VREF Bank 2, L33P_Y	I/O, VREF Bank 2, L33P_Y
I/O	2	E21	XC2S100E	-	I/O, L23N_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#N	2	F20	XC2S100E, 150E, 200E, 300E, 400E, 600E	-	I/O, L23P_Y	I/O, L30N_Y	I/O, L32N_Y	I/O, L32N_Y	I/O, L32N_Y	I/O, L32N_Y
I/O, L#P	2	F19	XC2S150E, 200E, 300E, 400E, 600E	-	-	I/O, L30P_Y	I/O, L32P_Y	I/O, L32P_Y	I/O, L32P_Y	I/O, L32P_Y
I/O	2	F18	-	-	-	-	-	I/O	I/O	I/O
I/O, L#N	2	D22	XC2S100E, 200E, 300E, 600E	-	I/O, L22N_Y	I/O, L29N	I/O, L31N_Y	I/O, L31N_Y	I/O, L31N	I/O, L31N_Y
I/O, L#P	2	D21	XC2S100E, 200E, 300E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L22P_Y	I/O, L29P	I/O, VREF Bank 2, L31P_Y	I/O, VREF Bank 2, L31P_Y	I/O, VREF Bank 2, L31P	I/O, VREF Bank 2, L31P_Y
I/O, L#N	2	E20	XC2S200E, 300E, 400E	-	I/O	I/O, L28N	I/O, L30N_Y	I/O, L30N_Y	I/O, L30N_Y	I/O, L30N
I/O, L#P	2	E19	XC2S200E, 300E, 400E	-	-	I/O, L28P	I/O, L30P_Y	I/O, L30P_Y	I/O, L30P_Y	I/O, L30P
I/O	2	D20	-	-	-	-	-	I/O	I/O	I/O

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O (DIN, D0), L#N_YY	2	C22	All	-	I/O (DIN, D0), L21N_YY	I/O (DIN, D0), L27N_YY	I/O (DIN, D0), L29N_YY	I/O (DIN, D0), L29N_YY	I/O (DIN, D0), L29N_YY	I/O (DIN, D0), L29N_YY
I/O (DOUT, BUSY), L#P_YY	2	C21	All	-	I/O (DOUT, BUSY), L21P_YY	I/O (DOUT, BUSY), L27P_YY	I/O (DOUT, BUSY), L29P_YY	I/O (DOUT, BUSY), L29P_YY	I/O (DOUT, BUSY), L29P_YY	I/O (DOUT, BUSY), L29P_YY
CCLK	2	B22	-	-	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
TDO	2	A21	-	-	TDO	TDO	TDO	TDO	TDO	TDO
TDI	-	C19	-	-	TDI	TDI	TDI	TDI	TDI	TDI
I/O ($\overline{CS}$), L#P_YY	1	B20	All	-	I/O ($\overline{CS}$), L20P_YY	I/O ($\overline{CS}$), L26P_YY	I/O ($\overline{CS}$), L28P_YY	I/O ($\overline{CS}$), L28P_YY	I/O ($\overline{CS}$), L28P_YY	I/O ($\overline{CS}$), L28P_YY
I/O ($\overline{WRITE}$), L#N_YY	1	A20	All	-	I/O ($\overline{WRITE}$), L20N_YY	I/O ($\overline{WRITE}$), L26N_YY	I/O ($\overline{WRITE}$), L28N_YY	I/O ($\overline{WRITE}$), L28N_YY	I/O ($\overline{WRITE}$), L28N_YY	I/O ($\overline{WRITE}$), L28N_YY
I/O	1	D18	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C18	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	B19	XC2S200E, 300E, 400E, 600E	-	-	I/O, L25P	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y	I/O, L27P_Y
I/O, L#N	1	A19	XC2S200E, 300E, 400E, 600E	-	I/O	I/O, L25N	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y	I/O, L27N_Y
I/O, L#P	1	B18	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L19P_Y	I/O, L24P	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y	I/O, VREF Bank 1, L26P_Y
I/O, L#N	1	A18	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L19N_Y	I/O, L24N	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y	I/O, L26N_Y
I/O	1	D17	-	-	-	-	-	I/O	I/O	I/O
I/O	1	C17	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P_YY	1	B17	All	-	I/O, L18P_YY	I/O, L23P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY	I/O, L25P_YY
I/O, L#N_YY	1	A17	All	-	I/O, L18N_YY	I/O, L23N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY	I/O, L25N_YY
I/O, VREF Bank 1, L#P_YY	1	E16	All	All	I/O, VREF Bank 1, L17P_YY	I/O, VREF Bank 1, L22P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY	I/O, VREF Bank 1, L24P_YY
I/O, L#N_YY	1	E17	All	-	I/O, L17N_YY	I/O, L22N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY	I/O, L24N_YY
I/O	1	E15	-	-	-	I/O	I/O	I/O	I/O	I/O
I/O, L#P	1	D16	XC2S300E, 600E	-	-	I/O, L21P	I/O, L23P	I/O, L23P_Y	I/O, L23P	I/O, L23P_Y
I/O, L#N	1	C16	XC2S300E, 600E	-	I/O	I/O, L21N	I/O, L23N	I/O, L23N_Y	I/O, L23N	I/O, L23N_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#P	1	B16	XC2S100E, 300E, 600E	XC2S600E	I/O, L16P_Y	I/O, L20P	I/O, L22P	I/O, L22P_Y	I/O, L22P	I/O, VREF Bank 1, L22P_Y
I/O, L#N	1	A16	XC2S100E, 300E, 600E	-	I/O, L16N_Y	I/O, L20N	I/O, L22N	I/O, L22N_Y	I/O, L22N	I/O, L22N_Y
I/O	1	F14	-	-	-	-	-	I/O	I/O	I/O
I/O, VREF Bank 1, L#P	1	D15	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L15P_Y	I/O, VREF Bank 1, L19P	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y	I/O, VREF Bank 1, L21P_Y
I/O, L#N	1	C15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L15N_Y	I/O, L19N	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y	I/O, L21N_Y
I/O, L#P	1	B15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14P_Y	I/O, L18P	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y	I/O, L20P_Y
I/O, L#N	1	A15	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L14N_Y	I/O, L18N	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y	I/O, L20N_Y
I/O	1	E14	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L17P_Y	I/O, L19P	I/O, L19P_Y	I/O, L19P_Y	I/O, L19P_Y
I/O, L#N	1	C14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13P_Y	I/O, L17N_Y	I/O, L19N	I/O, L19N_Y	I/O, L19N_Y	I/O, L19N_Y
I/O, L#P	1	B14	XC2S100E, 150E, 300E, 400E, 600E	-	I/O, L13N_Y	I/O, L16P_Y	I/O, L18P	I/O, L18P_Y	I/O, L18P_Y	I/O, L18P_Y
I/O, L#N	1	A14	XC2S150E, 300E, 400E, 600E	-	-	I/O, L16N_Y	I/O, L18N	I/O, L18N_Y	I/O, L18N_Y	I/O, L18N_Y
I/O	1	E13	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	1	D13	XC2S200E, 300E, 400E, 600E	-	I/O, L12P	I/O, L15P	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y	I/O, L17P_Y
I/O, L#N	1	C13	XC2S200E, 300E, 400E, 600E	-	I/O, L12N	I/O, L15N	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y	I/O, L17N_Y
I/O, VREF Bank 1, L#P	1	B13	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 1, L11P	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y	I/O, VREF Bank 1, L16P_Y
I/O, L#N	1	A13	XC2S200E, 300E, 400E, 600E	-	I/O, L11N	I/O, L14N	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y	I/O, L16N_Y
I/O	1	F13	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	1	C12	XC2S300E, 600E	-	-	-	I/O, L15P	I/O, L15P_Y	I/O, L15P	I/O, L15P_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name			LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank	Pin			100E	150E	200E	300E	400E	600E
I/O, L#N	1	B12	XC2S300E, 600E	-	I/O, L10P	I/O	I/O, L15N	I/O, L15N_Y	I/O, L15N	I/O, L15N_Y
I/O, L#P	1	D12	XC2S150E, 300E, 600E	XC2S400E, 600E	I/O, L10N	I/O, L13P_Y	I/O, L14P	I/O, L14P_Y	I/O, VREF Bank 1, L14P	I/O, VREF Bank 1, L14P_Y
I/O, L#N	1	E12	XC2S150E, 300E, 600E	-	-	I/O, L13N_Y	I/O, L14N	I/O, L14N_Y	I/O, L14N	I/O, L14N_Y
I/O	1	F12	-	-	-	-	-	I/O	I/O	I/O
I/O (DLL), L#P	1	A12	-	-	I/O (DLL), L9P	I/O (DLL), L12P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P	I/O (DLL), L13P
GCK2, I	1	A11	-	-	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I	GCK2, I
GCK3, I	0	C11	-	-	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I	GCK3, I
I/O (DLL), L#N	0	B11	-	-	I/O (DLL), L9N	I/O (DLL), L12N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N	I/O (DLL), L13N
I/O	0	D11	-	-	-	-	-	I/O	I/O	I/O
I/O	0	F11	-	XC2S400E, 600E	-	-	I/O	I/O	I/O, VREF Bank 0	I/O, VREF Bank 0
I/O, L#P	0	A10	XC2S300E, 600E	-	I/O	I/O, L11P	I/O, L12P	I/O, L12P_Y	I/O, L12P	I/O, L12P_Y
I/O, L#N	0	B10	XC2S300E, 600E	-	-	I/O, L11N	I/O, L12N	I/O, L12N_Y	I/O, L12N	I/O, L12N_Y
I/O	0	E11	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	0	C10	XC2S200E, 300E, 400E, 600E	-	I/O, L8P	I/O, L10P	I/O, L11P_Y	I/O, L11P_Y	I/O, L11P_Y	I/O, L11P_Y
I/O, VREF Bank 0, L#N	0	D10	XC2S200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L8N	I/O, VREF Bank 0, L10N	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y	I/O, VREF Bank 0, L11N_Y
I/O	0	F10	-	-	I/O, L7P	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A9	-	-	I/O, L7N	I/O	I/O, L10P	I/O, L10P	I/O, L10P	I/O, L10P
I/O, L#N	0	B9	-	-	-	-	I/O, L10N	I/O, L10N	I/O, L10N	I/O, L10N
I/O	0	E10	-	-	-	-	I/O	I/O	I/O	I/O
I/O, L#P	0	C9	XC2S100E, 150E, 200E	-	I/O, L6P_Y	I/O, L9P_Y	I/O, L9P_Y	I/O, L9P	I/O, L9P	I/O, L9P
I/O, L#N	0	D9	XC2S100E, 150E, 200E	-	I/O, L6N_Y	I/O, L9N_Y	I/O, L9N_Y	I/O, L9N	I/O, L9N	I/O, L9N
I/O, L#P	0	F9	XC2S150E, 200E	-	-	I/O, L8P_Y	I/O, L8P_Y	I/O, L8P	I/O, L8P	I/O, L8P
I/O, L#N	0	E9	XC2S150E, 200E	-	-	I/O, L8N_Y	I/O, L8N_Y	I/O, L8N	I/O, L8N	I/O, L8N
I/O, L#P	0	A8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5P_Y	I/O, L7P	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y	I/O, L7P_Y

FG456 Pinouts (XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	V_{REF} Option	Device-Specific Pinouts: XC2S					
Function	Bank				100E	150E	200E	300E	400E	600E
I/O, L#N	0	B8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L5N_Y	I/O, L7N	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y	I/O, L7N_Y
I/O, L#P	0	C8	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L4P_Y	I/O, L6P	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y	I/O, L6P_Y
I/O, VREF Bank 0, L#N	0	D8	XC2S100E, 200E, 300E, 400E, 600E	All	I/O, VREF Bank 0, L4N_Y	I/O, VREF Bank 0, L6N	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y	I/O, VREF Bank 0, L6N_Y
I/O	0	A7	-	-	-	-	-	I/O	I/O	I/O
I/O	0	B7	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	C7	XC2S150E, 200E	XC2S600E	I/O, L3P	I/O, L5P_Y	I/O, L5P_Y	I/O, L5P	I/O, L5P	I/O, VREF Bank 0, L5P
I/O, L#N	0	D7	XC2S150E, 200E	-	I/O, L3N	I/O, L5N_Y	I/O, L5N_Y	I/O, L5N	I/O, L5N	I/O, L5N
I/O, L#P	0	E8	XC2S150E, 200E	-	-	I/O, L4P_Y	I/O, L4P_Y	I/O, L4P	I/O, L4P	I/O, L4P
I/O, L#N	0	E7	XC2S150E, 200E	-	-	I/O, L4N_Y	I/O, L4N_Y	I/O, L4N	I/O, L4N	I/O, L4N
I/O, L#P_YY	0	A6	All	-	I/O, L2P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L#N_YY	0	B6	All	All	I/O, VREF Bank 0, L2N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O	0	C6	XC2S100E	-	I/O, L1P_Y	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A5	XC2S100E	-	I/O, L1N_Y	I/O, L2P	I/O, L2P	I/O, L2P	I/O, L2P	I/O, L2P
I/O, L#N	0	B5	-	-	-	I/O, L2N	I/O, L2N	I/O, L2N	I/O, L2N	I/O, L2N
I/O	0	D6	-	-	-	-	-	I/O	I/O	I/O
I/O, L#P	0	B4	XC2S100E, 200E, 300E, 400E, 600E	-	I/O, L0P_Y	I/O, L1P	I/O, L1P_Y	I/O, L1P_Y	I/O, L1P_Y	I/O, L1P_Y
I/O, L#N	0	C5	XC2S100E, 200E, 300E, 400E, 600E	XC2S200E, 300E, 400E, 600E	I/O, L0N_Y	I/O, L1N	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y	I/O, VREF Bank 0, L1N_Y
I/O	0	A4	-	-	I/O	I/O	I/O	I/O	I/O	I/O
I/O, L#P	0	A3	XC2S150E, 400E, 600E	-	-	I/O, L0P_Y	I/O, L0P	I/O, L0P	I/O, L0P_Y	I/O, L0P_Y
I/O, L#N	0	B3	XC2S150E, 400E, 600E	-	-	I/O, L0N_Y	I/O, L0N	I/O, L0N	I/O, L0N_Y	I/O, L0N_Y
I/O	0	C4	-	-	-	-	-	I/O	I/O	I/O
I/O	0	D5	-	-	I/O	I/O	I/O	I/O	I/O	I/O
TCK	-	E6	-	-	TCK	TCK	TCK	TCK	TCK	TCK

Notes:
1. Although designated with the _YY suffix in the XC2S100E, XC2S150E, XC2S200E, and XC2S300E, these differential pairs are not asynchronous in the XC2S400E.

FG456 Differential Clock Pins

Clock	Bank	P		N	
		Pin	Name	Pin	Name
GCK0	4	AA12	GCK0, I	Y12	I/O (DLL), L#P
GCK1	5	AB12	GCK1, I	AB11	I/O (DLL), L#N
GCK2	1	A11	GCK2, I	A12	I/O (DLL), L#P
GCK3	0	C11	GCK3, I	B11	I/O (DLL), L#N

Additional FG456 Package Pins

VCCINT Pins								
D4(1)	D19(1)	E5	E18	F6	F17	G7	G8	G15
G16	H7	H16	R7	R16	T7	T8	T15	T16
U6	U17	V5	V18	W4(1)	W19(1)	-	-	-
VCCO Bank 0 Pins								
F7	F8	G9	G10	-	-	-	-	-
VCCO Bank 1 Pins								
F15	F16	G13	G14	-	-	-	-	-
VCCO Bank 2 Pins								
G17	H17	J16	K16	-	-	-	-	-
VCCO Bank 3 Pins								
N16	P16	R17	T17	-	-	-	-	-
VCCO Bank 4 Pins								
T13	T14	U15	U16	-	-	-	-	-
VCCO Bank 5 Pins								
T9	T10	U7	U8	-	-	-	-	-
VCCO Bank 6 Pins								
N7	P7	R6	T6	-	-	-	-	-
VCCO Bank 7 Pins								
G6	H6	J7	K7	-	-	-	-	-
GND Pins								
A1	A2(2)	A22	B1(2)	B2	B21	C3	C20	G11
G12	J9	J10	J11	J12	J13	J14	K9	K10
K11	K12	K13	K14	L7	L9	L10	L11	L12
L13	L14	L16	M7	M9	M10	M11	M12	M13
M14	M16	N9	N10	N11	N12	N13	N14	P9
P10	P11	P12	P13	P14	T11	T12	Y20	Y3
Y4(2)	AA2	AA4(2)	AA21	AA22(2)	AB1	AB22	-	-
Not Connected Pins								
A2(2)	B1(2)	D4(1)	D19(1)	W4(1)	W19(1)	Y4(2)	AA4(2)	AA22(2)

Notes:

1. VCCINT connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E.
2. GND connections in XC2S400E and XC2S600E. No Connects (no internal connection) in XC2S100E, XC2S150E, XC2S200E, and XC2S300E

FG676 Pinouts (XC2S400E, XC2S600E)

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
TMS	-	B1	-	-	TMS	TMS
I/O	7	D3	-	-	I/O	I/O
I/O, L204P	7	C2	-	-	-	I/O, L204P
I/O, L204N	7	C1	-	-	-	I/O, L204N
I/O, L203P	7	D2	XC2S600E	-	-	I/O, L203P_Y
I/O, L203N	7	D1	XC2S600E	-	I/O	I/O, L203N_Y
I/O, L202P_YY	7	E2	All	-	I/O, L202P_YY	I/O, L202P_YY
I/O, L202N_YY	7	E1	All	-	I/O, L202N_YY	I/O, L202N_YY
I/O, L201P	7	E4	XC2S400E	-	I/O, L201P_Y	I/O, L201P
I/O, L201N	7	F5	XC2S400E	-	I/O, L201N_Y	I/O, L201N
I/O, VREF Bank 7, L200P	7	F4	XC2S600E	All	I/O, VREF Bank 7, L200P	I/O, VREF Bank 7, L200P_Y
I/O, L200N	7	F3	XC2S600E	-	I/O, L200N	I/O, L200N_Y
I/O, L199P	7	F2	XC2S600E	-	-	I/O, L199P_Y
I/O, L199N	7	F1	XC2S600E	-	I/O	I/O, L199N_Y
I/O, L198P	7	G6	XC2S400E	-	I/O, L198P_Y	I/O, L198P
I/O, L198N	7	G5	XC2S400E	-	I/O, L198N_Y	I/O, L198N
I/O, L197P	7	G4	XC2S600E	-	I/O, L197P	I/O, L197P_Y
I/O, L197N	7	G3	XC2S600E	-	I/O, L197N	I/O, L197N_Y
I/O, VREF Bank 7, L196P_YY	7	G2	All	All	I/O, VREF Bank 7, L196P_YY	I/O, VREF Bank 7, L196P_YY
I/O, L196N_YY	7	G1	All	-	I/O, L196N_YY	I/O, L196N_YY
I/O	7	H7	-	-	I/O	I/O
I/O, L195P_YY	7	H6	All	-	I/O, L195P_YY	I/O, L195P_YY
I/O, L195N_YY	7	H5	All	-	I/O, L195N_YY	I/O, L195N_YY
I/O	7	J8	-	-	-	I/O
I/O, L194P	7	H2	XC2S400E	-	I/O, L194P_Y	I/O, L194P
I/O, L194N	7	H1	XC2S400E	-	I/O, L194N_Y	I/O, L194N
I/O, L193P	7	J7	XC2S600E	XC2S600E	I/O	I/O, VREF Bank 7, L193P_Y
I/O, L193N	7	J6	XC2S600E	-	-	I/O, L193N_Y
I/O	7	J5	-	-	I/O	I/O
I/O, L192P_YY	7	J4	All	-	I/O, L192P_YY	I/O, L192P_YY
I/O, L192N_YY	7	J3	All	-	I/O, L192N_YY	I/O, L192N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	7	K5	-	-	I/O	I/O
I/O, VREF Bank 7, L191P_YY	7	J2	All	All	I/O, VREF Bank 7, L191P_YY	I/O, VREF Bank 7, L191P_YY
I/O, L191N_YY	7	J1	All	-	I/O, L191N_YY	I/O, L191N_YY
I/O, L190P_YY	7	K8	All	-	I/O, L190P_YY	I/O, L190P_YY
I/O, L190N_YY	7	K7	All	-	I/O, L190N_YY	I/O, L190N_YY
I/O	7	K4	-	-	-	I/O
I/O, L189P_YY	7	K3	All	-	I/O, L189P_YY	I/O, L189P_YY
I/O, L189N_YY	7	K2	All	-	I/O, L189N_YY	I/O, L189N_YY
I/O	7	K1	-	-	-	I/O
I/O, L188P	7	L8	XC2S400E	-	I/O, L188P_Y	I/O, L188P
I/O, L188N	7	L7	XC2S400E	-	I/O, L188N_Y	I/O, L188N
I/O, L187P	7	L6	XC2S600E	-	I/O, L187P	I/O, L187P_Y
I/O, L187N	7	L5	XC2S600E	-	I/O, L187N	I/O, L187N_Y
I/O	7	L3	-	-	-	I/O
I/O, L186P	7	L2	XC2S600E	-	I/O, L186P	I/O, L186P_Y
I/O, L186N	7	L1	XC2S600E	-	I/O, L186N	I/O, L186N_Y
I/O	7	M9	-	-	-	I/O
I/O, L185P	7	M8	XC2S600E	-	I/O, L185P	I/O, L185P_Y
I/O, L185N	7	M7	XC2S600E	-	I/O, L185N	I/O, L185N_Y
I/O, VREF Bank 7, L184P_YY	7	M6	All	All	I/O, VREF Bank 7, L184P_YY	I/O, VREF Bank 7, L184P_YY
I/O, L184N_YY	7	M5	All	-	I/O, L184N_YY	I/O, L184N_YY
I/O	7	M4	-	-	-	I/O
I/O, L183P_YY	7	M2	All	-	I/O, L183P_YY	I/O, L183P_YY
I/O, L183N_YY	7	M1	All	-	I/O, L183N_YY	I/O, L183N_YY
I/O	7	N9	-	-	-	I/O
I/O, L182P	7	N8	XC2S400E	-	I/O, L182P_Y	I/O, L182P
I/O, L182N	7	N7	XC2S400E	-	I/O, L182N_Y	I/O, L182N
I/O, VREF Bank 7, L181P	7	N6	XC2S600E	All	I/O, VREF Bank 7, L181P	I/O, VREF Bank 7, L181P_Y
I/O, L181N	7	N5	XC2S600E	-	I/O, L181N	I/O, L181N_Y
I/O	7	N4	-	-	-	I/O
I/O, L180P_YY	7	N3	All	-	I/O, L180P_YY	I/O, L180P_YY
I/O, L180N_YY	7	N2	All	-	I/O, L180N_YY	I/O, L180N_YY
I/O	7	N1	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L179P_YY	7	P1	All	-	I/O, L179P_YY	I/O, L179P_YY
I/O (IRDY), L179N_YY	7	P2	All	-	I/O (IRDY), L179N_YY	I/O (IRDY), L179N_YY
I/O (TRDY), L178P	6	P3	XC2S600E	-	I/O (TRDY)	I/O (TRDY), L178P_Y
I/O, L178N	6	P4	XC2S600E	-	-	I/O, L178N_Y
I/O, L177P	6	P5	XC2S600E	-	-	I/O, L177P_Y
I/O, L177N	6	P6	XC2S600E	-	I/O	I/O, L177N_Y
I/O	6	P7	-	-	I/O	I/O
I/O, L176P	6	P8	XC2S600E	-	I/O, L176P	I/O, L176P_Y
I/O, VREF Bank 6, L176N	6	P9	XC2S600E	All	I/O, VREF Bank 6, L176N	I/O, VREF Bank 6, L176N_Y
I/O, L175P	6	R1	XC2S400E	-	I/O, L175P_Y	I/O, L175P
I/O, L175N	6	R2	XC2S400E	-	I/O, L175N_Y	I/O, L175N
I/O	6	R4	-	-	-	I/O
I/O, L174P_YY	6	R5	All	-	I/O, L174P_YY	I/O, L174P_YY
I/O, L174N_YY	6	R6	All	-	I/O, L174N_YY	I/O, L174N_YY
I/O	6	R7	-	-	-	I/O
I/O, L173P_YY	6	R8	All	-	I/O, L173P_YY	I/O, L173P_YY
I/O, VREF Bank 6, L173N_YY	6	R9	All	All	I/O, VREF Bank 6, L173N_YY	I/O, VREF Bank 6, L173N_YY
I/O, L172P	6	T1	XC2S600E	-	I/O, L172P	I/O, L172P_Y
I/O, L172N	6	T2	XC2S600E	-	I/O, L172N	I/O, L172N_Y
I/O	6	T3	-	-	-	I/O
I/O, L171P	6	T5	XC2S600E	-	I/O, L171P	I/O, L171P_Y
I/O, L171N	6	T6	XC2S600E	-	I/O, L171N	I/O, L171N_Y
I/O	6	U1	-	-	-	I/O
I/O, L170P	6	T7	XC2S600E	-	I/O, L170P	I/O, L170P_Y
I/O, L170N	6	T8	XC2S600E	-	I/O, L170N	I/O, L170N_Y
I/O, L169P	6	U2	XC2S400E	-	I/O, L169P_Y	I/O, L169P
I/O, L169N	6	U3	XC2S400E	-	I/O, L169N_Y	I/O, L169N
I/O	6	U7	-	-	-	I/O
I/O, L168P	6	U4	XC2S600E	-	-	I/O, L168P_Y
I/O, L168N	6	U5	XC2S600E	-	I/O	I/O, L168N_Y
I/O	6	U8	-	-	I/O	I/O
I/O, L167P_YY	6	V1	All	-	I/O, L167P_YY	I/O, L167P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L167N_YY	6	V2	All	-	I/O, L167N_YY	I/O, L167N_YY
I/O	6	V3	-	-	I/O	I/O
I/O, VREF Bank 6, L166P_YY	6	V4	All	All	I/O, VREF Bank 6, L166P_YY	I/O, VREF Bank 6, L166P_YY
I/O, L166N_YY	6	V5	All	-	I/O, L166N_YY	I/O, L166N_YY
I/O, L165P_YY	6	V6	All	-	I/O, L165P_YY	I/O, L165P_YY
I/O, L165N_YY	6	V7	All	-	I/O, L165N_YY	I/O, L165N_YY
I/O	6	V8	-	-	-	I/O
I/O, L164P	6	W1	XC2S600E	-	I/O, L164P	I/O, L164P_Y
I/O, L164N	6	W2	XC2S600E	XC2S600E	I/O, L164N	I/O, VREF Bank 6, L164N_Y
I/O, L163P	6	W5	XC2S400E	-	I/O, L163P_Y	I/O, L163P
I/O, L163N	6	W6	XC2S400E	-	I/O, L163N_Y	I/O, L163N
I/O	6	W7	-	-	I/O	I/O
I/O, L162P_YY	6	Y1	All	-	I/O, L162P_YY	I/O, L162P_YY
I/O, L162N_YY	6	Y2	All	-	I/O, L162N_YY	I/O, L162N_YY
I/O	6	Y3	-	-	-	I/O
I/O, L161P_YY	6	Y4	All	-	I/O, L161P_YY	I/O, L161P_YY
I/O, VREF Bank 6, L161N_YY	6	Y5	All	All	I/O, VREF Bank 6, L161N_YY	I/O, VREF Bank 6, L161N_YY
I/O	6	Y6	-	-	I/O	I/O
I/O, L160P_YY	6	AA1	All	-	I/O, L160P_YY	I/O, L160P_YY
I/O, L160N_YY	6	AA2	All	-	I/O, L160N_YY	I/O, L160N_YY
I/O, L159P	6	AA3	XC2S600E	-	I/O, L159P	I/O, L159P_Y
I/O, L159N	6	AA4	XC2S600E	-	I/O, L159N	I/O, L159N_Y
I/O	6	Y7	-	-	-	I/O
I/O, L158P	6	AA5	XC2S600E	-	I/O, L158P	I/O, L158P_Y
I/O, VREF Bank 6, L158N	6	AB5	XC2S600E	All	I/O, VREF Bank 6, L158N	I/O, VREF Bank 6, L158N_Y
I/O, L157P	6	AB1	XC2S400E	-	I/O, L157P_Y	I/O, L157P
I/O, L157N	6	AB2	XC2S400E	-	I/O, L157N_Y	I/O, L157N
I/O, L156P	6	AC1	XC2S600E	-	-	I/O, L156P_Y
I/O, L156N	6	AC2	XC2S600E	-	I/O	I/O, L156N_Y
I/O, L155P_YY	6	AC3	All	-	I/O, L155P_YY	I/O, L155P_YY
I/O, L155N_YY	6	AB4	All	-	I/O, L155N_YY	I/O, L155N_YY
I/O, L154P	6	AD1	-	-	-	I/O, L154P

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L154N	6	AD2	-	-	-	I/O, L154N
I/O, L153P_YY	6	AE1	All	-	I/O, L153P_YY	I/O, L153P_YY
I/O, L153N_YY	6	AF2	All	-	I/O, L153N_YY	I/O, L153N_YY
M1	-	AE3	-	-	M1	M1
M0	-	AF3	-	-	M0	M0
M2	-	AD4	-	-	M2	M2
I/O	5	AC5	-	-	I/O	I/O
I/O, L152N	5	AE4	-	-	I/O	I/O, L152N
I/O, L152P	5	AF4	-	-	-	I/O, L152P
I/O, L151N	5	AE5	-	-	-	I/O, L151N
I/O, L151P	5	AF5	-	-	I/O	I/O, L151P
I/O, L150N	5	AA6	XC2S400E	-	I/O, L150N_Y	I/O, L150N
I/O, L150P	5	AB6	XC2S400E	-	I/O, L150P_Y	I/O, L150P
I/O, L149N_YY	5	AC6	All	-	I/O, L149N_YY	I/O, L149N_YY
I/O, L149P_YY	5	AD6	All	-	I/O, L149P_YY	I/O, L149P_YY
I/O, VREF Bank 5, L148N_YY	5	AE6	All	All	I/O, VREF Bank 5, L148N_YY	I/O, VREF Bank 5, L148N_YY
I/O, L148P_YY	5	AF6	All	-	I/O, L148P_YY	I/O, L148P_YY
I/O, L147N	5	AA7	XC2S600E	-	-	I/O, L147N_Y
I/O, L147P	5	AB7	XC2S600E	-	I/O	I/O, L147P_Y
I/O, L146N_YY	5	AC7	All	-	I/O, L146N_YY	I/O, L146N_YY
I/O, L146P_YY	5	AD7	All	-	I/O, L146P_YY	I/O, L146P_YY
I/O, L145N_YY	5	AE7	All	-	I/O, L145N_YY	I/O, L145N_YY
I/O, L145P_YY	5	AF7	All	-	I/O, L145P_YY	I/O, L145P_YY
I/O, VREF Bank 5, L144N_YY	5	Y8	All	All	I/O, VREF Bank 5, L144N_YY	I/O, VREF Bank 5, L144N_YY
I/O, L144P_YY	5	AA8	All	-	I/O, L144P_YY	I/O, L144P_YY
I/O, L143N_YY	5	AE8	All	-	I/O, L143N_YY	I/O, L143N_YY
I/O, L143P_YY	5	AF8	All	-	I/O, L143P_YY	I/O, L143P_YY
I/O	5	AB8	-	-	I/O	I/O
I/O, L142N	5	W9	XC2S600E	-	I/O, L142N	I/O, L142N_Y
I/O, L142P	5	Y9	XC2S600E	-	I/O, L142P	I/O, L142P_Y
I/O, L141N	5	AA9	XC2S600E	XC2S600E	-	I/O, VREF Bank 5, L141N_Y
I/O, L141P	5	AB9	XC2S600E	-	I/O	I/O, L141P_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L140N_YY	5	AC9	All	-	I/O, L140N_YY	I/O, L140N_YY
I/O, L140P_YY	5	AD9	All	-	I/O, L140P_YY	I/O, L140P_YY
I/O, L139N_YY	5	AE9	All	-	I/O, L139N_YY	I/O, L139N_YY
I/O, L139P_YY	5	AF9	All	-	I/O, L139P_YY	I/O, L139P_YY
I/O, VREF Bank 5, L138N_YY	5	W10	All	All	I/O, VREF Bank 5, L138N_YY	I/O, VREF Bank 5, L138N_YY
I/O, L138P_YY	5	Y10	All	-	I/O, L138P_YY	I/O, L138P_YY
I/O, L137N_YY	5	AB10	All	-	I/O, L137N_YY	I/O, L137N_YY
I/O, L137P_YY	5	AC10	All	-	I/O, L137P_YY	I/O, L137P_YY
I/O	5	AD10	-	-	-	I/O
I/O, L136N	5	AE10	XC2S600E	-	I/O, L136N	I/O, L136N_Y
I/O, L136P	5	AF10	XC2S600E	-	I/O, L136P	I/O, L136P_Y
I/O	5	AD11	-	-	-	I/O
I/O, L135N_YY	5	W11	All	-	I/O, L135N_YY	I/O, L135N_YY
I/O, L135P_YY	5	Y11	All	-	I/O, L135P_YY	I/O, L135P_YY
I/O, L134N_YY	5	AA11	All	-	I/O, L134N_YY	I/O, L134N_YY
I/O, L134P_YY	5	AB11	All	-	I/O, L134P_YY	I/O, L134P_YY
I/O	5	V12	-	-	-	I/O
I/O, L133N	5	AE11	-	-	I/O, L133N	I/O, L133N
I/O, L133P	5	AF11	-	-	I/O, L133P	I/O, L133P
I/O	5	W12	-	-	-	I/O
I/O, L132N_YY	5	Y12	All	-	I/O, L132N_YY	I/O, L132N_YY
I/O, L132P_YY	5	AA12	All	-	I/O, L132P_YY	I/O, L132P_YY
I/O, VREF Bank 5, L131N_YY	5	AB12	All	All	I/O, VREF Bank 5, L131N_YY	I/O, VREF Bank 5, L131N_YY
I/O, L131P_YY	5	AC12	All	-	I/O, L131P_YY	I/O, L131P_YY
I/O	5	V13	-	-	-	I/O
I/O, L130N_YY	5	AE12	All	-	I/O, L130N_YY	I/O, L130N_YY
I/O, L130P_YY	5	AF12	All	-	I/O, L130P_YY	I/O, L130P_YY
I/O	5	W13	-	-	-	I/O
I/O, L129N	5	Y13	XC2S600E	-	I/O, L129N	I/O, L129N_Y
I/O, L129P	5	AA13	XC2S600E	-	I/O, L129P	I/O, L129P_Y
I/O, VREF Bank 5, L128N	5	AB13	XC2S600E	All	I/O, VREF Bank 5, L128N	I/O, VREF Bank 5, L128N_Y
I/O, L128P	5	AC13	XC2S600E	-	I/O, L128P	I/O, L128P_Y
I/O	5	AD13	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L127N	5	V14	-	-	I/O	I/O, L127N
I/O, L127P	5	W14	-	-	-	I/O, L127P
I/O (DLL), L126N	5	AE13	-	-	I/O (DLL), L126N	I/O (DLL), L126N
GCK1, I	5	AF13	-	-	GCK1, I	GCK1, I
GCK0, I	4	AF14	-	-	GCK0, I	GCK0, I
I/O (DLL), L126P	4	AE14	-	-	I/O (DLL), L126P	I/O (DLL), L126P
I/O	4	AD14	-	-	-	I/O
I/O, L125N	4	AC14	-	-	I/O, L125N	I/O, L125N
I/O, L125P	4	AB14	-	-	I/O, L125P	I/O, L125P
I/O	4	AC15	-	-	-	I/O
I/O, L124N	4	AA14	XC2S600E	-	I/O, L124N	I/O, L124N_Y
I/O, VREF Bank 4, L124P	4	Y14	XC2S600E	All	I/O, VREF Bank 4, L124P	I/O, VREF Bank 4, L124P_Y
I/O, L123N	4	AF15	XC2S600E	-	I/O, L123N	I/O, L123N_Y
I/O, L123P	4	AE15	XC2S600E	-	I/O, L123P	I/O, L123P_Y
I/O	4	AB15	-	-	-	I/O
I/O, L122N_YY	4	AA15	All	-	I/O, L122N_YY	I/O, L122N_YY
I/O, L122P_YY	4	Y15	All	-	I/O, L122P_YY	I/O, L122P_YY
I/O	4	AF16	-	-	-	I/O
I/O, L121N_YY	4	W15	All	-	I/O, L121N_YY	I/O, L121N_YY
I/O, VREF Bank 4, L121P_YY	4	V15	All	All	I/O, VREF Bank 4, L121P_YY	I/O, VREF Bank 4, L121P_YY
I/O, L120N_YY	4	AE16	All	-	I/O, L120N_YY	I/O, L120N_YY
I/O, L120P_YY	4	AD16	All	-	I/O, L120P_YY	I/O, L120P_YY
I/O	4	AB16	-	-	-	I/O
I/O, L119N	4	AA16	-	-	I/O, L119N	I/O, L119N
I/O, L119P	4	Y16	-	-	I/O, L119P	I/O, L119P
I/O	4	W16	-	-	-	I/O
I/O, L118N_YY	4	AF17	All	-	I/O, L118N_YY	I/O, L118N_YY
I/O, L118P_YY	4	AE17	All	-	I/O, L118P_YY	I/O, L118P_YY
I/O, L117N_YY	4	AD17	All	-	I/O, L117N_YY	I/O, L117N_YY
I/O, L117P_YY	4	AC17	All	-	I/O, L117P_YY	I/O, L117P_YY
I/O	4	AB17	-	-	-	I/O
I/O, L116N	4	Y17	XC2S600E	-	I/O, L116N	I/O, L116N_Y

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L116P	4	W17	XC2S600E	-	I/O, L116P	I/O, L116P_Y
I/O	4	AF18	-	-	-	I/O
I/O, L115N_YY	4	AE18	All	-	I/O, L115N_YY	I/O, L115N_YY
I/O, L115P_YY	4	AD18	All	-	I/O, L115P_YY	I/O, L115P_YY
I/O	4	AC18	-	-	I/O	I/O
I/O, VREF Bank 4, L114N	4	AB18	-	All	I/O, VREF Bank 4, L114N	I/O, VREF Bank 4, L114N
I/O, L114P	4	AA18	-	-	I/O, L114P	I/O, L114P
I/O, L113N	4	Y18	-	-	I/O, L113N	I/O, L113N
I/O, L113P	4	W18	-	-	I/O, L113P	I/O, L113P
I/O	4	AB19	-	-	I/O	I/O
I/O, L112N	4	AF19	XC2S600E	-	I/O	I/O, L112N_Y
I/O, L112P	4	AE19	XC2S600E	XC2S600E	-	I/O, VREF Bank 4, L112P_Y
I/O, L111N	4	AA19	XC2S600E	-	I/O, L111N	I/O, L111N_Y
I/O, L111P	4	Y19	XC2S600E	-	I/O, L111P	I/O, L111P_Y
I/O	4	AF20	-	-	-	I/O
I/O, L110N	4	AE20	XC2S600E	-	I/O, L110N	I/O, L110N_Y
I/O, L110P	4	AD20	XC2S600E	-	I/O, L110P	I/O, L110P_Y
I/O	4	AC20	-	-	I/O	I/O
I/O, L109N_YY	4	AB20	All	-	I/O, L109N_YY	I/O, L109N_YY
I/O, VREF Bank 4, L109P_YY	4	AA20	All	All	I/O, VREF Bank 4, L109P_YY	I/O, VREF Bank 4, L109P_YY
I/O	4	Y20	-	-	I/O	I/O
I/O, L108N	4	AF21	-	-	I/O, L108N	I/O, L108N
I/O, L108P	4	AE21	-	-	I/O, L108P	I/O, L108P
I/O, L107N	4	AD21	-	-	I/O, L107N	I/O, L107N
I/O, L107P	4	AC21	-	-	I/O, L107P	I/O, L107P
I/O	4	AC22	-	-	-	I/O
I/O, L106N_YY	4	AF22	All	-	I/O, L106N_YY	I/O, L106N_YY
I/O, VREF Bank 4, L106P_YY	4	AE22	All	All	I/O, VREF Bank 4, L106P_YY	I/O, VREF Bank 4, L106P_YY
I/O, L105N_YY	4	AB21	All	-	I/O, L105N_YY	I/O, L105N_YY
I/O, L105P_YY	4	AA21	All	-	I/O, L105P_YY	I/O, L105P_YY
I/O, L104N_YY	4	AF23	All	-	I/O, L104N_YY	I/O, L104N_YY
I/O, L104P_YY	4	AE23	All	-	I/O, L104P_YY	I/O, L104P_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L103N	4	AD23	XC2S600E	-	I/O	I/O, L103N_Y
I/O, L103P	4	AE24	XC2S600E	-	-	I/O, L103P_Y
I/O, L102N_YY	4	AF24	All	-	I/O, L102N_YY	I/O, L102N_YY
I/O, L102P_YY	4	AF25	All	-	I/O, L102P_YY	I/O, L102P_YY
DONE	3	AE26	-	-	DONE	DONE
$\overline{\text{PROGRAM}}$	-	AC24	-	-	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
I/O ($\overline{\text{INIT}}$), L101N_YY	3	AD25	All	-	I/O ($\overline{\text{INIT}}$), L101N_YY	I/O ($\overline{\text{INIT}}$), L101N_YY
I/O (D7), L101P_YY	3	AD26	All	-	I/O (D7), L101P_YY	I/O (D7), L101P_YY
I/O, L100N	3	AC25	-	-	-	I/O, L100N
I/O, L100P	3	AC26	-	-	-	I/O, L100P
I/O, L99N	3	AB22	XC2S600E	-	-	I/O, L99N_Y
I/O, L99P	3	AB23	XC2S600E	-	I/O	I/O, L99P_Y
I/O, L98N_YY	3	AB25	All	-	I/O, L98N_YY	I/O, L98N_YY
I/O, L98P_YY	3	AB26	All	-	I/O, L98P_YY	I/O, L98P_YY
I/O, L97N	3	AA23	-	-	I/O, L97N_Y	I/O, L97N
I/O, L97P	3	AA24	-	-	I/O, L97P_Y	I/O, L97P
I/O, VREF Bank 3, L96N	3	AA25	XC2S600E	All	I/O, VREF Bank 3, L96N	I/O, VREF Bank 3, L96N_Y
I/O, L96P	3	AA26	XC2S600E	-	I/O, L96P	I/O, L96P_Y
I/O, L95N	3	AA22	XC2S600E	-	-	I/O, L95N_Y
I/O, L95P	3	Y22	XC2S600E	-	I/O	I/O, L95P_Y
I/O, L94N	3	Y23	XC2S400E	-	I/O, L94N_Y	I/O, L94N
I/O, L94P	3	Y24	XC2S400E	-	I/O, L94P_Y	I/O, L94P
I/O, L93N	3	Y25	XC2S600E	-	I/O, L93N	I/O, L93N_Y
I/O, L93P	3	Y26	XC2S600E	-	I/O, L93P	I/O, L93P_Y
I/O, VREF Bank 3, L92N_YY	3	W21	All	All	I/O, VREF Bank 3, L92N_YY	I/O, VREF Bank 3, L92N_YY
I/O, L92P_YY	3	W22	All	-	I/O, L92P_YY	I/O, L92P_YY
I/O	3	Y21	-	-	-	I/O
I/O, L91N_YY	3	W25	All	-	I/O, L91N_YY	I/O, L91N_YY
I/O, L91P_YY	3	W26	All	-	I/O, L91P_YY	I/O, L91P_YY
I/O	3	W20	-	-	I/O	I/O
I/O, L90N	3	V19	XC2S400E	-	I/O, L90N_Y	I/O, L90N
I/O, L90P	3	V20	XC2S400E	-	I/O, L90P_Y	I/O, L90P

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L89N	3	V21	XC2S600E	XC2S600E	-	I/O, VREF Bank 3, L89N_Y
I/O, L89P	3	V22	XC2S600E	-	I/O	I/O, L89P_Y
I/O	3	V23	-	-	I/O	I/O
I/O, L88N_YY	3	V24	All	-	I/O, L88N_YY	I/O, L88N_YY
I/O, L88P_YY	3	V25	All	-	I/O, L88P_YY	I/O, L88P_YY
I/O	3	V26	-	-	I/O	I/O
I/O, VREF Bank 3, L87N_YY	3	U19	All	All	I/O, VREF Bank 3, L87N_YY	I/O, VREF Bank 3, L87N_YY
I/O (D6), L87P_YY	3	U20	All	-	I/O (D6), L87P_YY	I/O (D6), L87P_YY
I/O (D5), L86N_YY	3	U22	All	-	I/O (D5), L86N_YY	I/O (D5), L86N_YY
I/O, L86P_YY	3	U23	All	-	I/O, L86P_YY	I/O, L86P_YY
I/O	3	U24	-	-	-	I/O
I/O, L85N	3	U25	XC2S600E	-	-	I/O, L85N_Y
I/O, L85P	3	U26	XC2S600E	-	I/O	I/O, L85P_Y
I/O	3	R18	-	-	I/O	I/O
I/O, L84N	3	T19	XC2S400E	-	I/O, L84N_Y	I/O, L84N
I/O, L84P	3	T20	XC2S400E	-	I/O, L84P_Y	I/O, L84P
I/O, L83N	3	T21	XC2S600E	-	I/O, L83N	I/O, L83N_Y
I/O, L83P	3	T22	XC2S600E	-	I/O, L83P	I/O, L83P_Y
I/O	3	T24	-	-	-	I/O
I/O, L82N	3	T25	XC2S600E	-	I/O, L82N	I/O, L82N_Y
I/O, L82P	3	T26	XC2S600E	-	I/O, L82P	I/O, L82P_Y
I/O	3	R19	-	-	-	I/O
I/O, L81N	3	R20	XC2S600E	-	I/O, L81N	I/O, L81N_Y
I/O, L81P	3	R21	XC2S600E	-	I/O, L81P	I/O, L81P_Y
I/O, VREF Bank 3, L80N_YY	3	R22	All	All	I/O, VREF Bank 3, L80N_YY	I/O, VREF Bank 3, L80N_YY
I/O (D4), L80P_YY	3	R23	All	-	I/O (D4), L80P_YY	I/O (D4), L80P_YY
I/O	3	P18	-	-	-	I/O
I/O, L79N_YY	3	R25	All	-	I/O, L79N_YY	I/O, L79N_YY
I/O, L79P_YY	3	R26	All	-	I/O, L79P_YY	I/O, L79P_YY
I/O	3	P19	-	-	-	I/O
I/O, L78N	3	P20	XC2S400E	-	I/O, L78N_Y	I/O, L78N
I/O, L78P	3	P21	XC2S400E	-	I/O, L78P_Y	I/O, L78P

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, VREF Bank 3, L77N	3	P22	XC2S600E	All	I/O, VREF Bank 3, L77N	I/O, VREF Bank 3, L77N_Y
I/O, L77P	3	P23	XC2S600E	-	I/O, L77P	I/O, L77P_Y
I/O	3	P24	-	-	-	I/O
I/O, L76N_YY	3	P25	All	-	I/O, L76N_YY	I/O, L76N_YY
I/O, L76P_YY	3	P26	All	-	I/O, L76P_YY	I/O, L76P_YY
I/O	3	N18	-	-	-	I/O
I/O (TRDY)	3	N24	-	-	I/O (TRDY)	I/O (TRDY)
I/O (IRDY), L75N_YY	2	N26	All	-	I/O (IRDY), L75N_YY	I/O (IRDY), L75N_YY
I/O, L75P_YY	2	N25	All	-	I/O, L75P_YY	I/O, L75P_YY
I/O	2	N19	-	-	-	I/O
I/O, L74N	2	N23	XC2S600E	-	-	I/O, L74N_Y
I/O, L74P	2	N22	XC2S600E	-	I/O	I/O, L74P_Y
I/O	2	M23	-	-	I/O	I/O
I/O, L73N	2	N21	XC2S600E	-	I/O, L73N	I/O, L73N_Y
I/O, VREF Bank 2, L73P	2	N20	XC2S600E	All	I/O, VREF Bank 2, L73P	I/O, VREF Bank 2, L73P_Y
I/O, L72N	2	M26	XC2S400E	-	I/O, L72N_Y	I/O, L72N
I/O, L72P	2	M25	XC2S400E	-	I/O, L72P_Y	I/O, L72P
I/O	2	M22	-	-	-	I/O
I/O, L71N_YY	2	M21	All	-	I/O, L71N_YY	I/O, L71N_YY
I/O, L71P_YY	2	M20	All	-	I/O, L71P_YY	I/O, L71P_YY
I/O	2	L26	-	-	-	I/O
I/O (D3), L70N_YY	2	M19	All	-	I/O (D3), L70N_YY	I/O (D3), L70N_YY
I/O, VREF Bank 2, L70P_YY	2	M18	All	All	I/O, VREF Bank 2, L70P_YY	I/O, VREF Bank 2, L70P_YY
I/O, L69N	2	L25	XC2S600E	-	I/O, L69N	I/O, L69N_Y
I/O, L69P	2	L24	XC2S600E	-	I/O, L69P	I/O, L69P_Y
I/O	2	L22	-	-	-	I/O
I/O, L68N	2	L21	XC2S600E	-	I/O, L68N	I/O, L68N_Y
I/O, L68P	2	L20	XC2S600E	-	I/O, L68P	I/O, L68P_Y
I/O	2	L19	-	-	-	I/O
I/O, L67N	2	K26	XC2S600E	-	I/O, L67N	I/O, L67N_Y
I/O, L67P	2	K25	XC2S600E	-	I/O, L67P	I/O, L67P_Y
I/O, L66N	2	K24	-	-	-	I/O, L66N

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L66P	2	K23	-	-	I/O	I/O, L66P
I/O	2	K22	-	-	-	I/O
I/O, L65N	2	K20	XC2S600E	-	I/O	I/O, L65N_Y
I/O, L65P	2	K19	XC2S600E	-	I/O	I/O, L65P_Y
I/O	2	J26	-	-	I/O	I/O
I/O, L64N_YY	2	J25	All	-	I/O, L64N_YY	I/O, L64N_YY
I/O (D2), L64P_YY	2	J24	All	-	I/O (D2), L64P_YY	I/O (D2), L64P_YY
I/O (D1)	2	J23	-	-	I/O (D1)	I/O (D1)
I/O, VREF Bank 2, L63N_YY	2	J22	All	All	I/O, VREF Bank 2, L63N_YY	I/O, VREF Bank 2, L63N_YY
I/O, L63P_YY	2	J21	All	-	I/O, L63P_YY	I/O, L63P_YY
I/O, L62N_YY	2	J20	All	-	I/O, L62N_YY	I/O, L62N_YY
I/O, L62P_YY	2	J19	All	-	I/O, L62P_YY	I/O, L62P_YY
I/O	2	H22	-	-	I/O	I/O
I/O, L61N	2	H26	XC2S600E	-	I/O	I/O, L61N_Y
I/O, L61P	2	H25	XC2S600E	XC2S600E	-	I/O, VREF Bank 2, L61P_Y
I/O, L60N	2	H21	XC2S400E	-	I/O, L60N_Y	I/O, L60N
I/O, L60P	2	H20	XC2S400E	-	I/O, L60P_Y	I/O, L60P
I/O	2	G26	-	-	-	I/O
I/O, L59N_YY	2	G25	All	-	I/O, L59N_YY	I/O, L59N_YY
I/O, L59P_YY	2	G24	All	-	I/O, L59P_YY	I/O, L59P_YY
I/O	2	G23	-	-	I/O	I/O
I/O, L58N_YY	2	G22	All	-	I/O, L58N_YY	I/O, L58N_YY
I/O, VREF Bank 2, L58P_YY	2	G21	All	All	I/O, VREF Bank 2, L58P_YY	I/O, VREF Bank 2, L58P_YY
I/O	2	G20	-	-	I/O	I/O
I/O, L57N_YY	2	F26	All	-	I/O, L57N_YY	I/O, L57N_YY
I/O, L57P_YY	2	F25	All	-	I/O, L57P_YY	I/O, L57P_YY
I/O, L56N	2	F24	XC2S600E	-	I/O, L56N	I/O, L56N_Y
I/O, L56P	2	F23	XC2S600E	-	I/O, L56P	I/O, L56P_Y
I/O	2	F22	-	-	-	I/O
I/O, L55N	2	E26	XC2S600E	-	I/O, L55N	I/O, L55N_Y
I/O, VREF Bank 2, L55P	2	E25	XC2S600E	All	I/O, VREF Bank 2, L55P	I/O, VREF Bank 2, L55P_Y
I/O, L54N	2	E23	XC2S400E	-	I/O, L54N_Y	I/O, L54N

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L54P	2	E22	XC2S400E	-	I/O, L54P_Y	I/O, L54P
I/O, L53N_YY	2	F21	All	-	I/O, L53N_YY	I/O, L53N_YY
I/O, L53P_YY	2	E21	All	-	I/O, L53P_YY	I/O, L53P_YY
I/O, L52N	2	D26	XC2S600E	-	I/O	I/O, L52N_Y
I/O, L52P	2	D25	XC2S600E	-	-	I/O, L52P_Y
I/O, L51N	2	D24	-	-	-	I/O, L51N
I/O, L51P	2	C25	-	-	-	I/O, L51P
I/O (DIN, D0), L50N_YY	2	C26	All	-	I/O (DIN, D0), L50N_YY	I/O (DIN, D0), L50N_YY
I/O (DOUT, BUSY), L50P_YY	2	B26	All	-	I/O (DOUT, BUSY), L50P_YY	I/O (DOUT, BUSY), L50P_YY
CCLK	2	A25	-	-	CCLK	CCLK
TDO	2	C23	-	-	TDO	TDO
TDI	-	D22	-	-	TDI	TDI
I/O ($\overline{CS}$), L49P_YY	1	B24	All	-	I/O ($\overline{CS}$), L49P_YY	I/O ($\overline{CS}$), L49P_YY
I/O ($\overline{WRITE}$), L49N_YY	1	A24	All	-	I/O ($\overline{WRITE}$), L49N_YY	I/O ($\overline{WRITE}$), L49N_YY
I/O, L48P	1	B23	-	-	I/O	I/O, L48P
I/O, L48N	1	A23	-	-	-	I/O, L48N
I/O, L47P	1	B22	XC2S400E	-	I/O, L47P_Y	I/O, L47P
I/O, L47N	1	A22	XC2S400E	-	I/O, L47N_Y	I/O, L47N
I/O, L46P_YY	1	D21	All	-	I/O, L46P_YY	I/O, L46P_YY
I/O, L46N_YY	1	C21	All	-	I/O, L46N_YY	I/O, L46N_YY
I/O, VREF Bank 1, L45P_YY	1	B21	All	All	I/O, VREF Bank 1, L45P_YY	I/O, VREF Bank 1, L45P_YY
I/O, L45N_YY	1	A21	All	-	I/O, L45N_YY	I/O, L45N_YY
I/O, L44P	1	F20	XC2S600E	-	-	I/O, L44P_Y
I/O, L44N	1	E20	XC2S600E	-	I/O	I/O, L44N_Y
I/O, L43P_YY	1	D20	All	-	I/O, L43P_YY	I/O, L43P_YY
I/O, L43N_YY	1	C20	All	-	I/O, L43N_YY	I/O, L43N_YY
I/O, L42P_YY	1	B20	All	-	I/O, L42P_YY	I/O, L42P_YY
I/O, L42N_YY	1	A20	All	-	I/O, L42N_YY	I/O, L42N_YY
I/O, VREF Bank 1, L41P_YY	1	G19	All	All	I/O, VREF Bank 1, L41P_YY	I/O, VREF Bank 1, L41P_YY
I/O, L41N_YY	1	F19	All	-	I/O, L41N_YY	I/O, L41N_YY

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	1	E19	-	-	-	I/O
I/O, L40P_YY	1	B19	All	-	I/O, L40P_YY	I/O, L40P_YY
I/O, L40N_YY	1	A19	All	-	I/O, L40N_YY	I/O, L40N_YY
I/O	1	H18	-	-	I/O	I/O
I/O, L39P	1	G18	XC2S600E	-	I/O, L39P	I/O, L39P_Y
I/O, L39N	1	F18	XC2S600E	-	I/O, L39N	I/O, L39N_Y
I/O, L38P	1	D18	XC2S600E	XC2S600E	-	I/O, VREF Bank 1, L38P_Y
I/O, L38N	1	C18	XC2S600E	-	I/O	I/O, L38N_Y
I/O, L37P_YY	1	B18	All	-	I/O, L37P_YY	I/O, L37P_YY
I/O, L37N_YY	1	A18	All	-	I/O, L37N_YY	I/O, L37N_YY
I/O, L36P_YY	1	H17	All	-	I/O, L36P_YY	I/O, L36P_YY
I/O, L36N_YY	1	G17	All	-	I/O, L36N_YY	I/O, L36N_YY
I/O, VREF Bank 1, L35P_YY	1	E18	All	All	I/O, VREF Bank 1, L35P_YY	I/O, VREF Bank 1, L35P_YY
I/O, L35N_YY	1	E17	All	-	I/O, L35N_YY	I/O, L35N_YY
I/O, L34P_YY	1	D17	All	-	I/O, L34P_YY	I/O, L34P_YY
I/O, L34N_YY	1	C17	All	-	I/O, L34N_YY	I/O, L34N_YY
I/O	1	H16	-	-	-	I/O
I/O, L33P	1	B17	XC2S600E	-	I/O, L33P	I/O, L33P_Y
I/O, L33N	1	A17	XC2S600E	-	I/O, L33N	I/O, L33N_Y
I/O	1	G16	-	-	-	I/O
I/O, L32P_YY	1	F16	All	-	I/O, L32P_YY	I/O, L32P_YY
I/O, L32N_YY	1	E16	All	-	I/O, L32N_YY	I/O, L32N_YY
I/O, L31P_YY	1	C16	All	-	I/O, L31P_YY	I/O, L31P_YY
I/O, L31N_YY	1	B16	All	-	I/O, L31N_YY	I/O, L31N_YY
I/O	1	A16	-	-	-	I/O
I/O, L30P	1	J15	-	-	I/O, L30P	I/O, L30P
I/O, L30N	1	H15	-	-	I/O, L30N	I/O, L30N
I/O	1	G15	-	-	-	I/O
I/O, L29P_YY	1	F15	All	-	I/O, L29P_YY	I/O, L29P_YY
I/O, L29N_YY	1	E15	All	-	I/O, L29N_YY	I/O, L29N_YY
I/O, VREF Bank 1, L28P_YY	1	B15	All	All	I/O, VREF Bank 1, L28P_YY	I/O, VREF Bank 1, L28P_YY
I/O, L28N_YY	1	A15	All	-	I/O, L28N_YY	I/O, L28N_YY
I/O	1	D15	-	-	-	I/O

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L27P_YY	1	J14	All	-	I/O, L27P_YY	I/O, L27P_YY
I/O, L27N_YY	1	H14	All	-	I/O, L27N_YY	I/O, L27N_YY
I/O	1	G14	-	-	-	I/O
I/O, L26P	1	F14	XC2S600E	-	I/O, L26P	I/O, L26P_Y
I/O, L26N	1	E14	XC2S600E	-	I/O, L26N	I/O, L26N_Y
I/O, VREF Bank 1, L25P	1	D14	XC2S600E	All	I/O, VREF Bank 1, L25P	I/O, VREF Bank 1, L25P_Y
I/O, L25N	1	C14	XC2S600E	-	I/O, L25N	I/O, L25N_Y
I/O	1	J13	-	-	-	I/O
I/O, L24P	1	C13	-	-	I/O, L24P	I/O, L24P
I/O, L24N	1	D13	-	-	I/O, L24N	I/O, L24N
I/O	1	H13	-	-	-	I/O
I/O (DLL), L23P	1	B14	-	-	I/O (DLL), L23P	I/O (DLL), L23P
GCK2, I	1	A14	-	-	GCK2, I	GCK2, I
GCK3, I	0	A13	-	-	GCK3, I	GCK3, I
I/O (DLL), L23N	0	B13	-	-	I/O (DLL), L23N	I/O (DLL), L23N
I/O	0	E13	-	-	-	I/O
I/O, L22P_YY	0	F13	All	-	I/O, L22P_YY	I/O, L22P_YY
I/O, L22N_YY	0	G13	All	-	I/O, L22N_YY	I/O, L22N_YY
I/O, L21P	0	A12	XC2S600E	-	-	I/O, L21P_Y
I/O, VREF Bank 0, L21N	0	B12	XC2S600E	All	I/O, VREF Bank 0	I/O, VREF Bank 0, L21N_Y
I/O, L20P	0	D12	XC2S600E	-	I/O, L20P	I/O, L20P_Y
I/O, L20N	0	E12	XC2S600E	-	I/O, L20N	I/O, L20N_Y
I/O	0	F12	-	-	-	I/O
I/O, L19P_YY	0	G12	All	-	I/O, L19P_YY	I/O, L19P_YY
I/O, L19N_YY	0	H12	All	-	I/O, L19N_YY	I/O, L19N_YY
I/O	0	J12	-	-	-	I/O
I/O, L18P_YY	0	A11	All	-	I/O, L18P_YY	I/O, L18P_YY
I/O, VREF Bank 0, L18N_YY	0	B11	All	All	I/O, VREF Bank 0, L18N_YY	I/O, VREF Bank 0, L18N_YY
I/O, L17P_YY	0	E11	All	-	I/O, L17P_YY	I/O, L17P_YY
I/O, L17N_YY	0	F11	All	-	I/O, L17N_YY	I/O, L17N_YY
I/O	0	C11	-	-	-	I/O
I/O, L16P	0	G11	-	-	I/O, L16P	I/O, L16P

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O, L16N	0	H11	-	-	I/O, L16N	I/O, L16N
I/O	0	C10	-	-	-	I/O
I/O, L15P_YY	0	A10	All	-	I/O, L15P_YY	I/O, L15P_YY
I/O, L15N_YY	0	B10	All	-	I/O, L15N_YY	I/O, L15N_YY
I/O, L14P_YY	0	D10	All	-	I/O, L14P_YY	I/O, L14P_YY
I/O, L14N_YY	0	E10	All	-	I/O, L14N_YY	I/O, L14N_YY
I/O	0	G10	-	-	-	I/O
I/O, L13P	0	A9	XC2S600E	-	I/O, L13P	I/O, L13P_Y
I/O, L13N	0	B9	XC2S600E	-	I/O, L13N	I/O, L13N_Y
I/O	0	H10	-	-	-	I/O
I/O, L12P_YY	0	C9	All	-	I/O, L12P_YY	I/O, L12P_YY
I/O, L12N_YY	0	D9	All	-	I/O, L12N_YY	I/O, L12N_YY
I/O	0	E9	-	-	I/O	I/O
I/O, VREF Bank 0, L11P	0	F9	-	All	I/O, VREF Bank 0, L11P	I/O, VREF Bank 0, L11P
I/O, L11N	0	G9	-	-	I/O, L11N	I/O, L11N
I/O, L10P	0	A8	-	-	I/O, L10P	I/O, L10P
I/O, L10N	0	B8	-	-	I/O, L10N	I/O, L10N
I/O	0	H9	-	-	I/O	I/O
I/O, L9P	0	E8	XC2S600E	-	I/O	I/O, L9P_Y
I/O, L9N	0	F8	XC2S600E	XC2S600E	-	I/O, VREF Bank 0, L9N_Y
I/O, L8P	0	A7	XC2S600E	-	I/O, L8P	I/O, L8P_Y
I/O, L8N	0	B7	XC2S600E	-	I/O, L8N	I/O, L8N_Y
I/O	0	G8	-	-	I/O	I/O
I/O, L7P_YY	0	C7	All	-	I/O, L7P_YY	I/O, L7P_YY
I/O, L7N_YY	0	D7	All	-	I/O, L7N_YY	I/O, L7N_YY
I/O	0	E7	-	-	-	I/O
I/O, L6P_YY	0	F7	All	-	I/O, L6P_YY	I/O, L6P_YY
I/O, VREF Bank 0, L6N_YY	0	G7	All	All	I/O, VREF Bank 0, L6N_YY	I/O, VREF Bank 0, L6N_YY
I/O	0	A6	-	-	I/O	I/O
I/O, L5P	0	B6	-	-	I/O, L5P	I/O, L5P
I/O, L5N	0	C6	-	-	I/O, L5N	I/O, L5N
I/O, L4P	0	D6	-	-	I/O, L4P	I/O, L4P
I/O, L4N	0	E6	-	-	I/O, L4N	I/O, L4N

FG676 Pinouts (XC2S400E, XC2S600E) *(Continued)*

Pad Name		Pin	LVDS Async. Output Option	VREF Option	Device-Specific Pinouts	
Function	Bank				XC2S400E	XC2S600E
I/O	0	F6	-	-	-	I/O
I/O, L3P_YY	0	A5	All	-	I/O, L3P_YY	I/O, L3P_YY
I/O, VREF Bank 0, L3N_YY	0	B5	All	All	I/O, VREF Bank 0, L3N_YY	I/O, VREF Bank 0, L3N_YY
I/O, L2P_YY	0	D5	All	-	I/O, L2P_YY	I/O, L2P_YY
I/O, L2N_YY	0	E5	All	-	I/O, L2N_YY	I/O, L2N_YY
I/O, L1P_YY	0	B4	All	-	I/O, L1P_YY	I/O, L1P_YY
I/O, L1N_YY	0	C4	All	-	I/O, L1N_YY	I/O, L1N_YY
I/O, L0P	0	A3	XC2S600E	-	I/O	I/O, L0P_Y
I/O, L0N	0	B3	XC2S600E	-	-	I/O, L0N_Y
I/O	0	A4	-	-	I/O	I/O
TCK	-	A2	-	-	TCK	TCK

FG676 Differential Clock Pins

Clock	Bank	P Input		N Input	
		Pin	Name	Pin	Name
GCK0	4	AF14	GCK0, I	AE14	I/O (DLL), L126P
GCK1	5	AF13	GCK1, I	AE13	I/O (DLL), L126N
GCK2	1	A14	GCK2, I	B14	I/O (DLL), L23P
GCK3	0	A13	GCK3, I	B13	I/O (DLL), L23N

Additional FG676 Package Pins

VCCINT Pins						
H8	H19	J9	J18	K10	K11	K16
K17	L10	L17	T10	T17	U10	U11
U16	U17	V9	V18	W8	W19	-
VCCO Bank 0 Pins						
C5	C8	D11	J10	J11	K12	K13
VCCO Bank 1 Pins						
C19	C22	D16	J16	J17	K14	K15
VCCO Bank 2 Pins						
E24	H24	K18	L18	L23	M17	N17
VCCO Bank 3 Pins						
P17	R17	T18	T23	U18	W24	AB24
VCCO Bank 4 Pins						
U14	U15	V16	V17	AC16	AD19	AD22

Additional FG676 Package Pins *(Continued)*

VCCO Bank 5 Pins						
U12	U13	V10	V11	AC11	AD5	AD8
VCCO Bank 6 Pins						
P10	R10	T4	T9	U9	W3	AB3
VCCO Bank 7 Pins						
H3	K9	L4	L9	M10	N10	E3
GND Pins						
A1	A26	B2	B25	C3	C12	C15
C24	D4	D8	D19	D23	F10	F17
H4	H23	K6	K21	L11	L12	L13
L14	L15	L16	M3	M11	M12	M13
M14	M15	M16	M24	N11	N12	N13
N14	N15	N16	P11	P12	P13	P14
P15	P16	R3	R11	R12	R13	R14
R15	R16	R24	T11	T12	T13	T14
T15	T16	U6	U21	W4	W23	AA10
AA17	AC4	AC8	AC19	AC23	AD3	AD12
AD15	AD24	AE2	AE25	AF1	AF26	-
Not Connected Pins (XC2S400E Only)						
A12	A16	A23	B3	C1	C2	C10
C11	C25	D2	D15	D18	D24	D25
E7	E13	E19	F2	F6	F8	F12
F20	F22	G10	G14	G15	G16	G26
H10	H13	H16	H25	J6	J8	J12
J13	K1	K4	K22	K24	L3	L19
L22	L26	M4	M9	M22	N1	N4
N9	N18	N19	N23	P4	P5	P18
P19	P24	R4	R7	R19	T3	T24
U1	U4	U7	U24	U25	V8	V12
V13	V21	W12	W13	W14	W16	Y3
Y7	Y21	AA7	AA9	AA22	AB15	AB16
AB17	AB22	AC1	AC15	AC22	AC25	AC26
AD1	AD2	AD10	AD11	AD13	AD14	AE5
AE19	AE24	AF4	AF16	AF18	AF20	-

Revision History

Version No.	Date	Description
1.0	11/15/01	Initial Xilinx release.
1.1	12/20/01	Corrected differential pin pair designations.
2.0	11/18/02	Added XC2S400E and XC2S600E and FG676. Removed L37 designation from FT256 pinouts. Minor corrections and clarifications to pinout definitions. Removed Preliminary designation.
2.1	02/14/03	Added differential pairs table on page 3, fixed 3 P/N designation typos introduced in v2.0. Clarified that XC2S50E has two VREF pins per bank.

The Spartan-IIE Family Data Sheet

DS001-1, ***Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS001-2, ***Spartan-IIE 1.8V FPGA Family: Functional Description*** (Module 2)

DS001-3, ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS001-4, ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** (Module 4)