Problem Solutions to Problems Marked With a * in

Logic Computer Design Fundamentals, Ed. 2

C H A P T E R 1 2

12-1.

	Binary	a	b	c
54	0010 1 01 00	M	M	M
58	0010 1 10 00	M	M	M
104	1000 0 01 00	M	M	M
5C	0010 1 11 00	M	M	M
108	1000 0 10 00	M	M	M
60	0011 0 00 00	M	M	M
F0	0111 1 00 00	M	M	M
64	0011 0 01 00	M	M	M
54	0010 1 01 00	H	H	M
58	0010 1 10 00	H	H	H
10C	1000 0 11 00	M	M	M
5C	0010 1 11 00	H	H	H
110	1000 1 00 00	M	M	M
60	0011 0 00 00	H	H	M
F0	0111 1 00 00	M	H	M
64	0011 0 01 00	H	H	H

12-4.

Since the lines are 32 bytes, 5 bits are used to address bytes in the lines.

Since there are 512K bytes, there are 512 K/32 = 2^{14} cache lines.

a) Index = 14 Bits,

b) Tag = 32 – 5 – 14 = 13 Bits

c) $(13 + 1) \times 16{,}384 + 512 \times 1024 \times 8 = 4320$ K bits = 540 K bytes

12-6.

a) See page 631 of text.

b) See page 628 of text.

12-8.

000000 00 00 (i0)	000001 00 00 (i4)	000001 10 00 (i6)	000010 10 00 (i10)
000000 01 00 (i1)	000011 00 00 (d)	00001 11 00 (i7)	000011 10 00 (d)
000000 10 00 (i2)	000001 01 00 (i5)	000010 00 00 (i8)	000010 11 00 (i11)
000000 11 00 (i3)	000011 01 00 (d)	000010 01 00 (i9)	000011 11 00 (d)

Addresses of instructions (i) and Data (d) in sequence down and then to the right with the instructions in a loop with instruction i0 following i11. For the split cache, the hit - miss pattern for instructions is (assuming the cache initially empty and LRU replacement) M, M, M, M, M, M, M, M, M, M, M, M, M, ... since there are only eight locations available for instructions. For the unified cache, the hit-miss pattern for instructions with the same assumptions is M, M, M, M, M, M, M, M, M, M, M, M, H, H, H, ... since there are 12 locations indexed appropriately for instructions and four indexed appropriately for data.

12-11.

a) Effective Access Time = 0.91 * 8ns + 0.09 * 85 ns
= 14.93 ns

b) Effective Access Time = 0.82 * 8ns + 0.18* 85 ns
= 21.86 ns

c) Effective Access Time = 0.96 * 8ns + 0.04 * 85 ns
= 11.08 ns

12-14.

a) Each page table handles 512 pages assuming 64-bit words. There are 4395 pages which is more than 4.0 K and less than 4.5 K, so 10 page tables are required including 1 directory page.

b) 9 directory entries are required.

c) 4395 - 8*512 = 299 entries in the last page table.

12-18.

In section 12-3, it is mentioned that write-through in caches can slow down processing, but this can be avoided by using write buffering. When virtual memory does a write to the secondary device, the amount of data being written is typically very large and the device very slow. These two factors generally make it impossible to do write-through with virtual memory. Either the slow down is prohibitively large, or the buffering cost is just too high.