Problem Solutions to Problems Marked With a * in

Logic Computer Design Fundamentals, Ed. 2

C H A P T E R 1 1

11-1.

Heads x (cylinders/Head) x (sectors/cylinder) x (1 cylinder/track) x (bytes/sector)

a) 5 x 733 x 17 x 512   =   31,152.5 Kbytes (K = 1024)

b) 15 x 900 x 17 x 512   =   114,750 Kbytes

c) 7 x 1023 x 64 x 512   =   229,152 Kbytes

11-4.

a) If each address line is used for a different CS input, there will be no way to address
    the four registers. So only 10 lines can be used for CS inputs permitting at most 10 I/O
    Interface Units to be supported.

b) Since two bits must be used to address the four registers, there are 10 bits remaining and
 2^{10} or 1024 distinct I/O Interface Units can be supported.

11-6.

A given address can be shared by two registers if one is written and one is read. If a register is both
read and written, then it needs its own address. Each RW operation requires its own address. Since
there are more read only addresses than write only addresses, the write only addresses can be shared
with read addresses. Since there are twice as many read only registers as there are RW registers, the
number of RW registers is $256/3 = 85$. The number of read only registers is $2 \times 85 = 170$, and the
number of write only registers is 85. This gives a total of 340 registers. (Due to integer numbers of
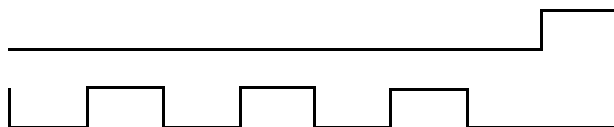registers with the % distributions, there is one address left over.)

11-8.

a)
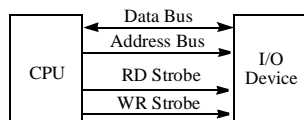
b)
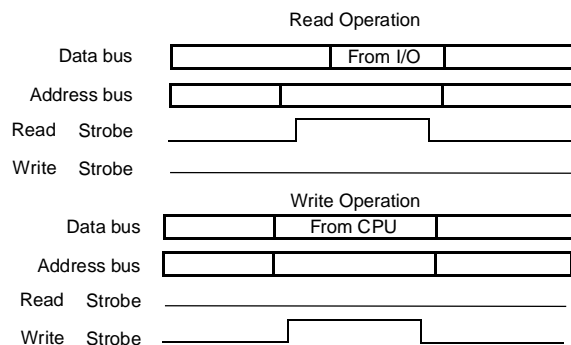
11-10.

a) 28,800 Baud/ 11 Bits   = 2618 Characters/sec

b) 28,800 Baud/ 10 Bits   = 2880 Characters/sec

c) 57,600 Baud/ 11 Bits   = 5636 Characters/sec

d) 115,200 Baud/ 10 Bits = 11,520 Characters/sec

11-13.

There are 7 edges in the NRZI waveform for the SYNC pattern that can be used for synchroniztion.

11-15.

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 1110010	Endpoint Address 4 bits	CRC	EOP

(a) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data 00010010 10010110	CRC	EOP

(b) Data packet (Data0 type) (bits LSB first)

SYNC 8 bits	Type 4 bits 0111	Check 4 bits 1000	EOP

(c) Handshake packet (Acknowledge type)

11-18.

Description	Device 0				Device 1				Device 2			
	PI	PO	RF	VAD	PI	PO	RF	VAD	PI	PO	RF	VAD
Initially	0	0	0	-	0	0	0	-	0	0	1	-
Before CPU acknowledges Device 2	0	0	1	-	0	0	0	-	0	0	1	-
After CPU sends acknowledge	1	0	1	0	0	0	0	-	0	0	1	-

11-20.

Replace the 6 leading 0's in Figure 11-17 wiht 101000.

11-22.

This is Figure 11-17 with the Interrupt and Mask Registers increased to 8 bits each, and the 4x2 Priority Encoder replaced by a 8x3 Priority Encoder. Additionally, VAD must accept a 3rd bit from the Priority Encoder.

11-24.

When the CPU communicates with DMA, the read and write lines are used as inputs. When the DMA communicates with the Memory these lines are used as outputs from the DMA.