Problem Solutions to Problems Marked With a * in

Logic Computer Design Fundamentals, Ed. 2

C H A P T E R 1 0

10-1.

a) $PSR \leftarrow M[SP], SP \leftarrow SP + 1$
$PC \leftarrow M[SP], SP \leftarrow SP + 1$

b) $R6 \leftarrow 0F0F_{16}$

c) $R2 \leftarrow M[255 + R3], M[255 + R3] \leftarrow R2$

d) $M[SP] \leftarrow PC + 2, SP \leftarrow SP–1, PC \leftarrow M[PC + 2 + 00F0_{16}]$

PC and *SP* are the value at the time of the instruction fetch.

10-4.

Register: R3, Register Indirect: 3, Immediate: 2002_{10}, Direct: 1000_{10},
Indexed: 1003_{10}, Indexed Indirect: 1003_{10}, Relative: 3003_{10}, Relative Indirect: 3003_{10}

10-10.

	Sym	RT	MC	MM/ LS	MR/ PS	DSA/ MS	SB	MA	MB	MD	FS/ NA	MO
a)	SHRA0	$R9 \leftarrow SD$	0	0	0	09	0D	0	0	0	10	0
	1	$R9 \leftarrow R9$ (Set MSTS)	0	0	0	09	0	0	0	0	00	F
	2	z: $CAR \leftarrow$ SHRA6	3	0	0	6	00	0	0	0	SHRA6	0
	3	$DD \leftarrow DD(15)\|\|DD(15{:}1)$	0	0	0	0F	0F	0	0	0	15	0
	4	$R9 \leftarrow R9 - 1$	0	0	0	09	00	0	0	0	06	F
	5	z : $CAR \leftarrow SHRA3$	3	0	1	6	00	0	0	0	SHRA3	0
	6	$DD \leftarrow DD, CAR \leftarrow WB0(ROM)$	2	1	4	0F	00	0	0	0	00	D
b)	RLC0	$R9 \leftarrow SD$	0	0	0	09	0D	0	0	0	10	0
	1	$R9 \leftarrow R9$ (Set MSTS)	0	0	0	09	0	0	0	0	00	F
	2	z: $CAR \leftarrow$ RLC6	3	0	0	6	00	0	0	0	RLC6	0
	3	$DD \leftarrow DD(14{:}0)\|\|C, C \leftarrow DD(15)$	0	0	0	0F	0F	0	0	0	1B	D
	4	$R9 \leftarrow R9 - 1$	0	0	0	09	00	0	0	0	06	F
	5	$\bar{z}$: $CAR \leftarrow RLC2$	3	0	1	6	00	0	0	0	RLC2	0
	6	$DD \leftarrow DD, CAR \leftarrow WB0(ROM)$	2	1	4	0F	00	0	0	0	00	D
c)	BV0	V: $CAR \leftarrow BRA$	3	0	0	4	00	0	0	0	BRA	0
	1	$CAR \leftarrow$ INT0(ROM)	2	1	5	00	00	0	0	0	00	0

10-12.

Sym	RT	MC	MM /LS	MR /PS	DSA /MS	SB	MA	MB	MD	FS /NA	MO
MUL0	$R9 \leftarrow 16$	0	0	0	09	10	0	2	0	10	0
1	$R10 \leftarrow DD$	0	0	0	0A	0F	0	0	0	10	0
2	$DD \leftarrow R0$	0	0	0	0F	00	0	0	0	10	0
3	$SD \leftarrow rorc(SD)$	0	0	0	0D	0D	0	0	0	17	D
4	$\bar{C}$: $CAR \leftarrow$ MUL6	3	0	1	3	00	0	0	0	MUL6	0
5	$DD \leftarrow DD + R10$	0	0	0	0F	0A	0	0	0	02	D
6	$DD \leftarrow rorc(DD)$	0	0	0	0F	0F	0	0	0	17	D
7	$R9 \leftarrow R9 - 1$	0	0	0	09	00	0	0	0	06	F
8	z: $CAR \leftarrow MWB0$	3	0	0	6	00	0	0	0	MWB0	0
9	$CAR \leftarrow$ MUL3	3	0	0	0	00	0	0	0	MUL3	0

MWB0 is the write back routine for the Multiply Operation.

10-17.

Cycle 1: PC = 10F

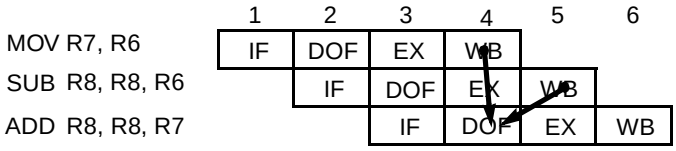
Cycle 2: PC_{-1} = 110, IR = 4418 $2F01_{16}$

Cycle 3: PC_{-2} = 110, RW = 1, DA = 01, MD = 0, BS = 0, PS = X, MW = 0, FS = 02, SH = 01, MA = 0, MB = 1
BUS A = 0000 001F, BUS B = 0000 2F01

Cycle 4: RW = 1, DA = 01, MD = 0, D0 = 0000 2F20, D1 = XXXX XXXX, D2 = 0000 00000

Cycle 5: R1 = 0000 2F20

10-21.



10-23.

a)
```
MOV R7, R6
SUB R8, R8, R6
NOP
ADD R8, R8, R7
```

b)
```
SUB R7, R7, R6
NOP
BNZ R7, 000F
NOP
NOP
AND R8, R7
OR  R5, R7
```

10-28.

a)
```
LD   R1, INDEX
LD   R2, ADDRESS
ADD  R3, R2, R1
LD   R4, R3
SBI  R4, R4, 1
ST   R3, R4
```
Time = 10 RISC Clock Cycles

b) IF = 2 CISC Clock Cycles
1OF = 4 CISC Clock Cycles
EX = 1 CISC Clock Cycles
WB = 2 CISC Clock Cycles
INT = 1 CISC Clock Cycles

Time = 10 CISC Clock Cycles

Time = 30 RISC Clock Cycles