

Fig. 11-1 Keyboard Scan Matrix

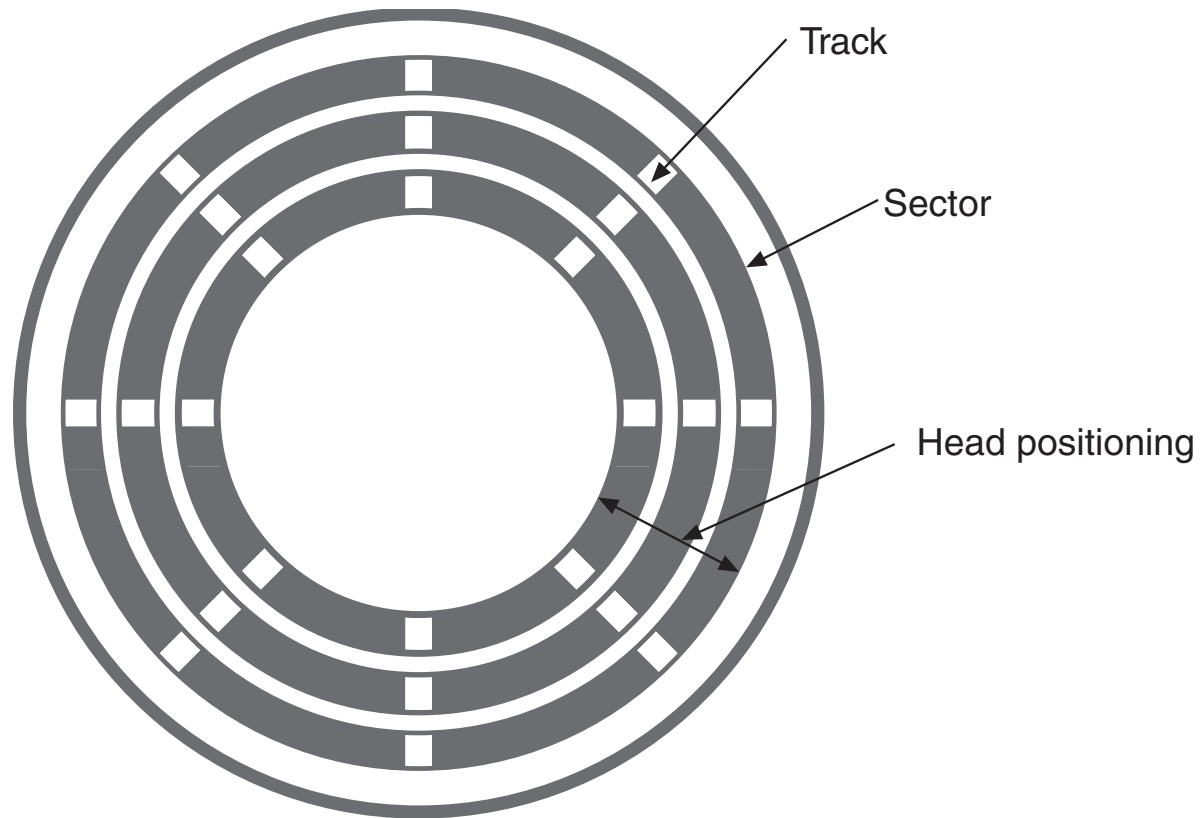


Fig. 11-2 Hard Disk Format

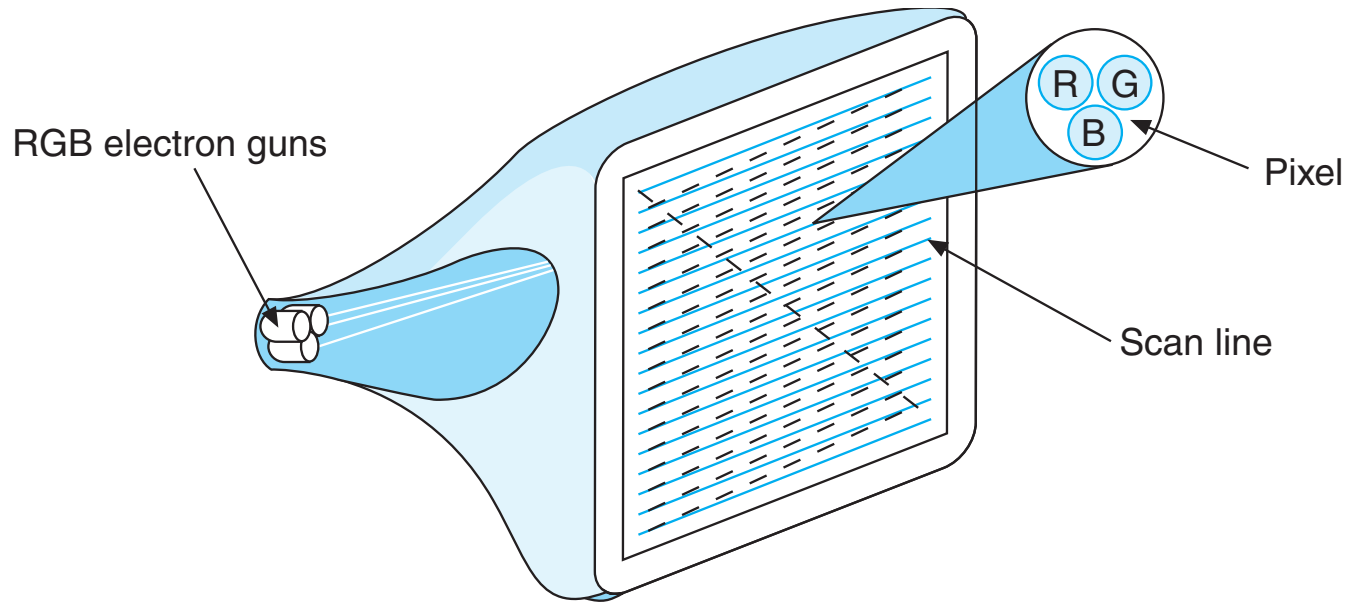


Fig. 11-3 CRT Display

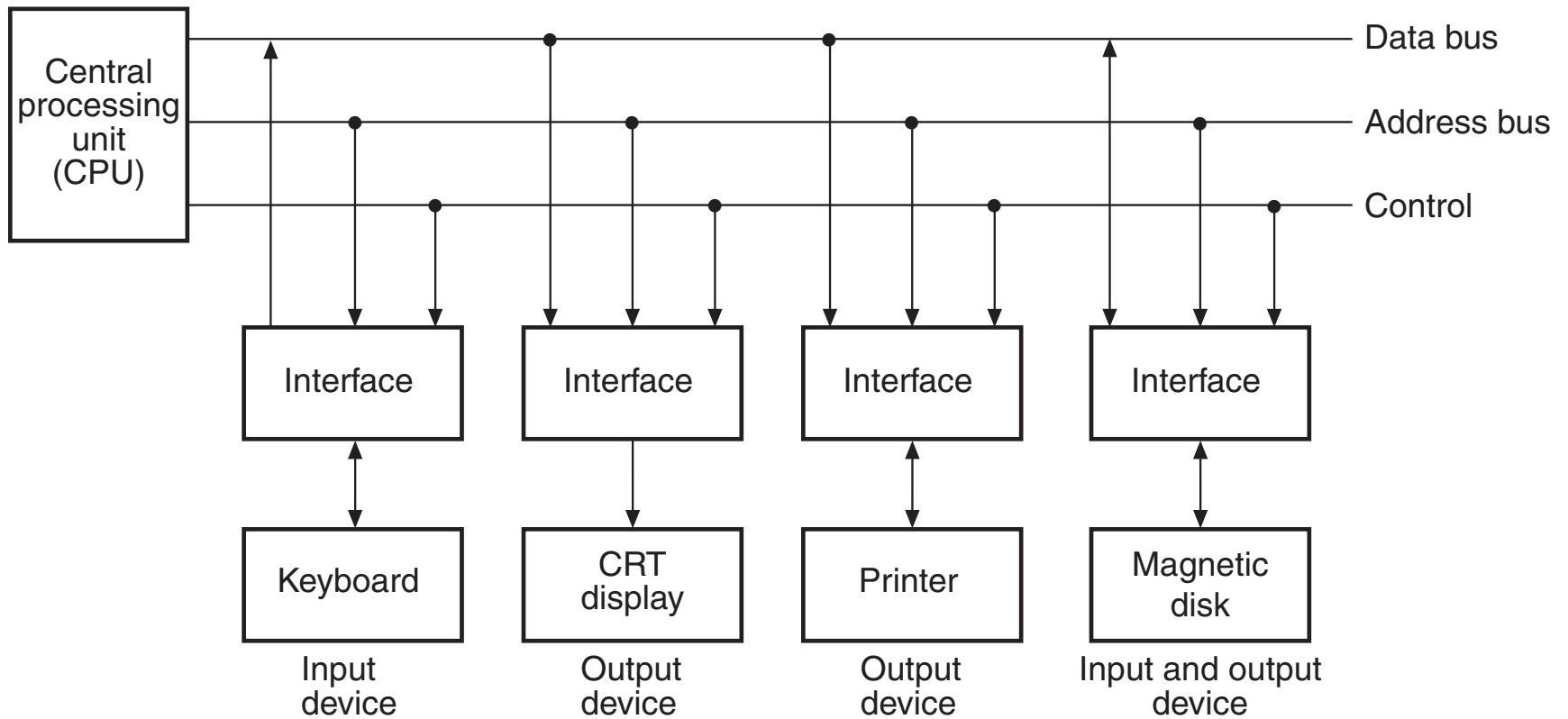
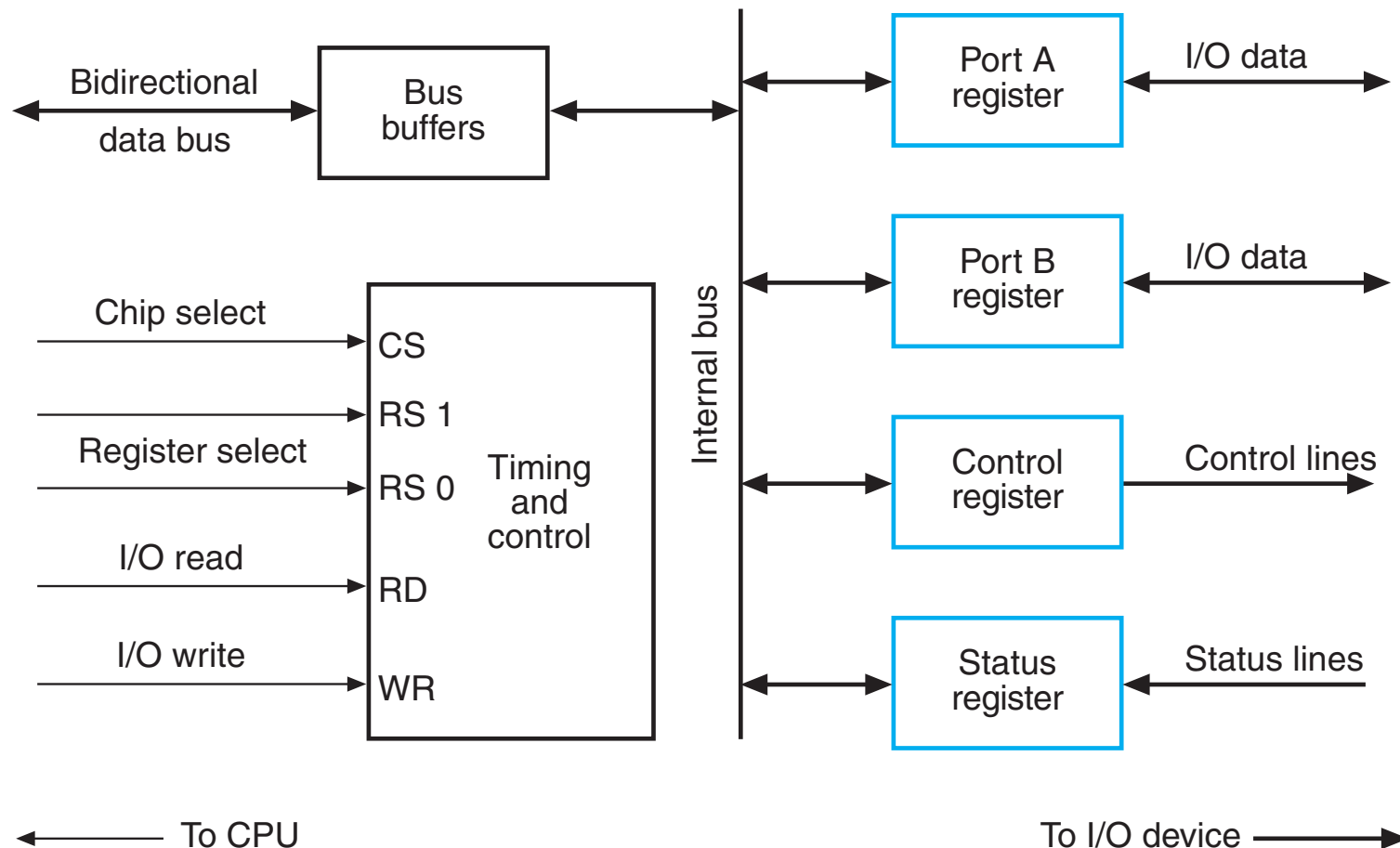


Fig. 11-4 Connection of I/O Devices to CPU



CS	RS1	RS0	Register selected
0	x	x	None: data bus in high-impedance state
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register

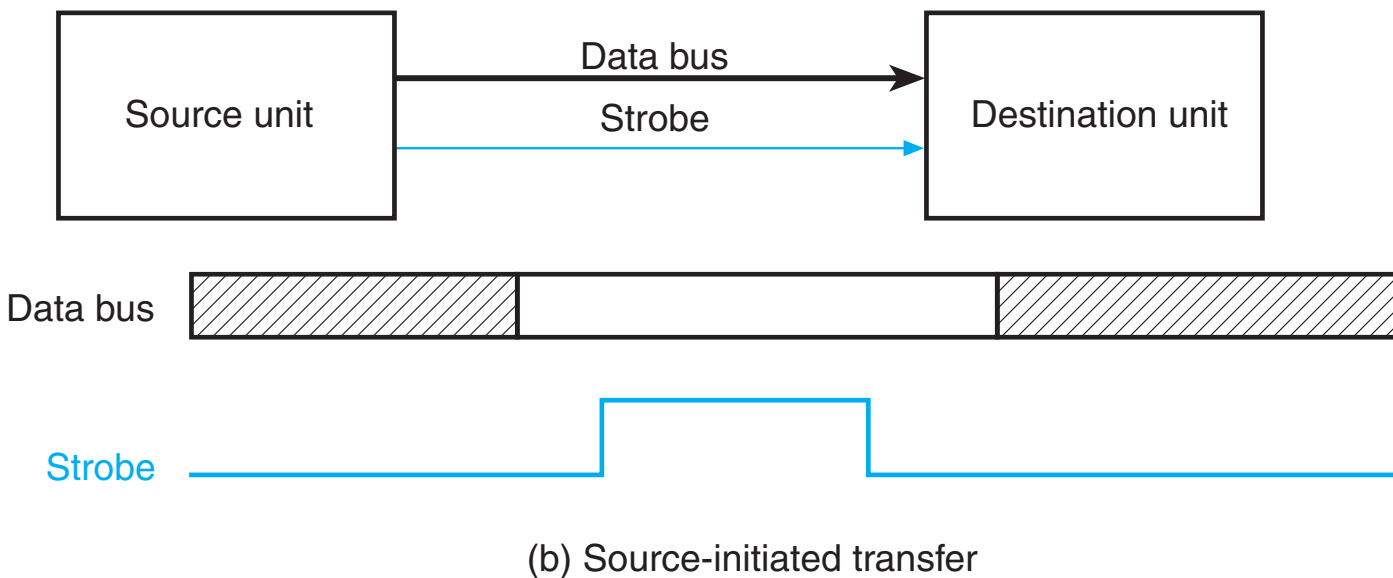
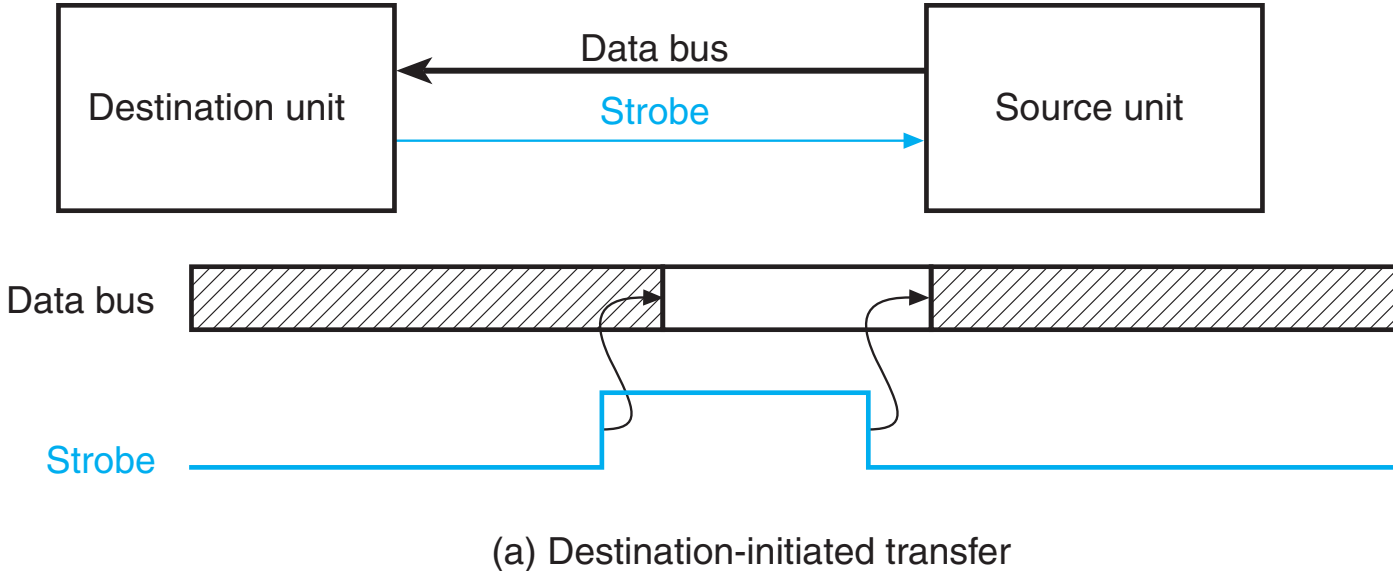
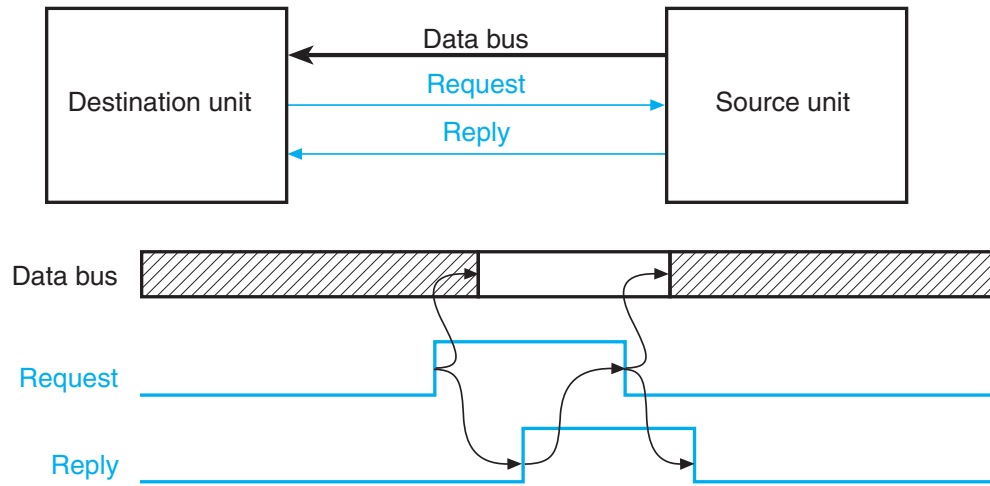
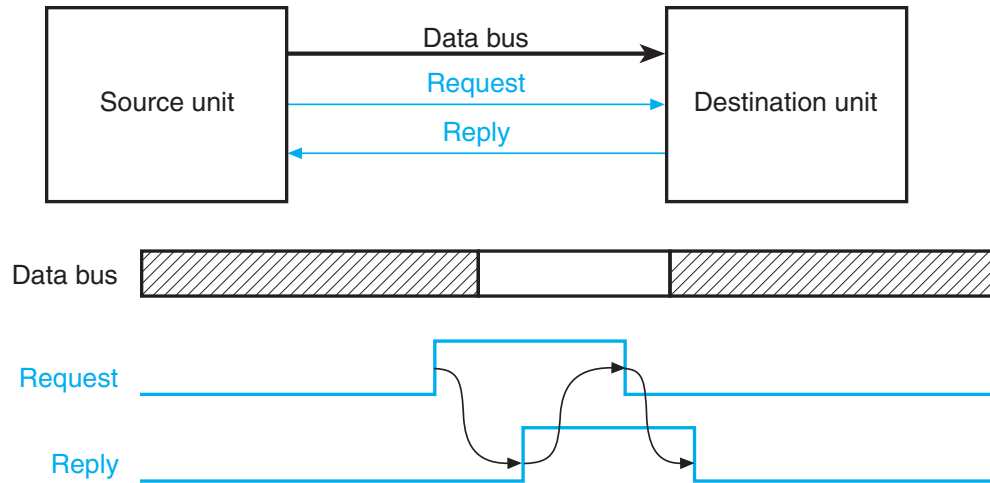


Fig. 11-6 Asynchronous Transfer Using Strobing



(a) Destination-initiated transfer



(b) Source-initiated transfer

Fig. 11-7 Asynchronous Transfer Using Handshaking

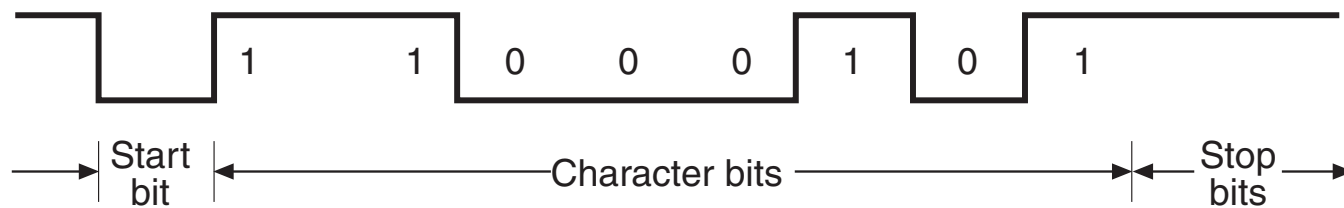


Fig. 11-8 Format of Asynchronous Serial Transfer of Data

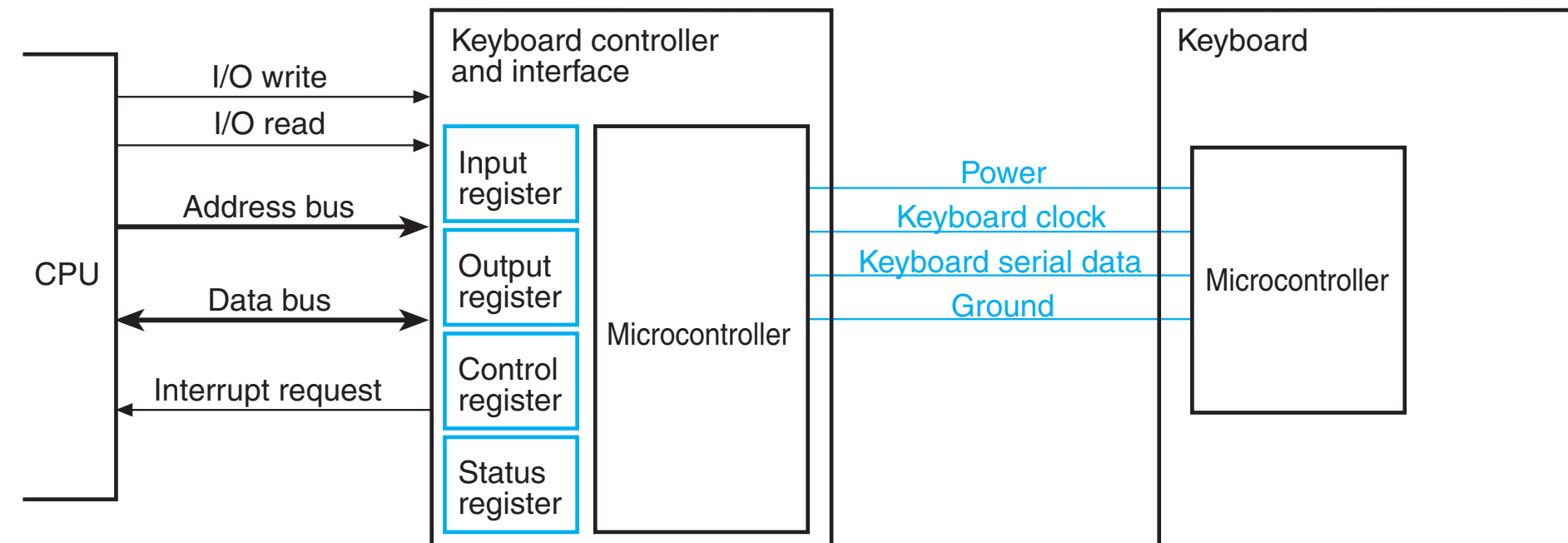


Fig. 11-9 Keyboard Controller and Interface

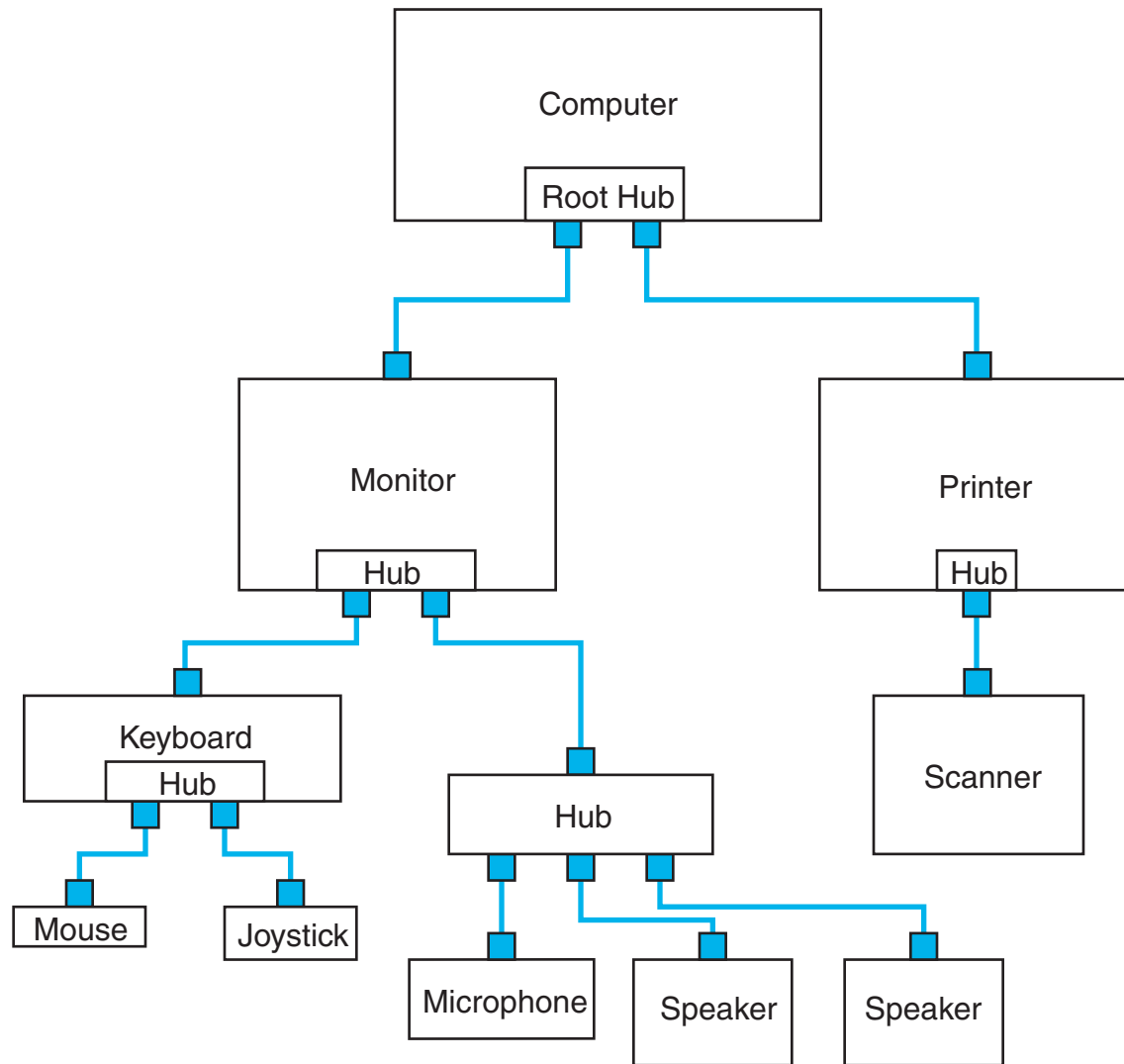


Fig. 11-10 I/O Device Connection Using the Universal Serial Bus (USB)

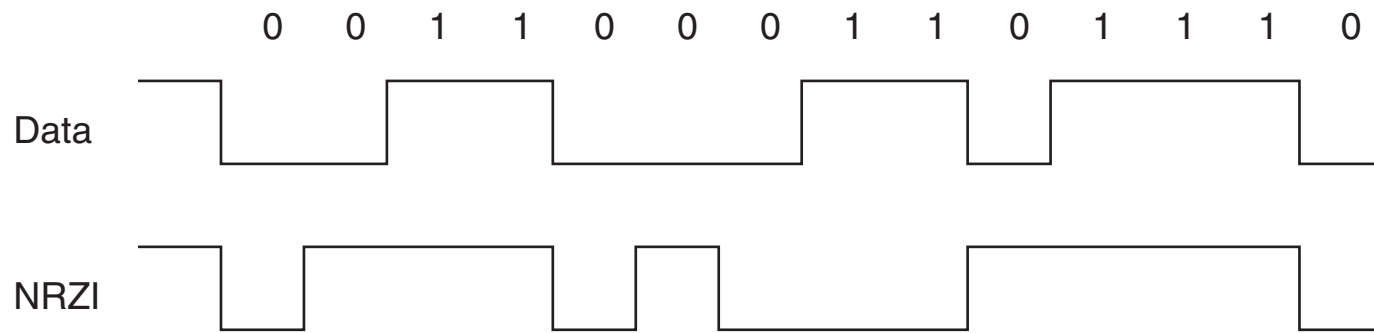


Fig. 11-11 Non-Return to Zero Inverted Data Representation

SYNC	PID	Packet Specific Data	CRC	EOP
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(a) General packet format

SYNC 8 bits	Type 4 bits 1001	Check 4 bits 0110	Device Address 7 bits	Endpoint Address 4 bits	CRC	EOP
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(b) Output packet

SYNC 8 bits	Type 4 bits 1100	Check 4 bits 0011	Data (Up to 1024 bytes)	CRC	EOP
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(c) Data packet (Data0 type)

SYNC 8 bits	Type 4 bits 0100	Check 4 bits 1011	EOP
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(d) Handshake packet (Acknowledge type)

Fig.11-12 USB Packet Formats

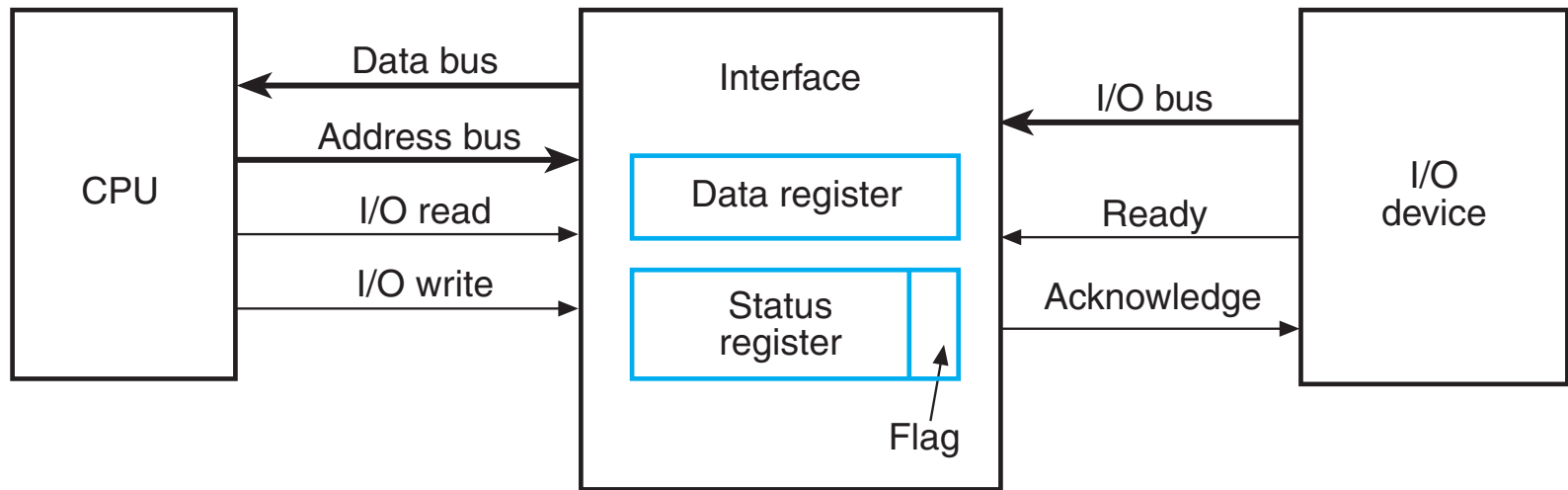


Fig. 11-13 Data Transfer from I/O Device to CPU

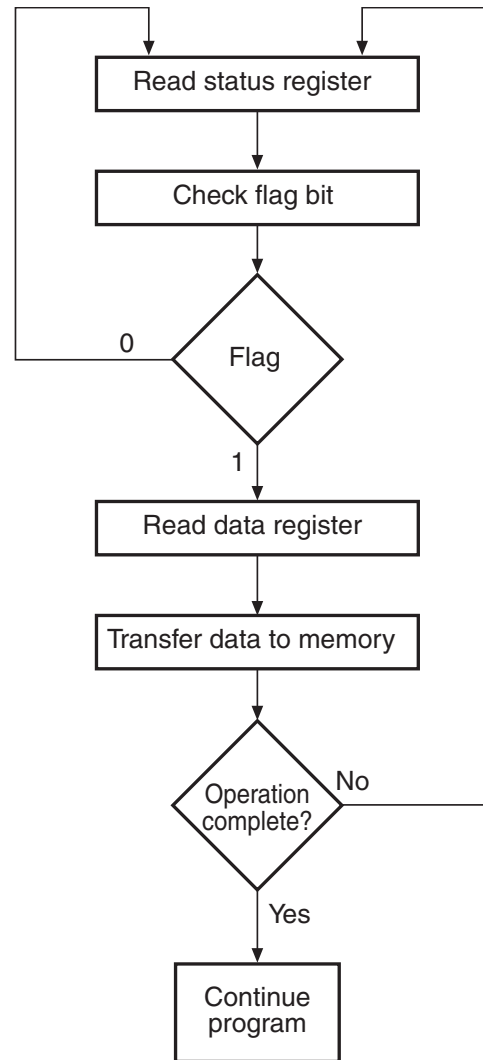


Fig. 11-14 Flowchart for CPU Program to Input Data

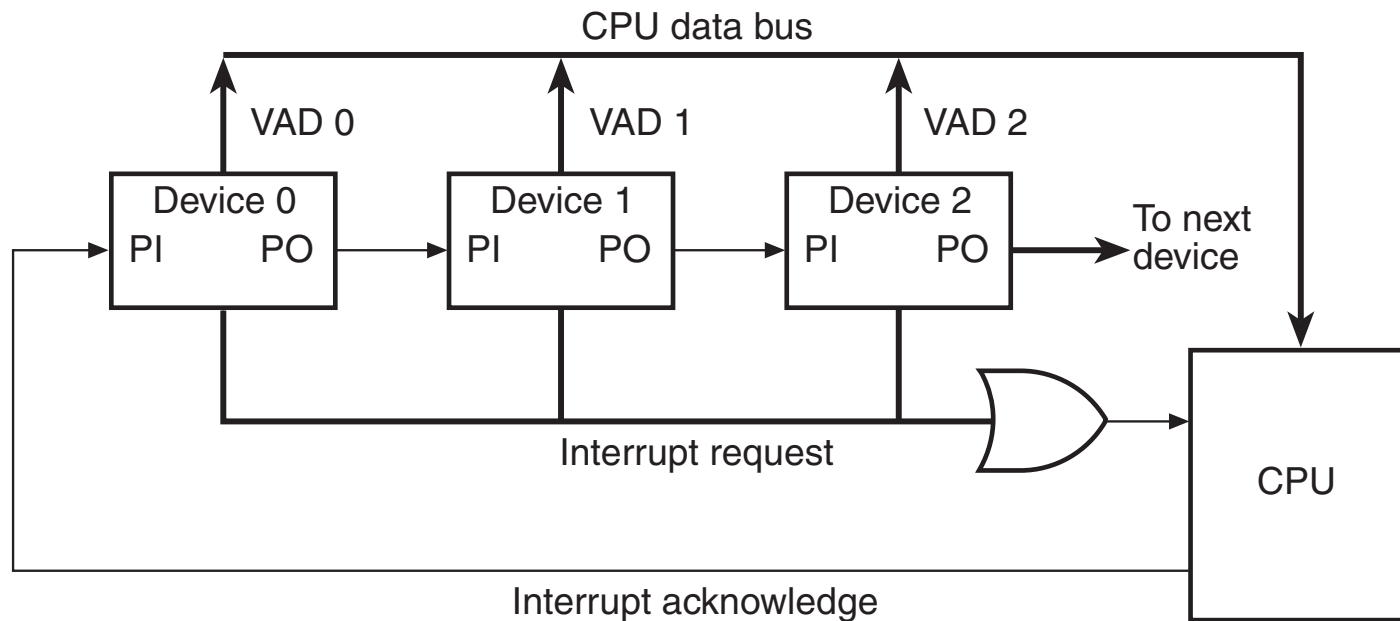


Fig. 11-15 Daisy Chain Priority Interrupt

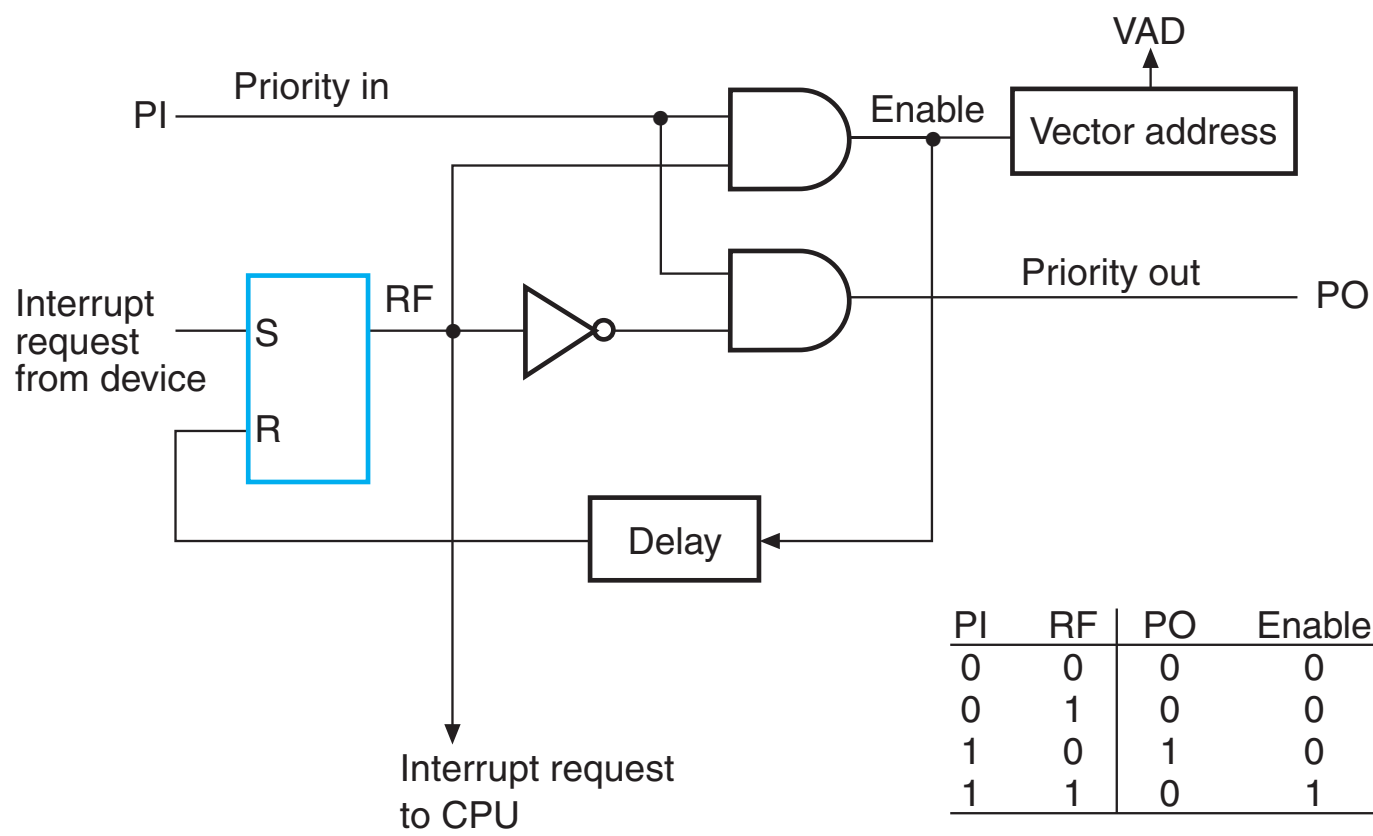


Fig. 11-16 One Stage of the Daisy Chain Priority Arrangement

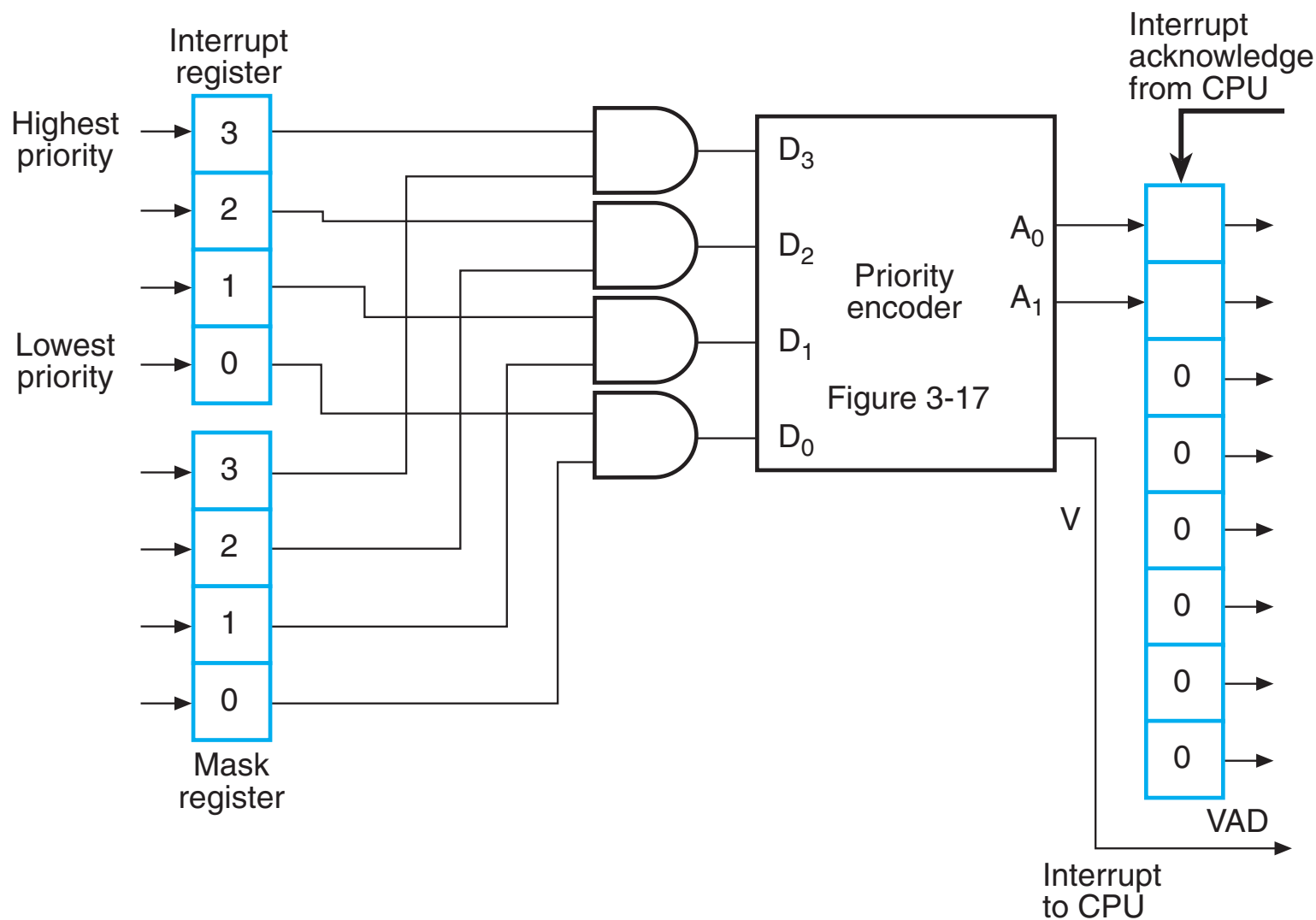


Fig. 11-17 Parallel Priority Interrupt Hardware

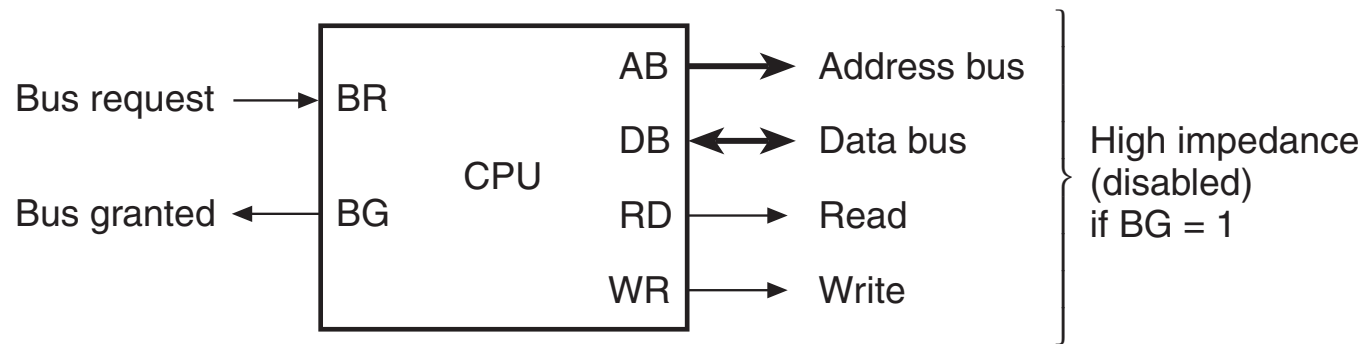


Fig. 11-18 CPU Bus Control Signals

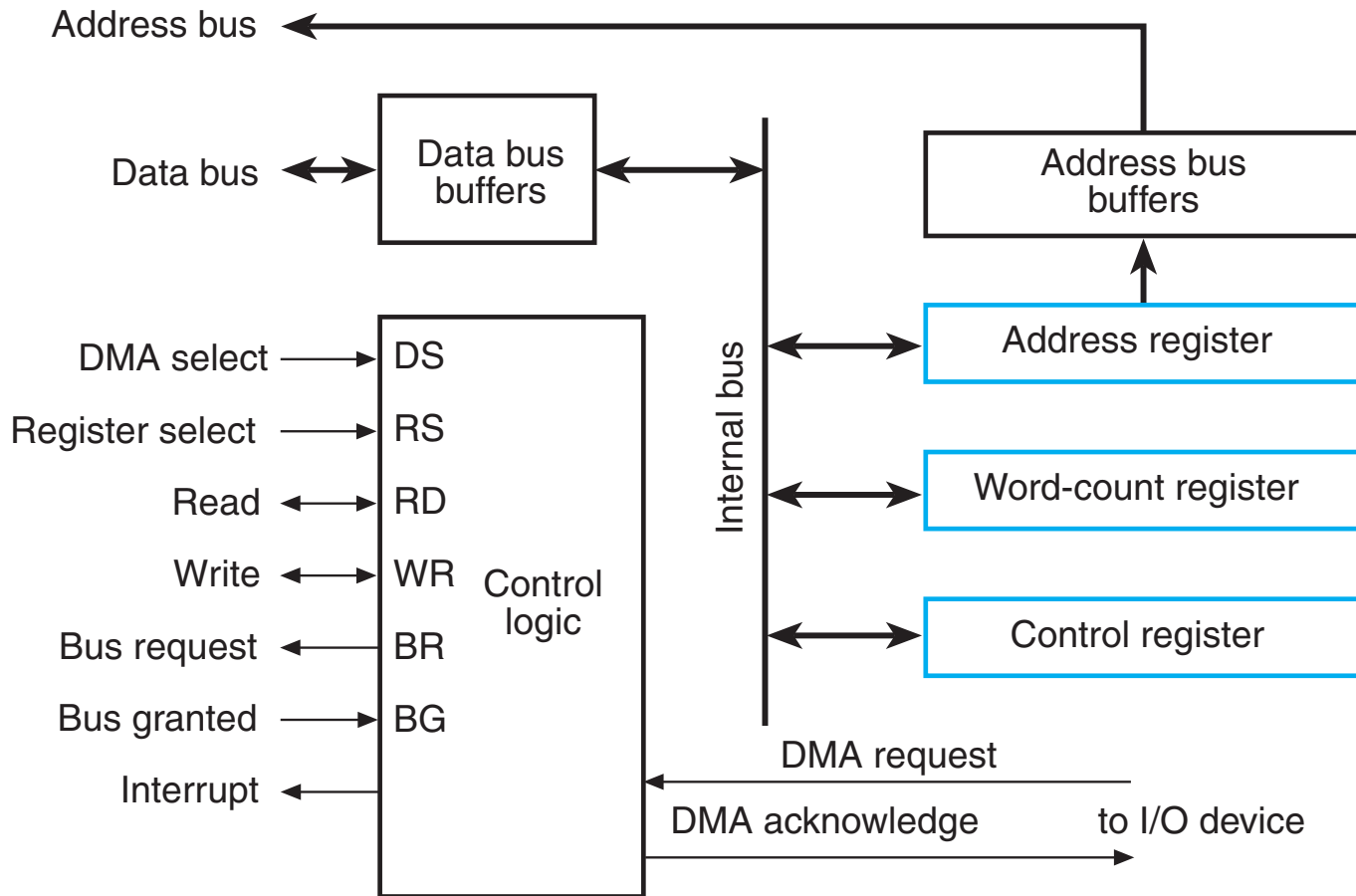


Fig. 11-19 Block Diagram of a DMA Controller

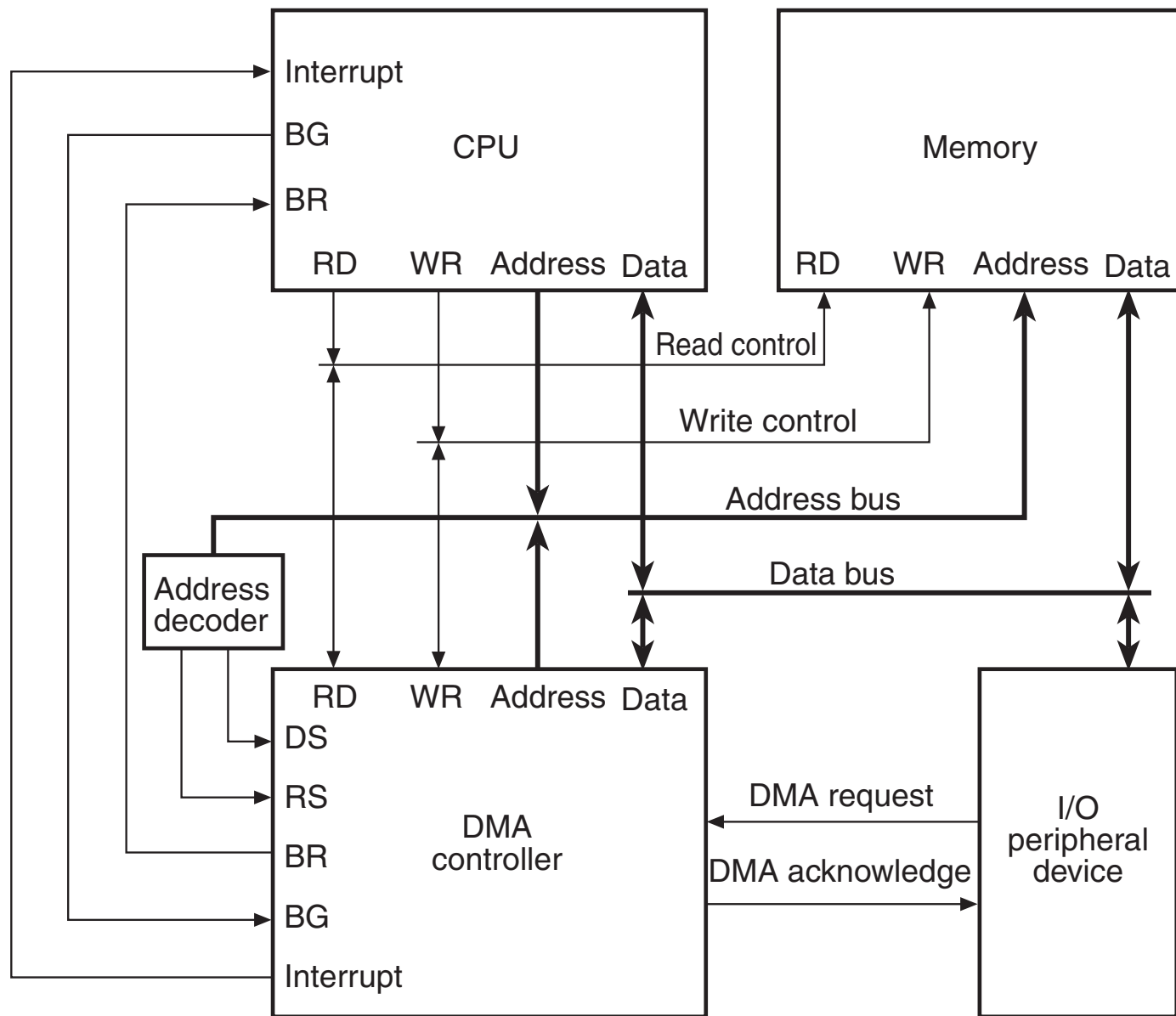


Fig. 11-20 DMA Transfer in a Computer System

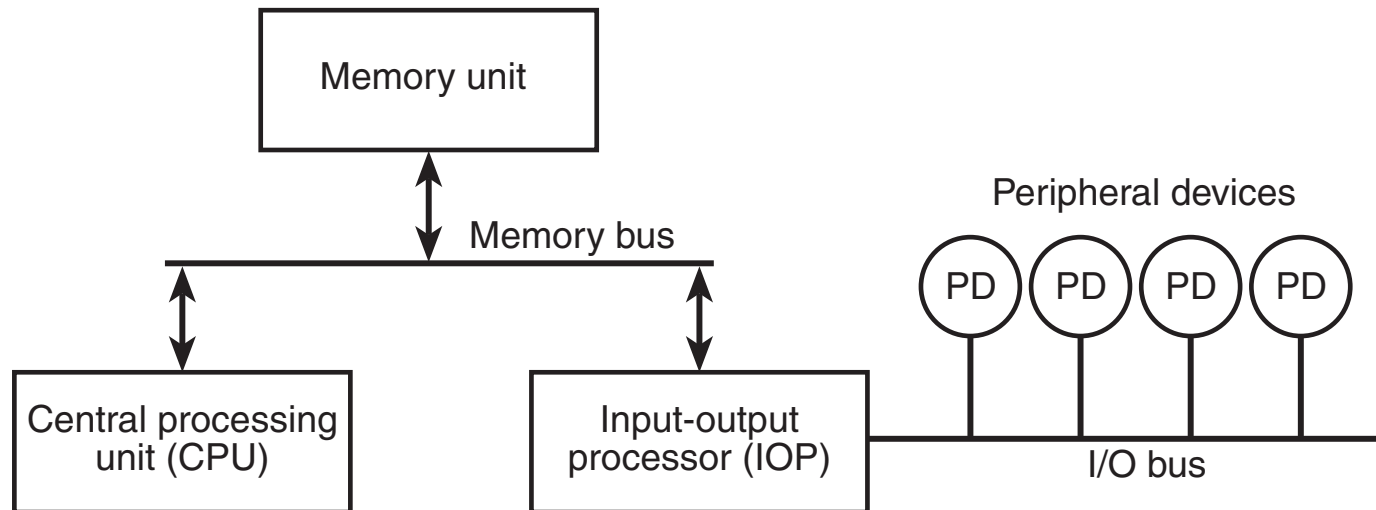


Fig. 11-21 Block Diagram of a Computer with I/O Processor

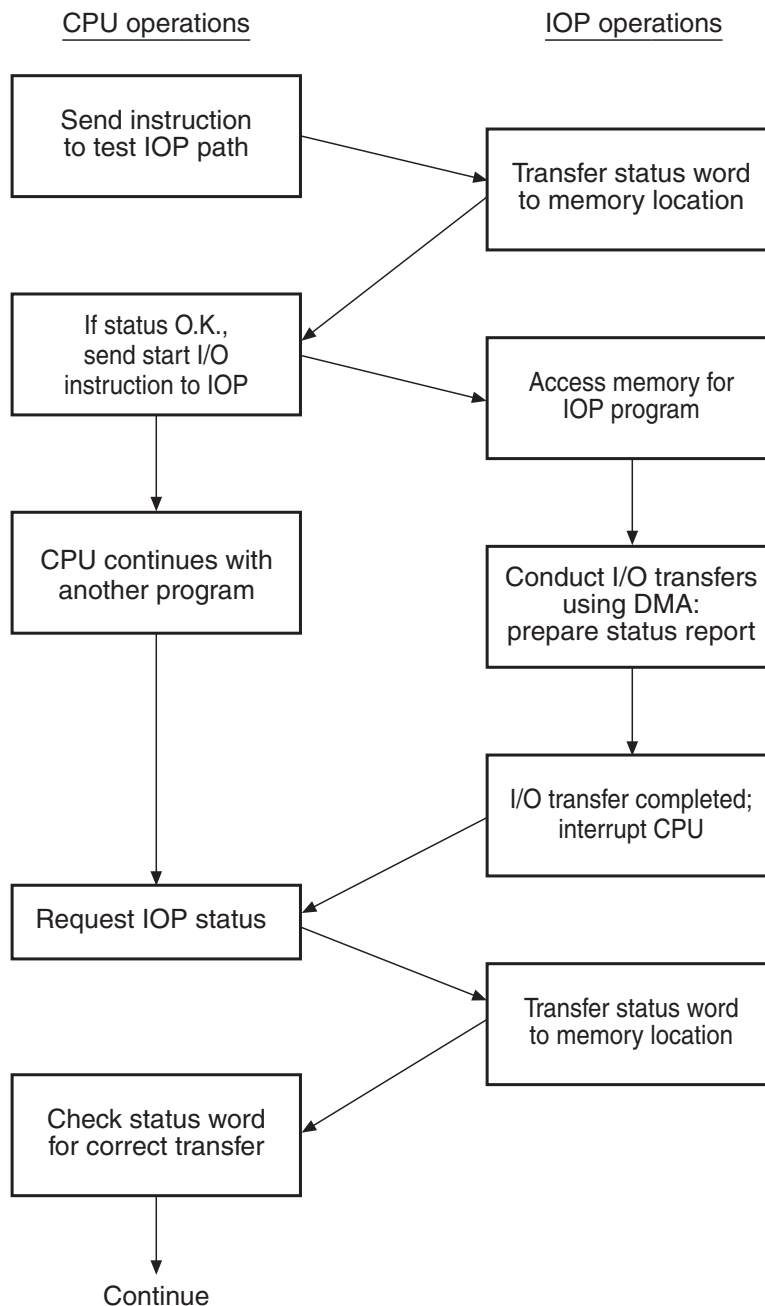


Fig. 11-22 CPU-IOP Communication