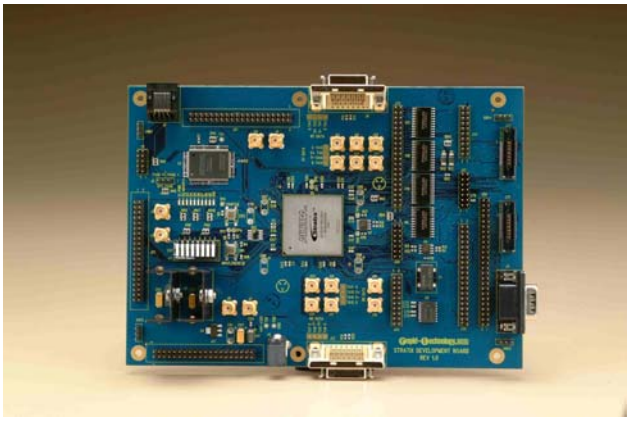
Stratix Development Board

January 2003, ver. 1.3 Data Sheet

Features

- Flexible and powerful development platform ideal for evaluating Altera Stratix™ device features. Ideal for analyzing high speed LVDS communication as well as DSP algorithm development. The board comes populated with a 1S10 device in a 780 pin Fineline BGA package (ordering code: DB-STRATIX1S10-F780).
- Support for several physical connections to device IO including:
  - Nine Channels of Receive and Transmit LVDS at 840 Mbps
    - 2 TX Data Channels + Clock and 2 RX Data Channels + Clock via SMA Connectors
    - 7 TX Data Channels + Clock and 7 RX Data Channels + Clock via 3M MDR (Mini-D-Ribbon) LVDS Connectors and Cabling
    - PCB Pads support Differential Probe analysis on select LVDS channels
  - General Purpose IO interfacing through 0.100" double row headers, well suited for standard ribbon cable connectors or wire wrap
  - Interfaces directly to DAC and ADC Evaluation Boards
  - Interfaces directly to TI DSP Evaluation Boards
  - Mictor Connectors support analysis with Tektronix and HP Test Equipment
  - Altera Santa Cruz Headers support existing and future development kits including the Nios Ethernet Development Kit and Linux Development Kit. These headers can also be used as General Purpose IO. One header supports 5V to 3.3V level shifting.
- Configuration through JTAG port or on board EPC8 configuration device
- Extra storage for Nios code or other algorithm development available in EPCS4 serial Flash device. Note, this socket will be populated when silicon becomes available.
- JTAG interface through RJ-45 connection or 10 pin header compatible with Altera ByteBlasterMV™ download cable or Rapid-Technology MVDC cable.
- Additional features:
  - Eight user-definable Switches, Two Pushbutton Switches
  - 52.5MHz socketed half size Crystal Oscillator
  - Eight user-definable LEDs
  - Power and Configuration LEDs



Picture 1. Stratix High Speed Development Board

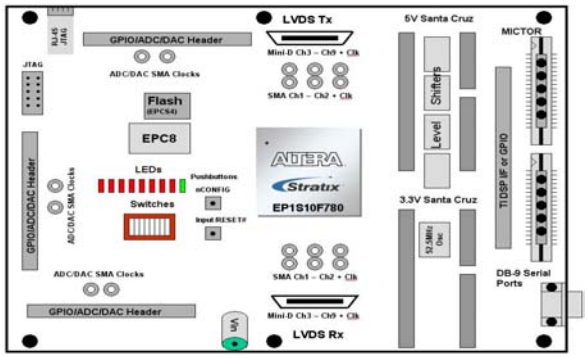


Figure 1. Stratix Development Board Functional Block Diagram

Picture 2. Stratix High Speed Development Kit

General Description

The Stratix development board provides an economical platform for hardware verification and testing. This board enables the user to quickly verify design functionality and timing. Several IO Connections are available including support for LVDS, ADC and DAC, TI DSP Development Kit interfacing, serial ports, and Mictor. These connections make this board an excellent evaluation platform to test various features of the Stratix device family. The optional Stratix Development Kit (ordering code: DK-STRATIX1S10-F780) provides everything needed for development including the Stratix Development Board, Altera QuartusII Web Edition Development Software, Desktop Power Supply, and a Rapid Technology Multi-Volt-Download-Cable (MVDC).

Integrated Circuitry

The board contains the following integrated circuitry: an EP1S10F780C5, EPC8LC100, EPCS4 (when available), 52.5 MHz socketed crystal oscillator, three voltage regulators, two clock drivers, four level shifters, and a RS-232 transceiver.

Board Power

The Stratix Development Board operates from a 6 to 12 VDC source that can be supplied through the barrel connector or from a supply through the power pads TB1(+) and TB2(-). The Stratix Development Kit comes with a desktop transformer and connects to the board through barrel connector J4. The barrel connector J4 is center positive (+). Make sure polarity is correct as reversing polarity may damage the components on the board.

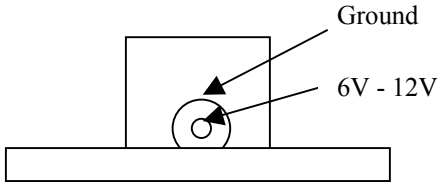


Figure 2. J1 Power Input Connector

I/O Power

The IO voltage (VCCIO rail) is set for 3.3V. See the Altera Stratix datasheet for further information about VCCIO, http://www.altera.com/literature/ds/ds_stx.pdf.

I/O Connectors

LVDS: The Stratix Development Board has 9 channels of LVDS transmit data and 9 channels of LVDS receive data. Two channels of Rx and Tx plus clock channel run through SMA connectors. Seven channels of Rx and Tx plus clock connect through 3M LVDS connector/cable (MDR-14526-EZ5B-xxx-02C). Each data channel runs at a speed of 840 Mbps. Connector pin assignments are shown in Appendix A.

ADC/DAC: The Stratix Development Board has three 40 pin I/O connectors (0.100" spacing) that can be used as general purpose IO or to connect to either Analog/Digital Converter or Digital/Analog Converter Evaluation Boards supplied by manufacturers. The connector pin-out is listed in Appendix A. A sample list of compatible TI and Analog Devices demo boards are listed in Appendix B.

DSP I/O Port: One connector supports a physical connection to TI DSP evaluation boards allowing quick and easy Stratix co-processing capability. The TI interface is shown in Appendix A.

Santa Cruz (Nios) Headers: There are two Altera Santa Cruz headers (3.3V and 5V) to support existing and future Altera development kits. Two examples of kits that are compatible with these headers are the Altera Nios Ethernet Development Kit and Nios Linux Development Kit. One header has 5V to 3.3V level shifters to support interfacing to 5V devices. The Santa Cruz header pin assignments are shown in Appendix A.

Mictor: Several I/O signals are mapped to Mictor connectors to connect directly to HP or Tektronix test equipment. See Appendix A for the pin assignments.

Serial Ports: There are two serial port connections from the Stratix device to RS-232 transceivers and a DB9 connector to support embedded Nios designs. Pin assignments for this connector are in Appendix A.

LEDs

The board has 10 LEDs, one Power LED, one Configuration LED, and eight user defined LEDs.

D1 "Power" LED. This green LED illuminates when the 3.3V rail is active.

D2 "Unconfig" LED. This red LED illuminates when the Stratix is NOT configured. It should be off when the chip is configured properly.

D3-D10 User Defined LEDs. The FPGA pins associated with these 8 LED's are referenced in Appendix A.

Switches

There are 8 user-defined switches. The FPGA pins associated with the 8 switches (SW3) are referenced in Appendix A.

SW1 connects to the Stratix DEV_CLRn pin, which can be configured in QuartusII to be a device wide clear OR a general purpose IO pin.

Config Device

The Stratix device configures from the EPC8 device. The EPC8 supports multiple configuration pages, or spaces. This board supports the selection of two pages with a jumper selection. Use the supplied shunt to select either Page 0 or Page 1. See Appendix A, section V for details.

JTAG

The JTAG connection to the EPC8 and the EP1S10 are through J1 or J2. J2 is the standard 10 pin header for the Altera ByteBlasterMV. J1 is an RJ-45 connector for the Rapid Technology JTAG Multi-Volt-Download-Cable (MVDC). The MVDC is compatible with Altera software and is functionally equivalent to the Altera ByteBlasterMV cable. Resistors R2 and R3 allow the JTAG chain to be viewed at selective points.

Sockets

Socket XY1 is an 8 pin DIP for a half-size 3.3V crystal oscillator. The board comes with a 52.5MHz crystal oscillator which can be replaced with a different frequency crystal oscillator if desired.

Development Kit

The optional Development Kit can be purchased which includes:

- The Stratix Development Board
- Desktop Power Supply
- Rapid-Technology Multi-Volt-Download-Cable (MVDC)
- Altera QuartusII Web Edition Development Software.

Visit www.rapid-technology.com for more details on the Kit.

Appendix A: Pin Tables

Note: The board comes with complete schematics as well as a tcl script which has all the pin assignments already selected and can easily be modified as needed.

I. JTAG

Signal Name	Connector	Pin	Connector	Pin
TCK	J1	6	J2	1
TDO	J1	5	J2	3
TDI	J1	2	J2	9
TMS	J1	4	J2	5

II. LEDs

LED	Signal Name	Stratix Pin	Comments
D3	LED0	F17	Stratix pin logic level "0" Turns On LED
D4	LED1	F19	Stratix pin logic level "0" Turns On LED
D5	LED2	G18	Stratix pin logic level "0" Turns On LED
D6	LED3	G19	Stratix pin logic level "0" Turns On LED
D7	LED4	H17	Stratix pin logic level "0" Turns On LED
D8	LED5	H18	Stratix pin logic level "0" Turns On LED
D9	LED6	J13	Stratix pin logic level "0" Turns On LED
D10	LED7	J17	Stratix pin logic level "0" Turns On LED
D1	Power	None	LED On Indicates power supplied to 3.3V rail
D2	Unconfig'd	G17	LED On Indicates FPGA is NOT configured

III. Switches

Switch	Location	Stratix Pin	Comments
SW1	-	AC9	Can be used as device wide clear if selected in Quartus device options.
SW2	-	L16	NO LOAD. Can be populated to force reconfiguration of device.
SW3	1	F10	
SW3	2	F12	
SW3	3	G10	
SW3	4	G11	
SW3	5	H11	
SW3	6	L11	
SW3	7	J11	Can be used as device wide OE if selected in Quartus device options.
SW3	8	J12	

Appendix A: Continued

IV. Stratix Clocks

Signal Name	Stratix Pin	Instance	Instance	Description
FPGA_CLK0	AC17	U6	3	Input, Osc Y1 drives clock driver U6 which drives Stratix
FPGA_CLK1	K17	U6	6	Input, Osc Y1 drives clock driver U6 which drives Stratix
ADC_CLK_IN0	W13	J7	1	Input from SMA connector J7
ADC_CLK_IN1	M17	J9	1	Input from SMA connector J9
ADC_CLK_IN2	AA17	J11	1	Input from SMA connector J11
CLK_STRATIX	AF15	U7	1	Output #2 from Stratix PLL#6 drives clock driver chip U7 Pin1
CLK_N1	W14	U1(B), J33	R2, 13	Output #1 from Stratix PLL#6 loops back to PLL#9, pin R2 and Nios header J33, pin 13
CLK_N2	AD15	J34	13	Driven by Nios header J34 pin 13
DAC_CLK_OUT0	E15	J8	1	Stratix Output #0 of PLL #5 drives SMA connector J8
DAC_CLK_OUT1	K14	J10	1	Stratix Output #1 of PLL #5 drives SMA connector J10
DAC_CLK_OUT2	C15	J12	1	Stratix Output #2 of PLL #5 drives SMA connector J12
HDR_CLK	W16	J33, J34	9, 9	Stratix Output #3 of PLL #6 drives Pin 9 of Nios headers J33 and J34

V. EPC8 Configuration Page Selection

Connector	Shunt Setting	Description
J3	1-2	Loads EPC8 Page 1 into FPGA
J3	2-3	Loads EPC8 Page 0 into FPGA

Appendix A: Continued

VI. LVDS – MDR Connectors

Signal Name	Stratix Pin	Connector	Pin	Test Point	Signal Name	Stratix Pin	Connector	Pin	Test Point
MR_DATA0+	L2	J13	13	TA5	MR_DATA0-	L1	J13	26	TA8
MR_DATA1+	K3	J13	24		MR_DATA1-	K4	J13	12	
MR_DATA2+	K2	J13	10		MR_DATA2-	K1	J13	23	
MR_DATA3+	J4	J13	21		MR_DATA3-	J3	J13	9	
MR_DATA4+	J2	J13	18		MR_DATA4-	J1	J13	6	
MR_DATA5+	H4	J13	4		MR_DATA5-	H3	J13	17	
MR_DATA6+	H2	J13	15		MR_DATA6-	H1	J13	3	
MR_CLK+	P4	J13	1		MR_CLK-	P3	J13	14	

Signal Name	Stratix Pin	Connector	Pin	Test Point	Signal Name	Stratix Pin	Connector	Pin	Test Point
MT_DATA0+	N22	J6	14	TA2	MT_DATA0-	N21	J6	1	TA1
MT_DATA1+	N24	J6	3		MT_DATA1-	N23	J6	15	
MT_DATA2+	M22	J6	17		MT_DATA2-	M21	J6	4	
MT_DATA3+	M24	J6	6		MT_DATA3-	M23	J6	18	
MT_DATA4+	L22	J6	9		MT_DATA4-	L21	J6	21	
MT_DATA5+	L23	J6	23		MT_DATA5-	L24	J6	10	
MT_DATA6+	K21	J6	12		MT_DATA6-	K22	J6	24	
MT_CLK+	L20	J6	26		MT_CLK-	L19	J6	13	

VII. LVDS – SMA Connectors

Signal Name	Stratix Pin	Connector	Pin	Test Point	Signal Name	Stratix Pin	Connector	Pin	Test Point
DR_DATA0+	T1	J15	1	TA10	DR_DATA0-	U2	J17	1	TA16
DR_DATA1+	U3	J19	1		DR_DATA1-	U4	J21	1	
DR_CLK+	R4	J23	1		DR_CLK-	R3	J25	1	

DT_DATA0+	T26	J14	1	TA9	DT_DATA0-	T25	J16	1	TA15
DT_DATA1+	T23	J18	1		DT_DATA1-	T24	J20	1	
DT_CLK+	U24	J22	1		DT_CLK-	U23	J24	1	

Appendix A: Continued

VIII. Mictor Connector #1

Signal Name	Stratix Pin	Connector	Pin
F_D31	K18	J27	8
F_D30	J18	J27	10
F_D29	K19	J27	12
F_D28	J19	J27	14
F_D27	L18	J27	16
F_D26	M18	J27	18
F_D25	L25	J27	20
F_D24	L26	J27	22
F_D23	P26	J27	24
F_D22	M11	J27	26
F_D21	M12	J27	28
F_D20	F8	J27	30
F_D19	L13	J27	32
F_D18	M2	J27	34
F_D17	AB2	J27	36
F_D16	AB1	J27	38
F_D15	V5	J27	7
F_D14	AA2	J27	9
F_D13	AA1	J27	11
F_D12	U7	J27	13
F_D11	U8	J27	15
F_D10	Y2	J27	17
F_D9	Y1	J27	19
F_D8	U6	J27	21
F_D7	U5	J27	23
F_D6	U9	J27	25
F_D5	U10	J27	27
F_D4	W2	J27	29
F_D3	W1	J27	31
F_D2	T6	J27	33
F_D1	T5	J27	35
F_D0	V4	J27	37
DAS_CLK0	U6 Pin 2	J27	5, 6
GND	-	J27	3, 39-43

Appendix A: Continued

IX. Mictor Connector #2

Signal Name	Stratix Pin	Connector	Pin	Comments
T_D15	Y19	J28	7	Also connects to J26
T_D14	V6	J28	9	Also connects to J26
T_D13	Y17	J28	11	Also connects to J26
T_D12	Y13	J28	13	Also connects to J26
T_D11	AA3	J28	15	Also connects to J26
T_D10	Y11	J28	17	Also connects to J26
T_D9	AA28	J28	19	Also connects to J26
T_D8	AA27	J28	21	Also connects to J26
T_D7	AA26	J28	23	Also connects to J26
T_D6	W3	J28	25	Also connects to J26
T_D5	V7	J28	27	Also connects to J26
T_D4	W6	J28	29	Also connects to J26
T_D3	W4	J28	31	Also connects to J26
T_D2	Y4	J28	33	Also connects to J26
T_D1	AA11	J28	35	Also connects to J26
T_D0	AB28	J28	37	Also connects to J26
T_RD#	G7	J28	8	Also connects to J26
T_STRB#	W19	J28	10	Also connects to J26
T_RS#	W18	J28	12	Also connects to J26
T_WE#	Y3	J28	14	Also connects to J26
T_WR#	AA25	J28	16	Also connects to J26
T_READY	W5	J28	18	Also connects to J26
F_DVALID#	T9	J28	20	
F_SYNC#	L17	J28	22	
F_PSTROBE-	R26	J28	24	
F_PSTROBE+	R25, T3	J28	26	
F_PIO2	V3	J28	28	
F_PIO1	T10	J28	30	
F_DIR#	T19	J28	32	
F_NRDY#	U25	J28	34	
F_SUSPEND#	V24	J28	36	
F_STROB	U26	J28	38	
DAS_CLK1	U6 Pin 7	J28	5, 6	
GND	-	J28	3, 39-43	

Appendix A: Continued

X. TI DSP or General Purpose IO

Signal Name	Stratix Pin	Connector	Pin
T_D0	AB28	J26	3
T_D1	AA11	J26	4
T_D2	Y4	J26	5
T_D3	W4	J26	6
T_D4	W6	J26	7
T_D5	V7	J26	8
T_D6	W3	J26	9
T_D7	AA26	J26	10
T_D8	AA27	J26	11
T_D9	AA28	J26	12
T_D10	Y11	J26	13
T_D11	AA3	J26	14
T_D12	Y13	J26	15
T_D13	Y17	J26	16
T_D14	V6	J26	17
T_D15	Y19	J26	18
T_A0	AB10	J26	19
T_A1	AB11	J26	20
T_A2	V10	J26	21
T_A3	AA4	J26	22
T_A4	AB27	J26	23
T_A5	V19	J26	24
T_A6	V20	J26	25
T_A7	V21	J26	26
T_A8	Y25	J26	27
T_A9	Y26	J26	28
T_A10	W23	J26	29
T_A11	W24	J26	30
T_A12	V8	J26	31
T_A13	V9	J26	32
T_A14	V22	J26	33
T_A15	V23	J26	34
T_PS#	W12	J26	37
T_READY	W5	J26	39
T_WR#	AA25	J26	41
T_WE#	Y3	J26	43
T_RS#	W18	J26	47
T_DS#	W10	J26	38
T_IS#	W11	J26	40
T_STRB#	W19	J26	42
T_RD#	G7	J26	44

Appendix A: Continued

XI. A/D & D/A or General Purpose IO Headers

Signal Name	Stratix Pin	Connector	Pin	Signal Name	Stratix Pin	Connector	Pin
JA_IO_0	A3	JA1	1	JB_IO_0	B24	JB1	1
JA_IO_1	A4	JA1	3	JB_IO_1	B25	JB1	3
JA_IO_2	A5	JA1	5	JB_IO_2	B26	JB1	5
JA_IO_3	B3	JA1	7	JB_IO_3	A24	JB1	7
JA_IO_4	B4	JA1	9	JB_IO_4	A25	JB1	9
JA_IO_5	B5	JA1	11	JB_IO_5	A26	JB1	11
JA_IO_6	C4	JA1	13	JB_IO_6	C18	JB1	13
JA_IO_7	C5	JA1	15	JB_IO_7	C19	JB1	15
JA_IO_8	C6	JA1	17	JB_IO_8	C20	JB1	17
JA_IO_9	C7	JA1	19	JB_IO_9	C21	JB1	19
JA_IO_10	C8	JA1	21	JB_IO_10	C22	JB1	21
JA_IO_11	C9	JA1	23	JB_IO_11	C23	JB1	23
JA_IO_12	C10	JA1	25	JB_IO_12	C24	JB1	25
JA_IO_13	C11	JA1	27	JB_IO_13	C25	JB1	27
JA_IO_14	D5	JA1	29	JB_IO_14	D18	JB1	29
JA_IO_15	D6	JA1	31	JB_IO_15	D19	JB1	31
JA_IO_16	D7	JA1	33	JB_IO_16	D20	JB1	33
JA_IO_17	D8	JA1	35	JB_IO_17	D21	JB1	35
JA_IO_18	D9	JA1	37	JB_IO_18	D22	JB1	37
JA_IO_19	D10	JA1	39	JB_IO_19	D23	JB1	39
JA_IO_20	D11	JA1	2	JB_IO_20	D24	JB1	2
JA_IO_21	E6	JA1	36	JB_IO_21	E19	JB1	36
JA_IO_22	E8	JA1	38	JB_IO_22	E21	JB1	38
JA_IO_23	E10	JA1	40	JB_IO_23	E23	JB1	40

JC_IO_0	A6	JC1	1	JC_IO_12	B6	JC1	25
JC_IO_1	A7	JC1	3	JC_IO_13	B7	JC1	27
JC_IO_2	A8	JC1	5	JC_IO_14	B8	JC1	29
JC_IO_3	A9	JC1	7	JC_IO_15	B9	JC1	31
JC_IO_4	A10	JC1	9	JC_IO_16	B10	JC1	33
JC_IO_5	A11	JC1	11	JC_IO_17	B11	JC1	35
JC_IO_6	A18	JC1	13	JC_IO_18	B18	JC1	37
JC_IO_7	A19	JC1	15	JC_IO_19	B19	JC1	39
JC_IO_8	A20	JC1	17	JC_IO_20	B20	JC1	2
JC_IO_9	A21	JC1	19	JC_IO_21	B21	JC1	36
JC_IO_10	A22	JC1	21	JC_IO_22	B22	JC1	38
JC_IO_11	A23	JC1	23	JC_IO_23	B23	JC1	40

Appendix A: Continued

XII. Santa Cruz (Nios) 5V Connectors

Signal Name	Stratix Pin*	Connector	Pin
CARD_SEL_N2#	AB18	J32	38
N2_HIO_0	AH19	J32	3
N2_HIO_1	AH20	J32	4
N2_HIO_2	AH21	J32	5
N2_HIO_3	AH22	J32	6
N2_HIO_4	AH23	J32	7
N2_HIO_5	AH24	J32	8
N2_HIO_6	AH25	J32	9
N2_HIO_7	AH26	J32	10
N2_HIO_8	AG18	J32	11
N2_HIO_9	AG19	J32	12
N2_HIO_10	AG20	J32	13
N2_HIO_11	AG21	J32	14
N2_HIO_12	AG22	J32	15
N2_HIO_13	AG23	J32	16
N2_HIO_14	AG24	J32	17
N2_HIO_15	AG25	J32	18
N2_HIO_16	AG26	J32	21
N2_HIO_17	AF18	J32	23
N2_HIO_18	AF19	J32	25
N2_HIO_19	AF20	J32	27
N2_HIO_20	AF21	J32	28
N2_HIO_21	AF22	J32	29
N2_HIO_22	AF23	J32	31
N2_HIO_23	AF24	J32	32
N2_HIO_24	AF25	J32	33
N2_HIO_25	AE18	J32	35
N2_HIO_26	AE19	J32	36
N2_HIO_27	AE20	J32	37
N2_HIO_28	AE21	J32	39

Signal Name	Stratix Pin	Connector	Pin
N2_HIO_29	AE22	J31	4
N2_HIO_30	AE23	J31	5
N2_HIO_31	AE24	J31	6
N2_HIO_32	AD18	J31	7
N2_HIO_33	AD19	J31	8
N2_HIO_34	AA20	J31	9
N2_HIO_35	AD21	J31	10
N2_HIO_36	AB19	J31	11
N2_HIO_37	AD23	J31	12
N2_HIO_38	AC19	J31	13
N2_HIO_39	AC21	J31	14
HDR_CLK	W16	J34	9
CLK_STRATIX1	U7, Pin 3	J34	11
CLK_N2	AD14	J34	13

* Note: Level shifters U9-U12 separate Stratix device from 5V connectors J31, J32, J34

Appendix A: Continued

XIII. Santa Cruz (Nios) 3.3V Connectors

Signal Name	Stratix Pin	Connector	Pin
N1_IO_0	AH3	J30	3
N1_IO_1	AH4	J30	4
N1_IO_2	AH5	J30	5
N1_IO_3	AH6	J30	6
N1_IO_4	AH7	J30	7
N1_IO_5	AH8	J30	8
N1_IO_6	AH9	J30	9
N1_IO_7	AH10	J30	10
N1_IO_8	AH11	J30	11
N1_IO_9	AG3	J30	12
N1_IO_10	AG4	J30	13
N1_IO_11	AG5	J30	14
N1_IO_12	AG6	J30	15
N1_IO_13	AG7	J30	16
N1_IO_14	AG8	J30	17
N1_IO_15	AG9	J30	18
N1_IO_16	AG10	J30	21
N1_IO_17	AG11	J30	23
N1_IO_18	AF4	J30	25
N1_IO_19	AF5	J30	27
N1_IO_20	AF6	J30	28
N1_IO_21	AF7	J30	29
N1_IO_22	AF8	J30	31
N1_IO_23	AF9	J30	32
N1_IO_24	AF10	J30	33
N1_IO_25	AF11	J30	35
N1_IO_26	AB17	J30	36
N1_IO_27	AE4	J30	37
N1_IO_28	AE5	J30	39

Signal Name	Stratix Pin	Connector	Pin
N1_IO_29	AE6	J29	4
N1_IO_30	AE7	J29	5
N1_IO_31	AE8	J29	6
N1_IO_32	AE9	J29	7
N1_IO_33	AE10	J29	8
N1_IO_34	AE11	J29	9
N1_IO_35	AD6	J29	10
N1_IO_36	AD8	J29	11
N1_IO_37	AB7	J29	12
N1_IO_38	AD10	J29	13
N1_IO_39	AC10	J29	14
HDR_CLK	W16	J33	9
CLK_STRATIX0	U7, Pin 2	J33	11
CLK_N1	R2	J33	13

Appendix A: Continued

XIV. EPCS4 Interface

Signal Name	Stratix Pin	EPCS4	Pin
PROM_ASDI	Y9	U13	5
PROM_DCLK	V11	U13	6
PROM_nCS	V18	U13	1
PROM_DATA	J9	U13	2

XV. DB9 (RS-232) Interface

Signal Name	DB9 Connector	Pin	Stratix Pin*	Comments
TXD0	J5	2	M3	Transmit data channel 0
RXD0	J5	3	T20	Receive data channel 0
TXD1	J5	8	N6	Transmit data channel 1
RXD1	J5	7	T22	Receive data channel 1

*Note: Stratix interfaces to DB9 (J5) through RS-232 transceiver U5

XVI. TB (Vias) and TP (Test Pads)

TB	Function
TB1	Input supply, +6V - +12V. Can be used for lab supply connection points.
TB2	Input supply, GND

TP	Function
TP1	CONF_DONE (Stratix Pin G17)
TP2	CONFIG# (Stratix Pin L16)
TP3	Stratix TEMPDIODEn pin C14
TP4	Stratix TEMPDIODEp pin B14
TP5	Output of clock driver (U7, Pin 6)
TP6	Output of clock driver (U7, Pin 7)
TP7	Unused TP for user, Stratix CLK0p (Pin P27)
TP8	Unused TP for user, Stratix CLK0n (Pin N27)

Appendix B: Compatible ADC and DAC Eval Boards

Compatible Evaluation Board Pinouts

ADC	
Manufacturer	Part Number
Analog Devices	AD6645**
Analog Devices	AD7470
Analog Devices	AD7472
Analog Devices	AD9214
Analog Devices	AD9235
Analog Devices	AD9433

DAC	
Manufacturer	Part Number
Analog Devices	AD9708
Analog Devices	AD9751*
Analog Devices	AD9752
Analog Devices	AD9753*
Analog Devices	AD9754
Analog Devices	AD9755*
Analog Devices	AD9760
Analog Devices	AD9761
Analog Devices	AD9762
Analog Devices	AD9764

** Requires a 50 Pin header

* Dual DAC

This is a partial list. Almost any ADC evaluation board compatible with the HSC-ADC-EVAL-SC/DC FIFO board will connect to this board.