



# Current Mode PWM Controller

## FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

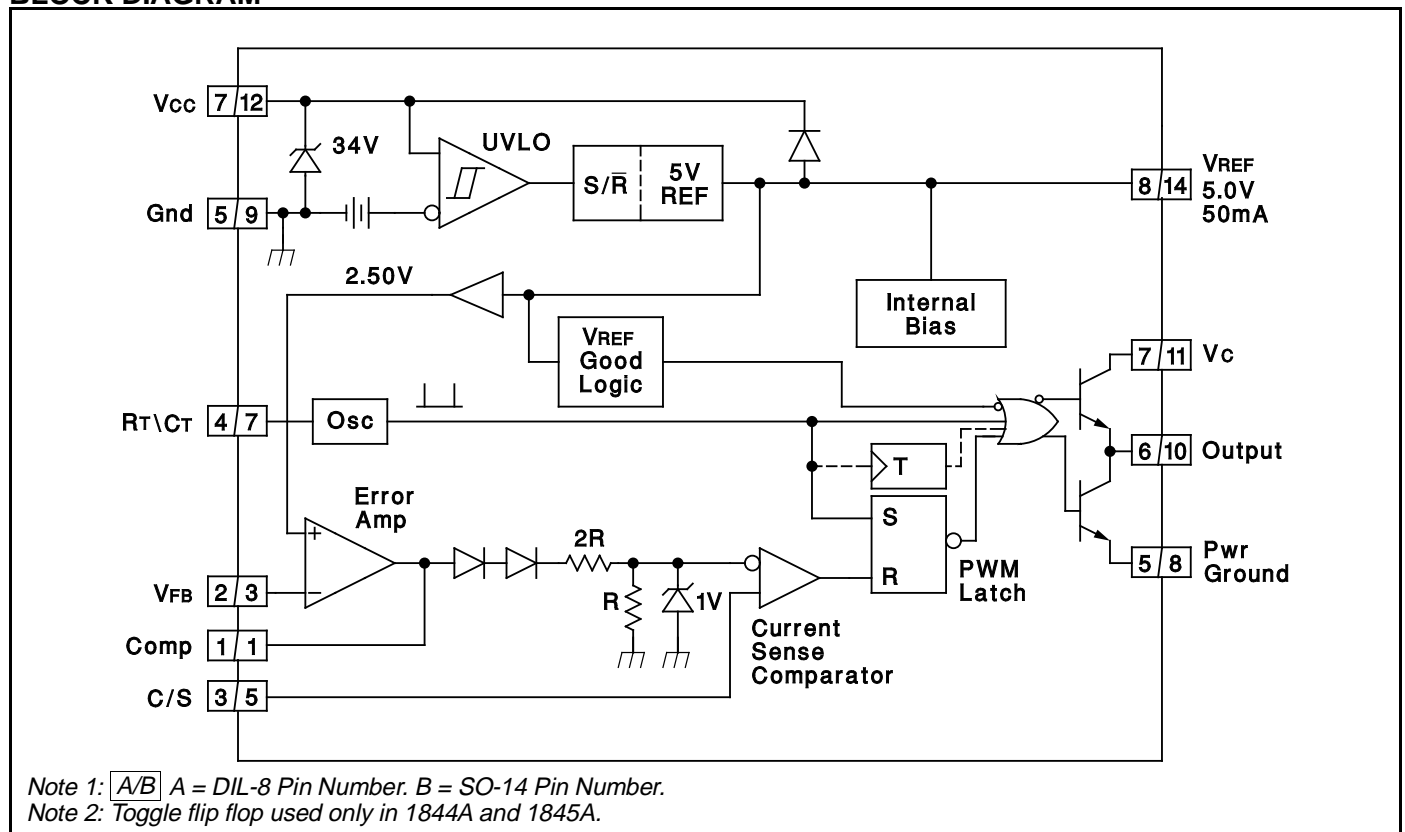
## DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for Vcc over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

## BLOCK DIAGRAM

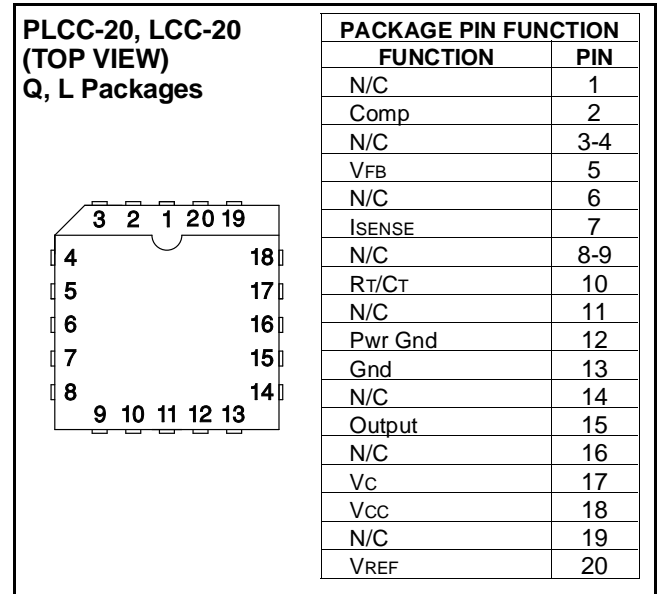
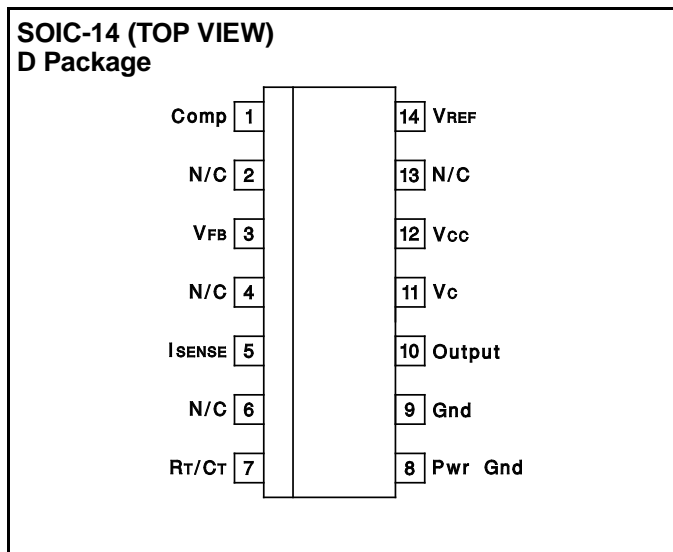
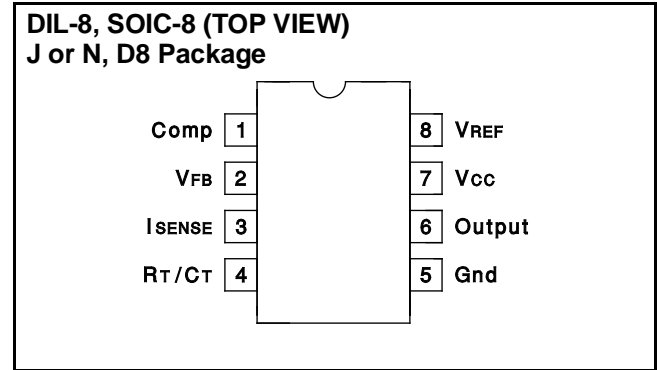


**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage (Low Impedance Source) . . . . .	30V
Supply Voltage (I <sub>CC</sub> mA) . . . . .	Self Limiting
Output Current . . . . .	±1A
Output Energy (Capacitive Load) . . . . .	5μJ
Analog Inputs (Pins 2, 3) . . . . .	-0.3V to +6.3V
Error Amp Output Sink Current . . . . .	10mA
Power Dissipation at T <sub>A</sub> ≤ 25°C (DIL-8) . . . . .	1W
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . .	300°C

Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

**CONNECTION DIAGRAMS**



**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, these specifications apply for -55°C ≤ T<sub>A</sub> ≤ 125°C for the UC184xA; -40°C ≤ T<sub>A</sub> ≤ 85°C for the UC284xA; 0 ≤ T<sub>A</sub> ≤ 70°C for the UC384xA; V<sub>CC</sub> = 15V (Note 5); R<sub>T</sub> = 10k; C<sub>T</sub> = 3.3nF; T<sub>A</sub> = T<sub>J</sub>; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA/UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<b>Reference Section</b>								
Output Voltage	T <sub>J</sub> = 25°C, I <sub>o</sub> = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V <sub>IN</sub> ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ I <sub>o</sub> ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz T <sub>J</sub> = 25°C (Note 2)		50			50		μV
Long Term Stability	T <sub>A</sub> = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
<b>Oscillator Section</b>								
Initial Accuracy	T <sub>J</sub> = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V <sub>CC</sub> ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub> (Note 2)		5			5		%
Amplitude	V <sub>PIN 4</sub> peak to peak (Note 2)		1.7			1.7		V
Discharge Current	T <sub>J</sub> = 25°C, V <sub>PIN 4</sub> = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	V <sub>PIN 4</sub> = 2V (Note 8)	7.5		8.8	7.6		8.8	mA

**ELECTRICAL CHARACTERISTICS (cont.)** Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  for the UC184xA;  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  for the UC284xA;  $0 \leq T_A \leq 70^{\circ}\text{C}$  for the UC384xA;  $V_{CC} = 15\text{V}$  (Note 5);  $R_T = 10\text{k}$ ;  $C_T = 3.3\text{nF}$ ;  $T_A = T_J$ ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA/UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<b>Error Amp Section</b>								
Input Voltage	$V_{PIN 1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	$\mu\text{A}$
AVOL	$2 \leq V_O \leq 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth	$T_J = 25^{\circ}\text{C}$ (Note 2)	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN 2} = 2.7\text{V}$ , $V_{PIN 1} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{PIN 2} = 2.3\text{V}$ , $V_{PIN 1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	$V_{PIN 2} = 2.3\text{V}$ , $R_L = 15\text{k}$ to ground	5	6		5	6		V
VOUT Low	$V_{PIN 2} = 2.7\text{V}$ , $R_L = 15\text{k}$ to Pin 8		0.7	1.1		0.7	1.1	V
<b>Current Sense Section</b>								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN 1} = 5\text{V}$ (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	$\mu\text{A}$
Delay to Output	$V_{PIN 3} = 0$ to $2\text{V}$ (Note 2)		150	300		150	300	ns
<b>Output Section</b>								
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		15	2.2		15	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12	13.5		12	13.5		V
Rise Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
Fall Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
UVLO Saturation	$V_{CC} = 5\text{V}$ , $I_{SINK} = 10\text{mA}$		0.7	1.2		0.7	1.2	V
<b>Under-Voltage Lockout Section</b>								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After TurnOn	x842A/4A	9	10	11	8.5	10	11.5	V
	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
<b>PWM Section</b>								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
<b>Total Standby Current</b>								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	$V_{PIN 2} = V_{PIN 3} = 0\text{V}$		11	17		11	17	mA
Vcc Zener Voltage	$I_{CC} = 25\text{mA}$	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with  $V_{PIN 2} = 0$ .

Note 4: Gain defined as:  $A = \frac{\Delta V_{PIN 1}}{\Delta V_{PIN 3}}$ ;  $0 \leq V_{PIN 3} \leq 0.8\text{V}$ .

Note 5: Adjust  $V_{CC}$  above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

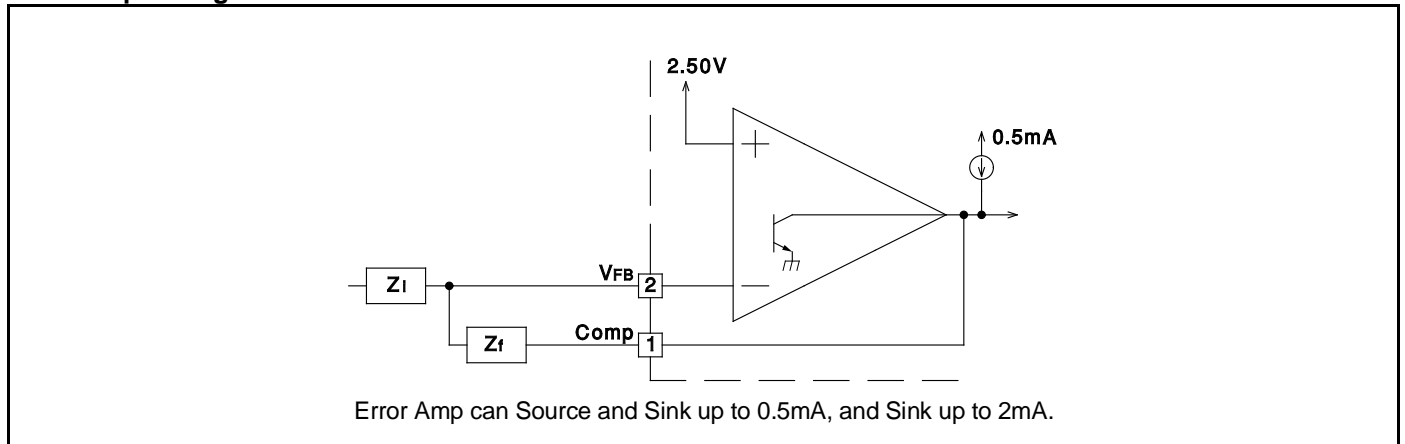
Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(\text{max}) - V_{REF}(\text{min})}{T_J(\text{max}) - T_J(\text{min})}$$

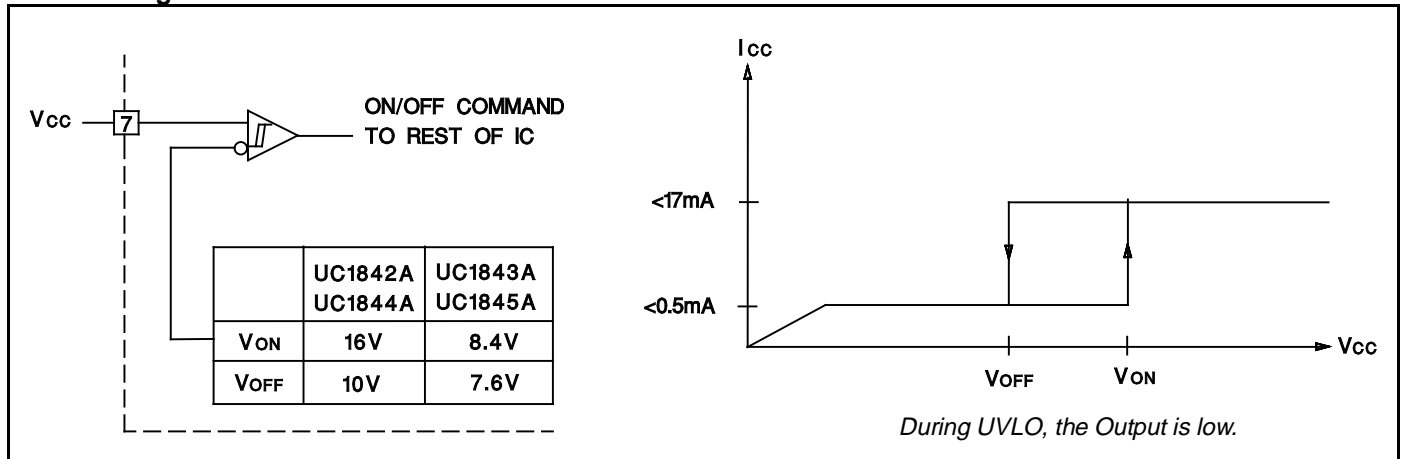
$V_{REF}(\text{max})$  and  $V_{REF}(\text{min})$  are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

Note 8: This parameter is measured with  $R_T = 10\text{k}\Omega$  to  $V_{REF}$ . This contributes approximately  $300\mu\text{A}$  of current to the measurement. The total current flowing into the  $R_T/C_T$  pin will be approximately  $300\mu\text{A}$  higher than the measured value.

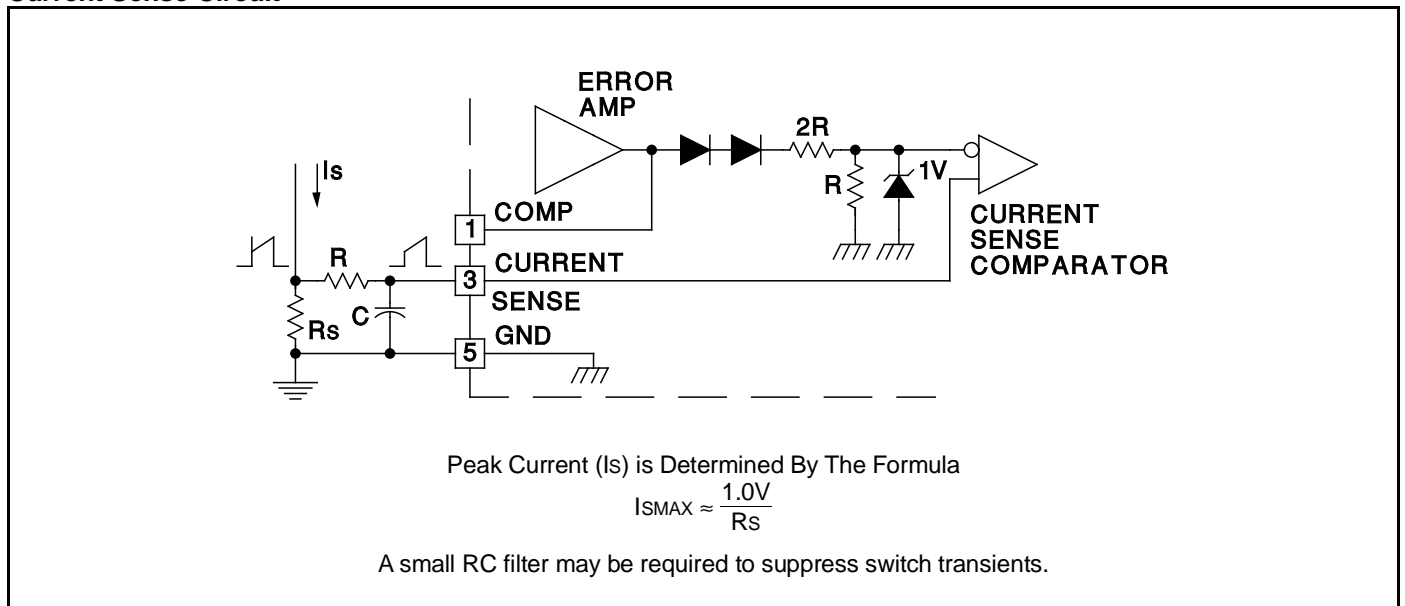
### Error Amp Configuration



### Under-Voltage Lockout

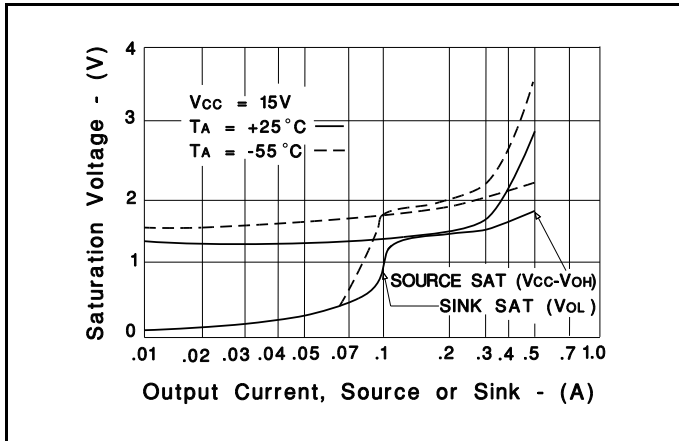


### Current Sense Circuit

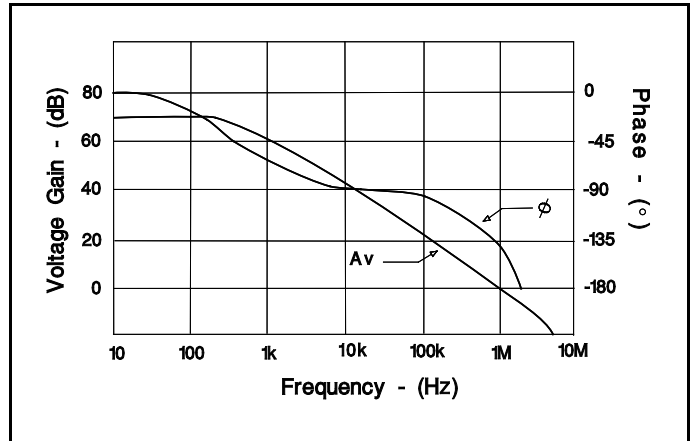


APPLICATIONS DATA (cont.)

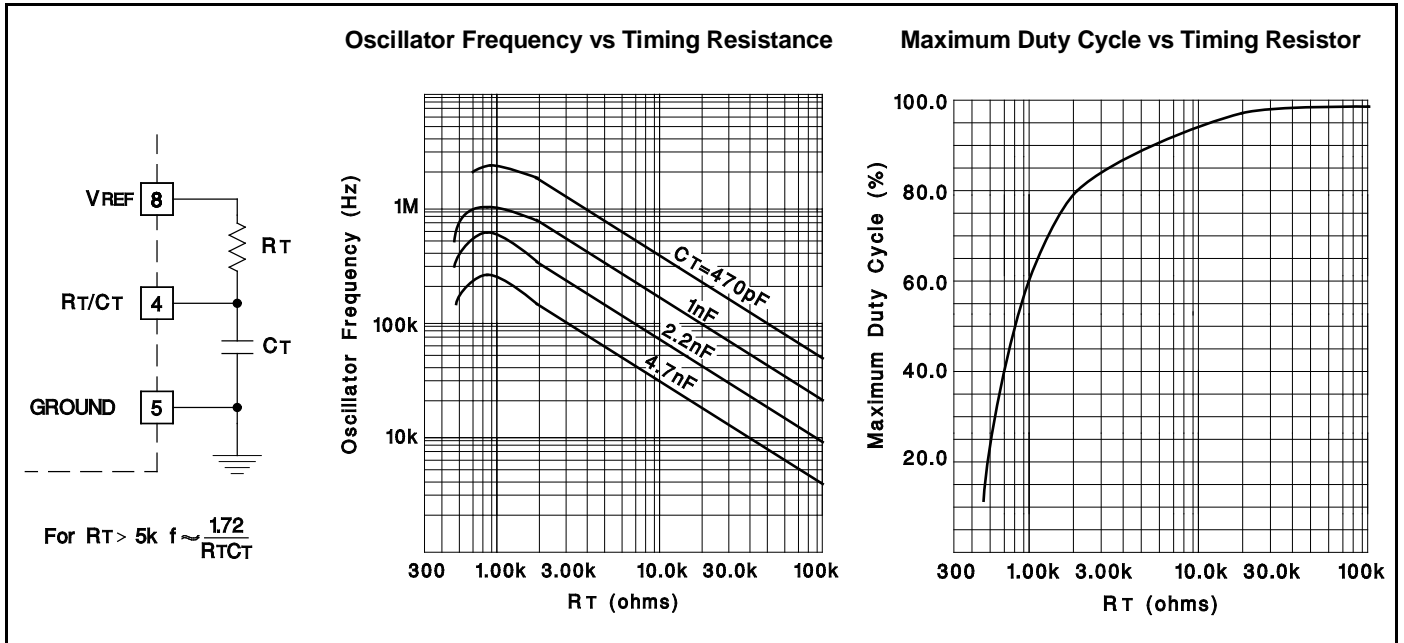
Output Saturation Characteristics



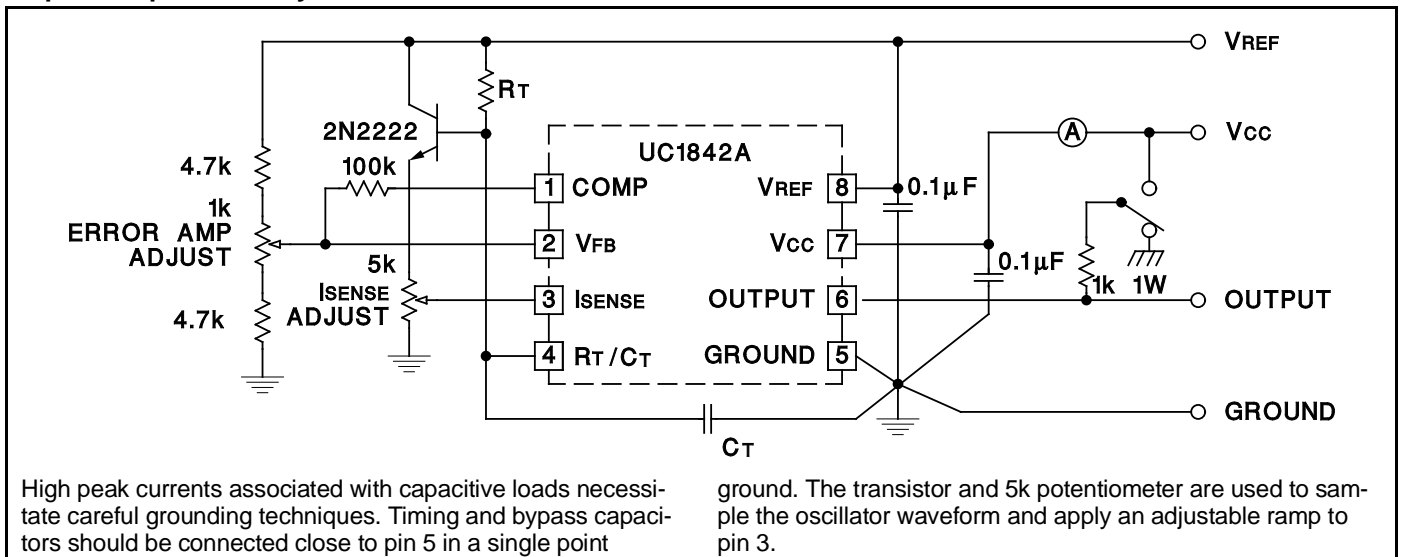
Error Amplifier Open-Loop Frequency Response



Oscillator Section

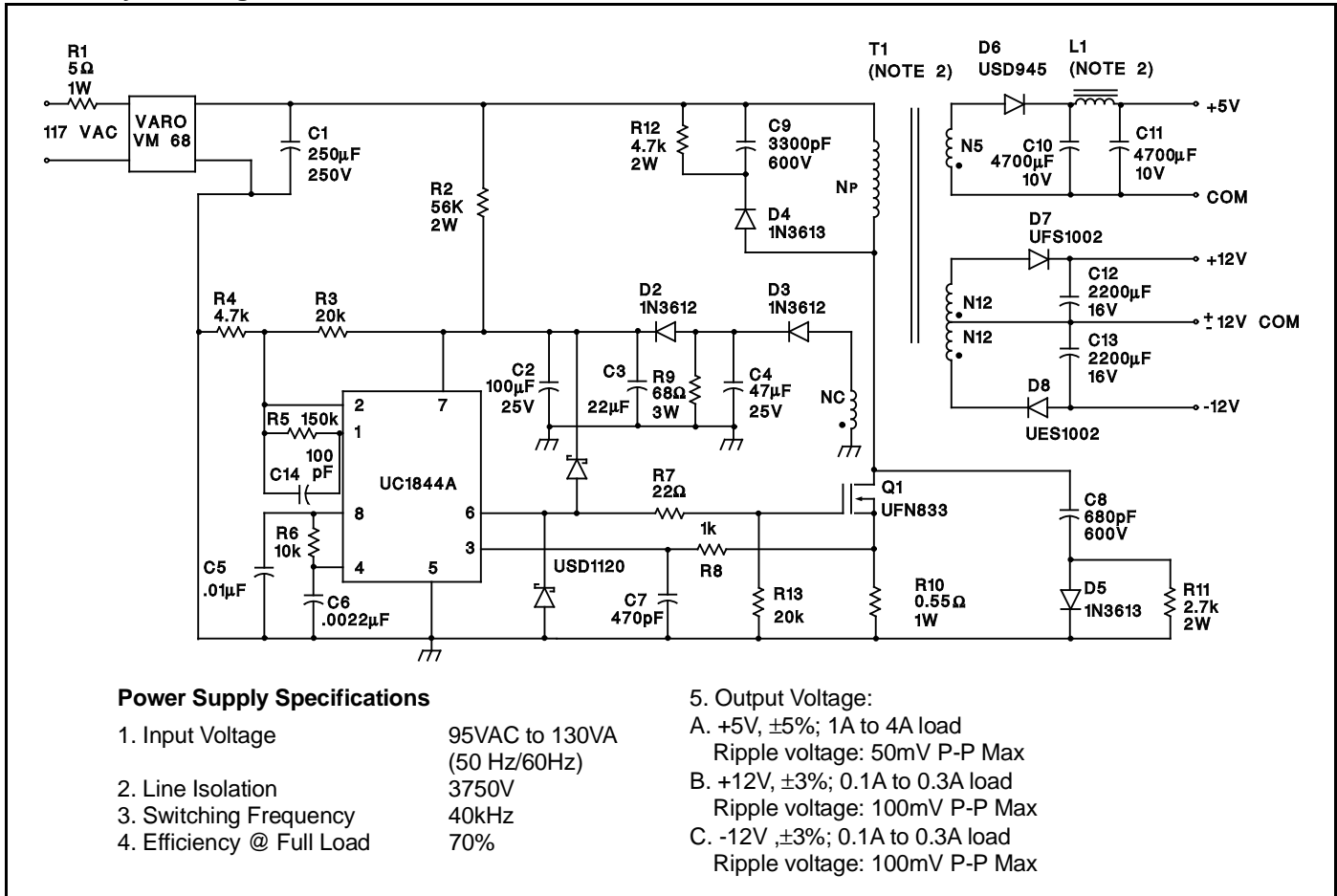


Open-Loop Laboratory Test Fixture

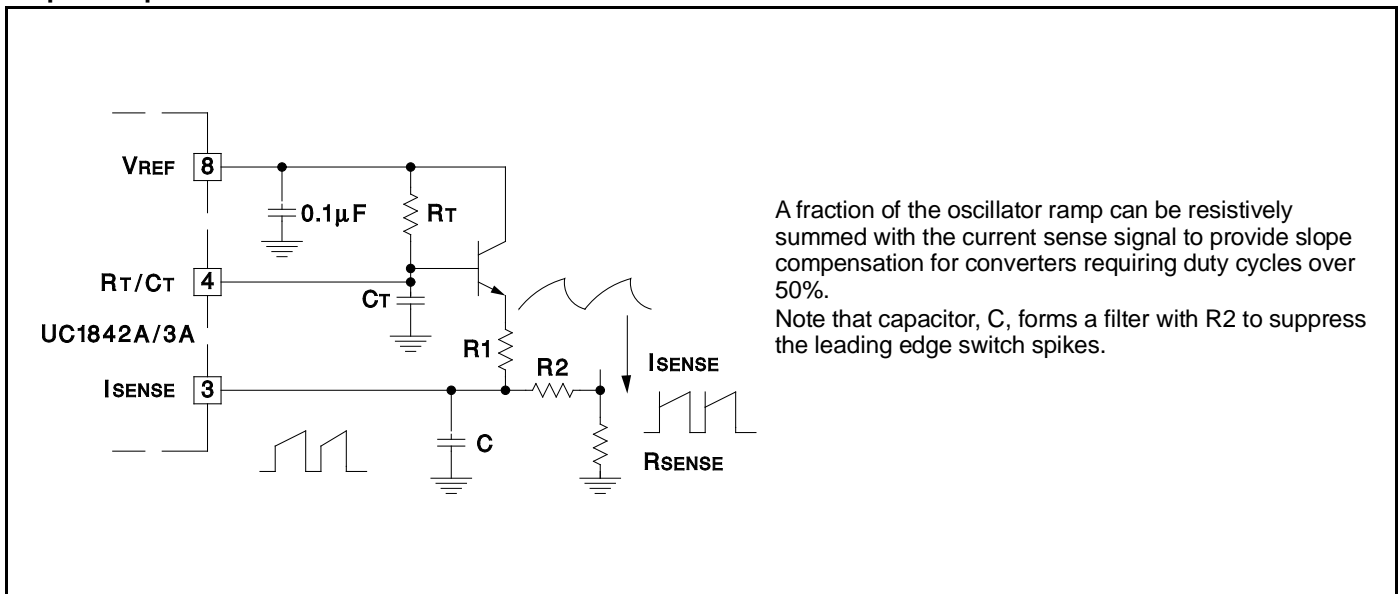


APPLICATIONS DATA (cont.)

Off-line Flyback Regulator



Slope Compensation



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